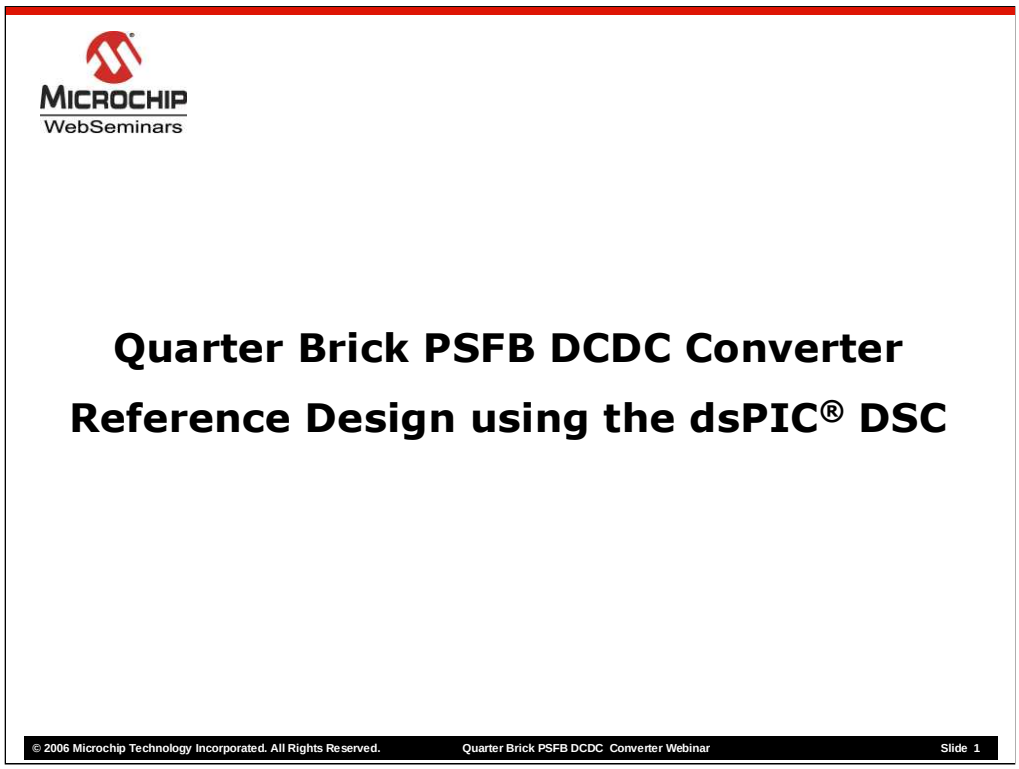
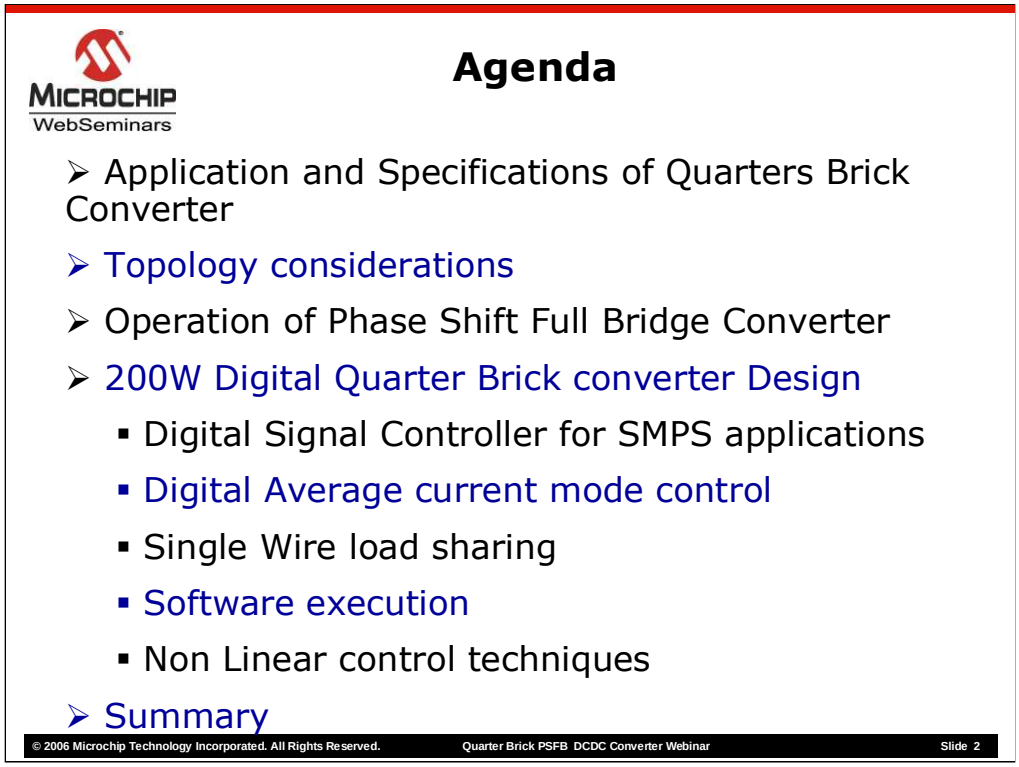
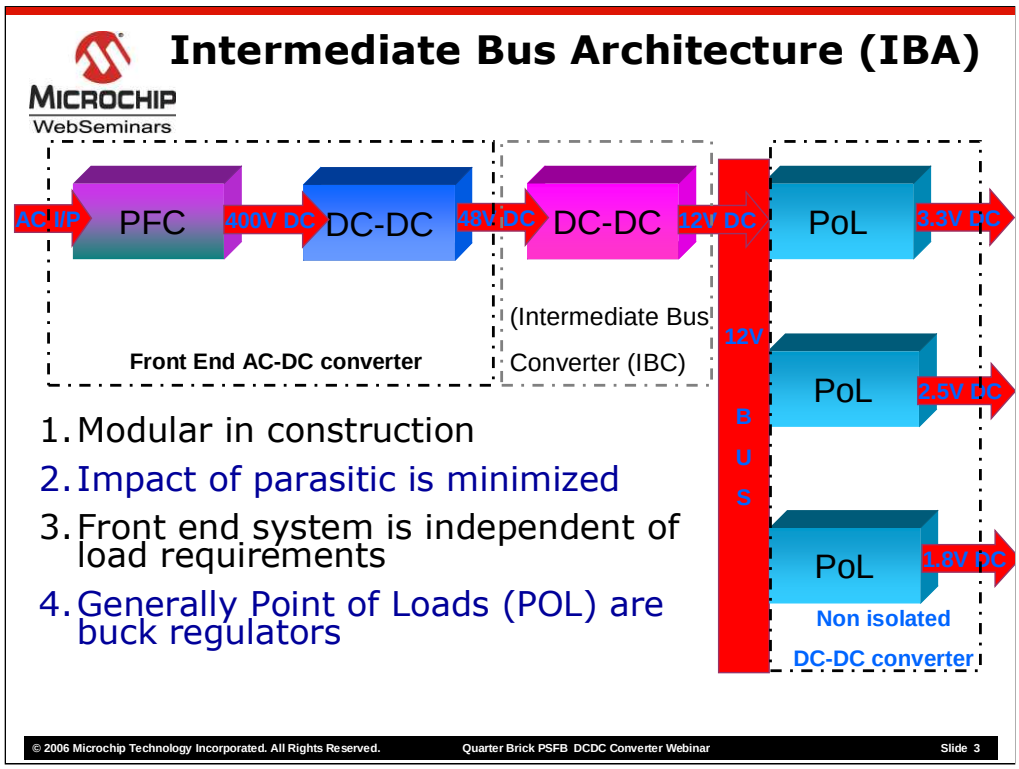



Welcome to the Quarter Brick Phase Shift Full Bridge DCDC converter web seminar: My Name is Ramesh Kankanala and I am a Principal Application Engineer at Microchip technology Inc.



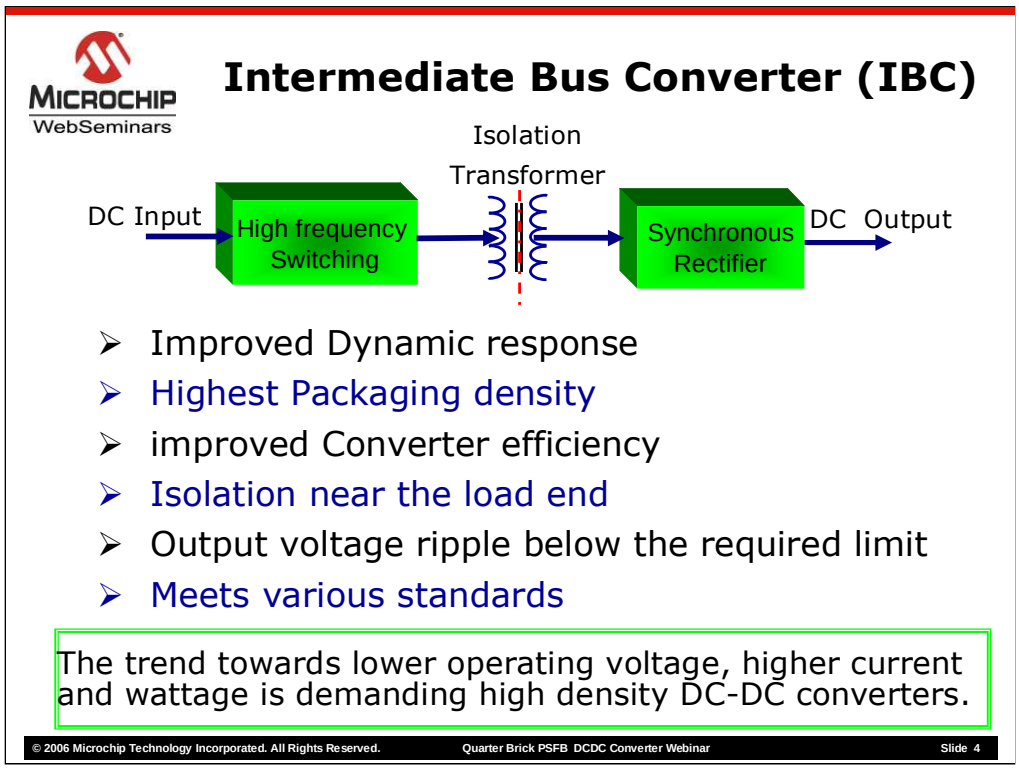

This session provides an overview of the digital 200W Quarter Brick Phase Shifted Full Bridge DCDC converter operations, Applications, advantages and specifications.

We will also discuss Digital Signal Controller (DSC) in SMPS applications, digital average current mode control design, single wire load sharing and few non linear controller techniques.

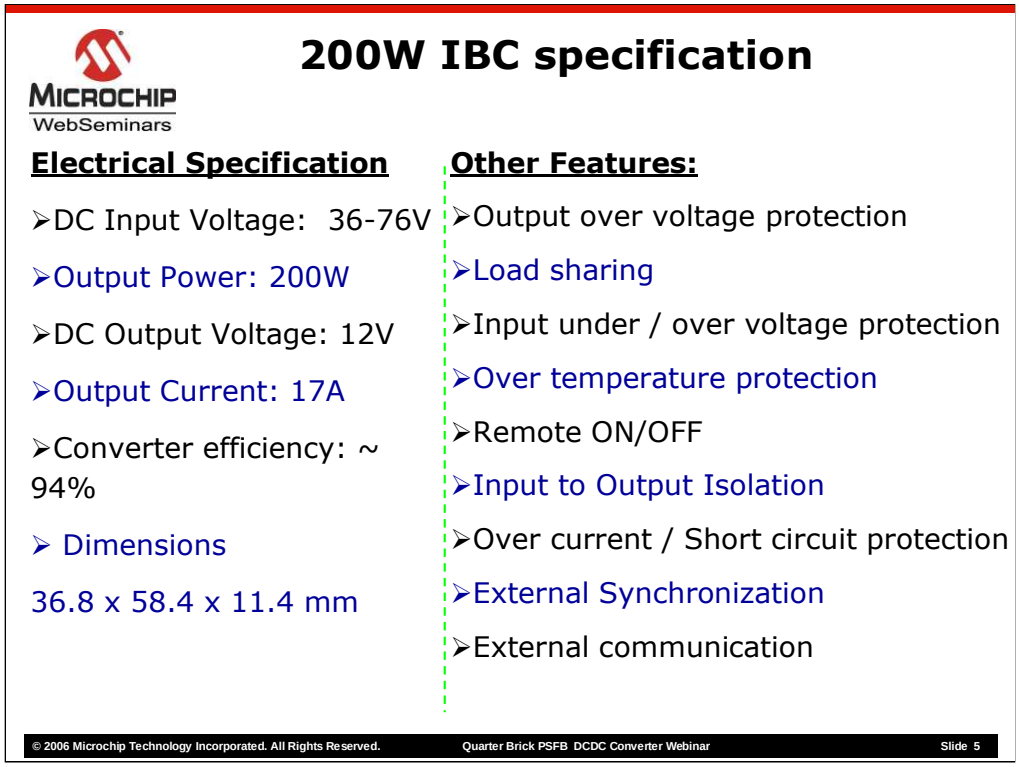



Intermediate Bus Architecture (IBA) is one of the prominent configurations used in server and telecom applications. The Front end AC/DC converter output is 48V in the IBA. This voltage is further stepped down to an intermediate voltage of 12V by an isolated Intermediate Bus Converter (IBC). This voltage is further stepped down to the required low voltage using PoL.

The Distributed-Power Open Standards Alliance (DOSA) defines the specifications for the single output Quarter Brick DC/DC Converter. In the IBA, power converters are modular in construction and parasitics are minimized. In this configuration the front end converter is independent of load requirements.

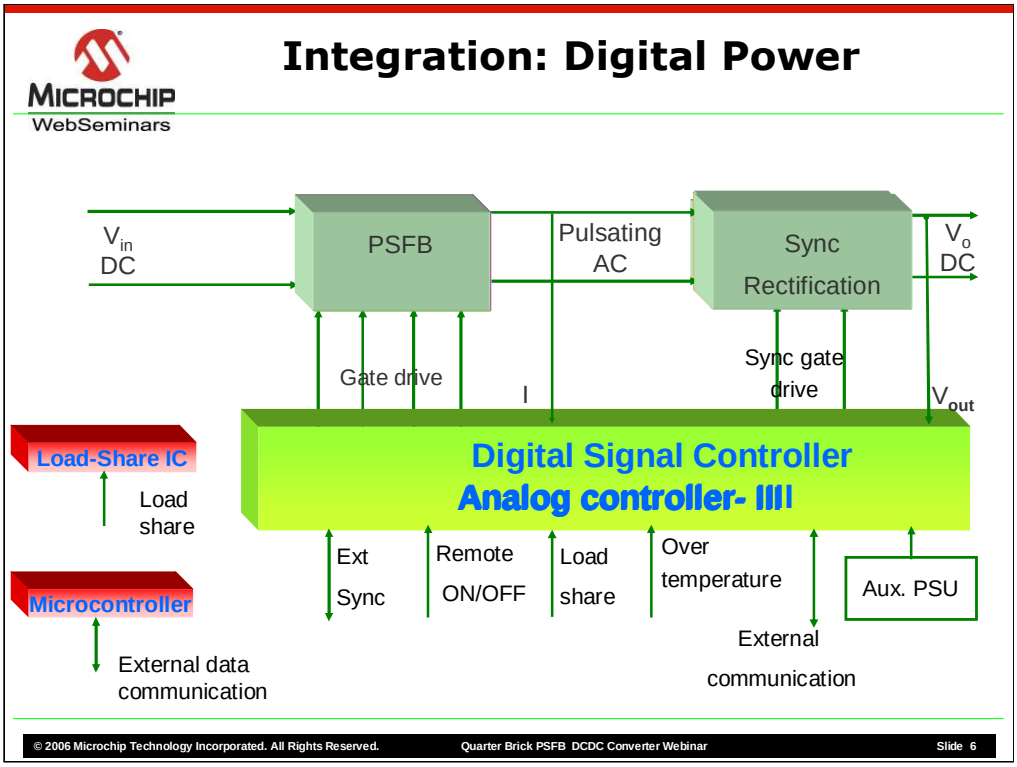



Intermediate Bus Converter provides Improved Dynamic response, Highest Packaging density, improved Converter efficiency, Galvanic Isolation near the load end, Output voltage ripple below the required limit. The trend towards lower operating voltages, higher current and wattage demands high density DC-DC power converters.




The intermediate Bus Converter operates from an input DC voltage of 36V to 76V with a rated output power of 200W at 12Vdc output voltage. This design achieves an efficiency of close to 94% with industry standard Quarter Brick dimensions.

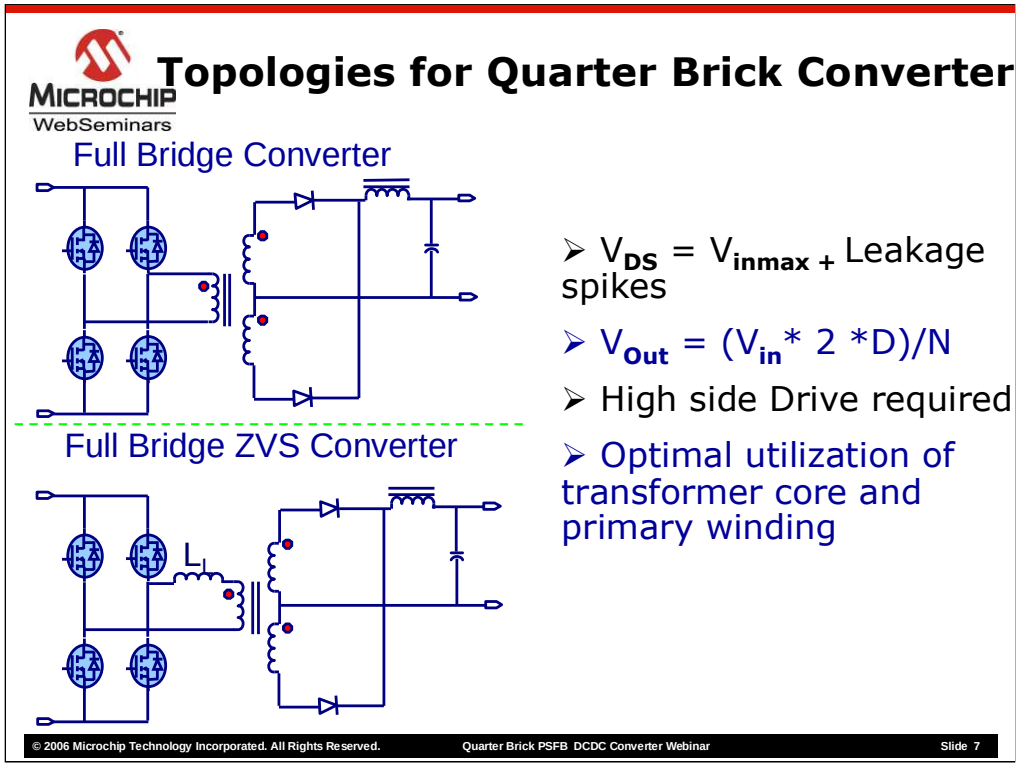
This converter also provides single wire load sharing, Output Over Voltage protection, Input under / Over voltage protections, Over temperature, Over current protection, Remote ON/OFF and galvanic isolation between input and output of the converter. This converter also features external Synchronization and external communication.



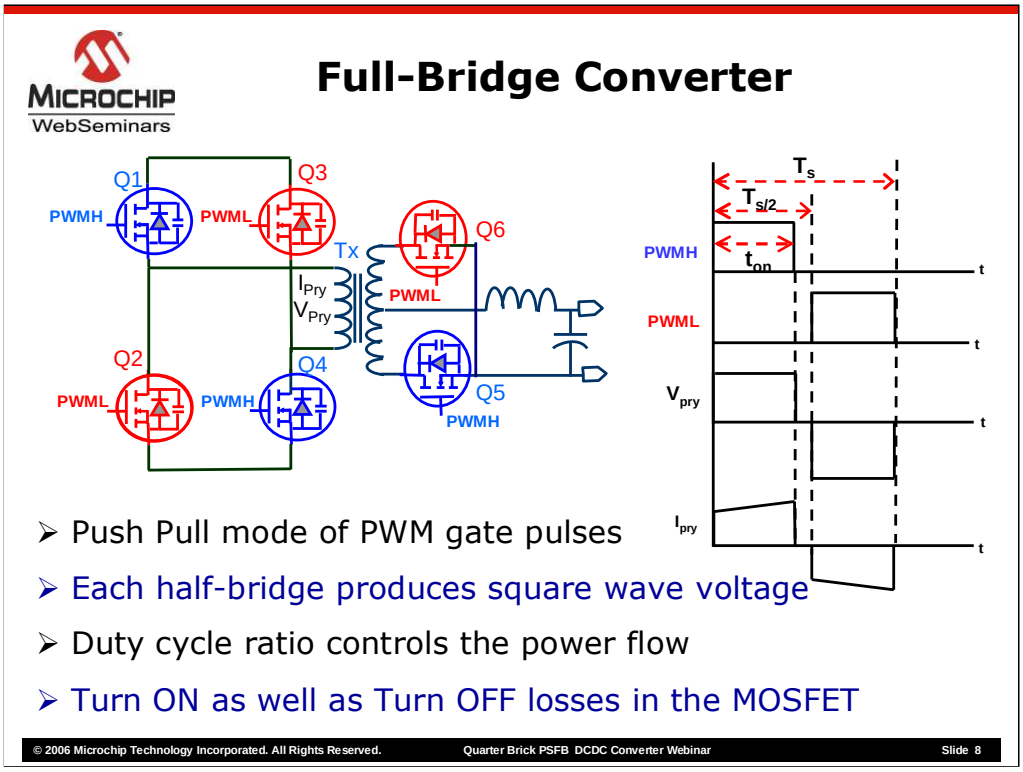

Numerous topologies can be selected based on the end product design specifications. However, suitable analog controllers should be selected based on the choice of topology.

A load share controller and a microcontroller should be chosen additionally to support load sharing and external communication respectively.

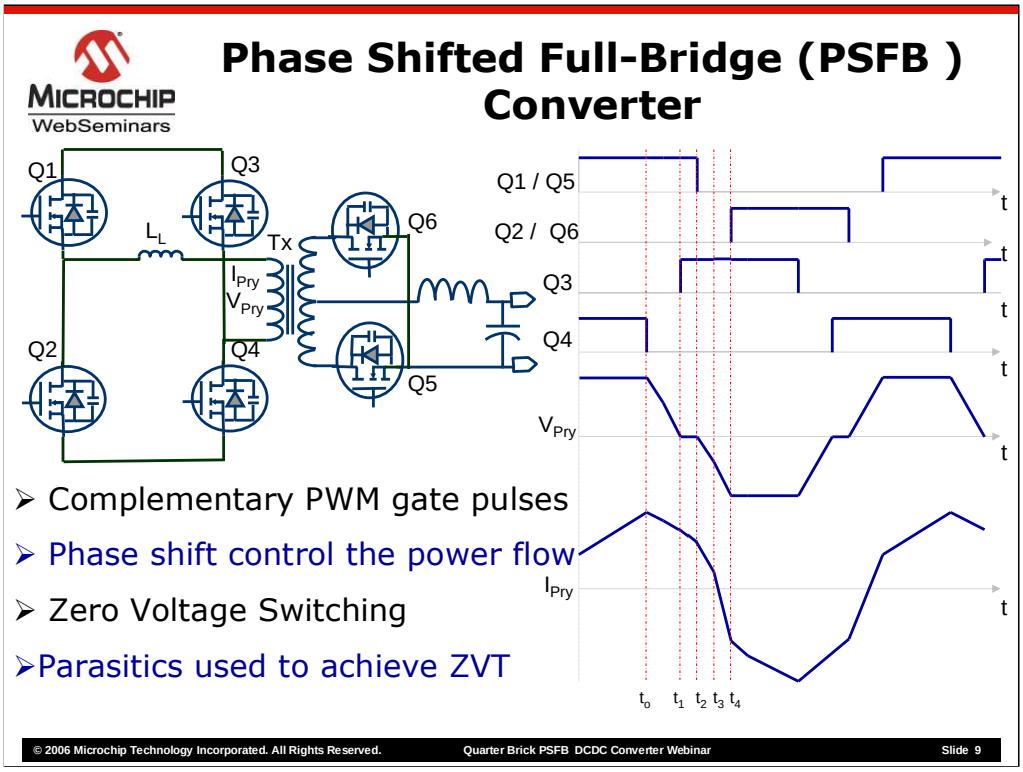
A digital Signal Controller (DSC) supports all the prominent Switched Mode Power Converter topologies and also supports external communication and load sharing between similarly designed converters.



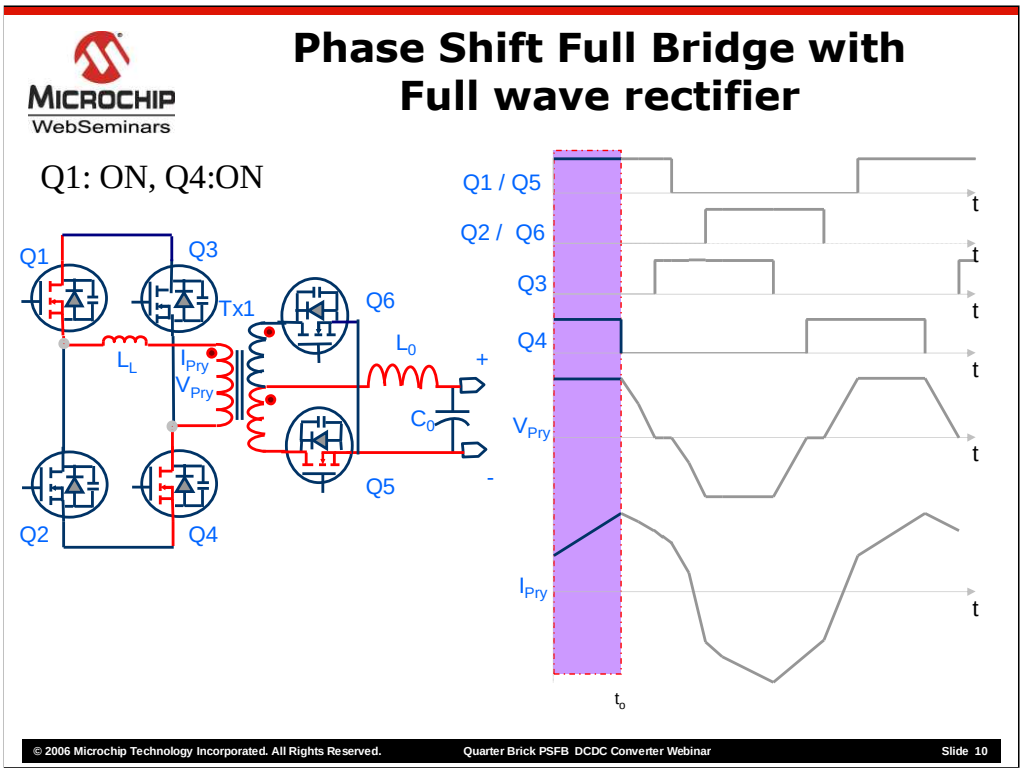

A simple full bridge or a Phase Shifted Full Bridge topology may be a good option to design a Quarter Brick DC-DC converter. In both these designs the transformer core will be used optimally and the primary MOSFET's will see only the input voltage plus leakage spikes. Driving the full bridge MOSFET's requires either a suitable High side / Low side driver or low side drive with an isolated gate drive transformer.



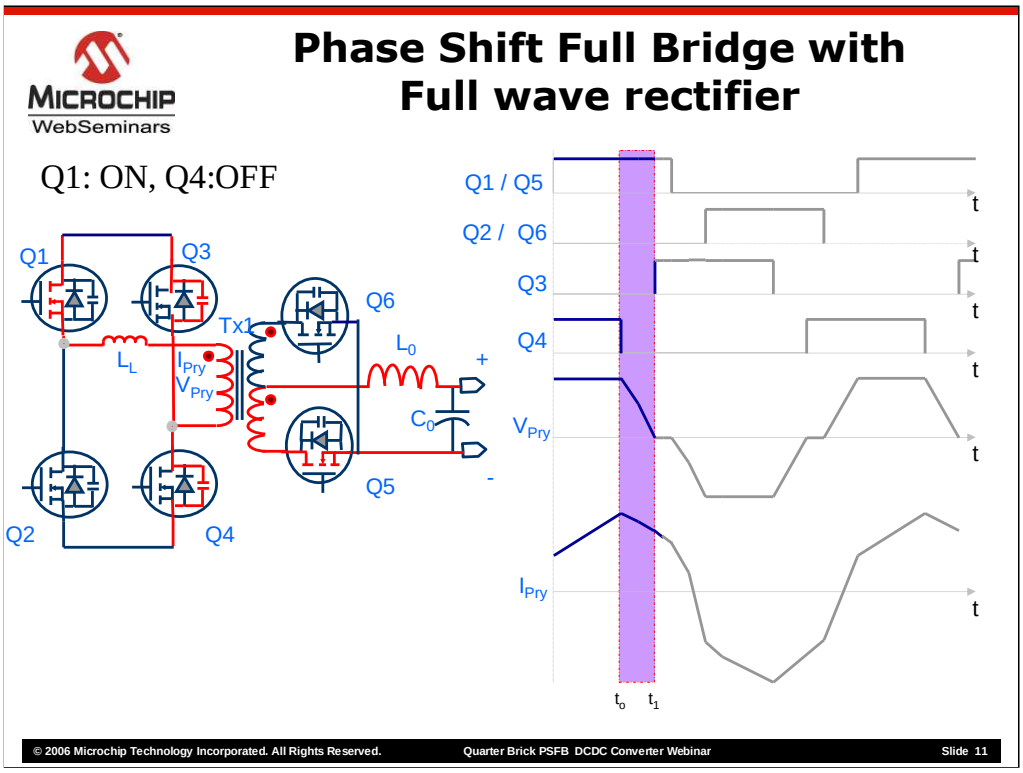

The full bridge converter can be configured for Push Pull configuration to drive the MOSFET's. The power will be transferred from primary to secondary when the diagonally opposite MOSFET's (Q1, Q4 and Q2, Q3) are turned ON. Output voltage regulation and power flow will be controlled by adjusting the duty cycle of the MOSFET's. In the simple full bridge topology MOSFET's will see both Turn ON and Turn OFF losses.



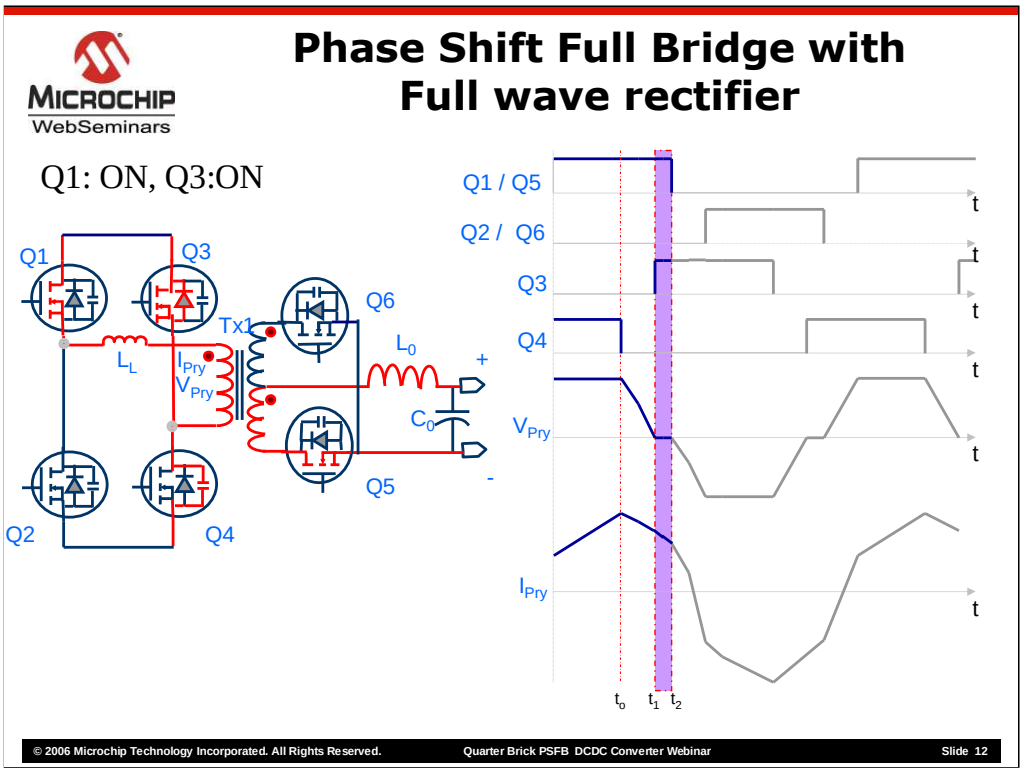

The Phase Shifted Full Bridge converter can be configured in complementary PWM mode to drive the same leg MOSFET's. Power will be transferred from primary to secondary when the diagonally opposite MOSFET's (Q1, Q4 and Q2, Q3) are turned ON. Output voltage regulation and power flow will be controlled by adjusting the Phase between the MOSFET's. In the Phase Shifted Full Bridge topology, MOSFET's will see the Turn OFF losses. In the next few slides we will see the operation of Zero Voltage Transition.



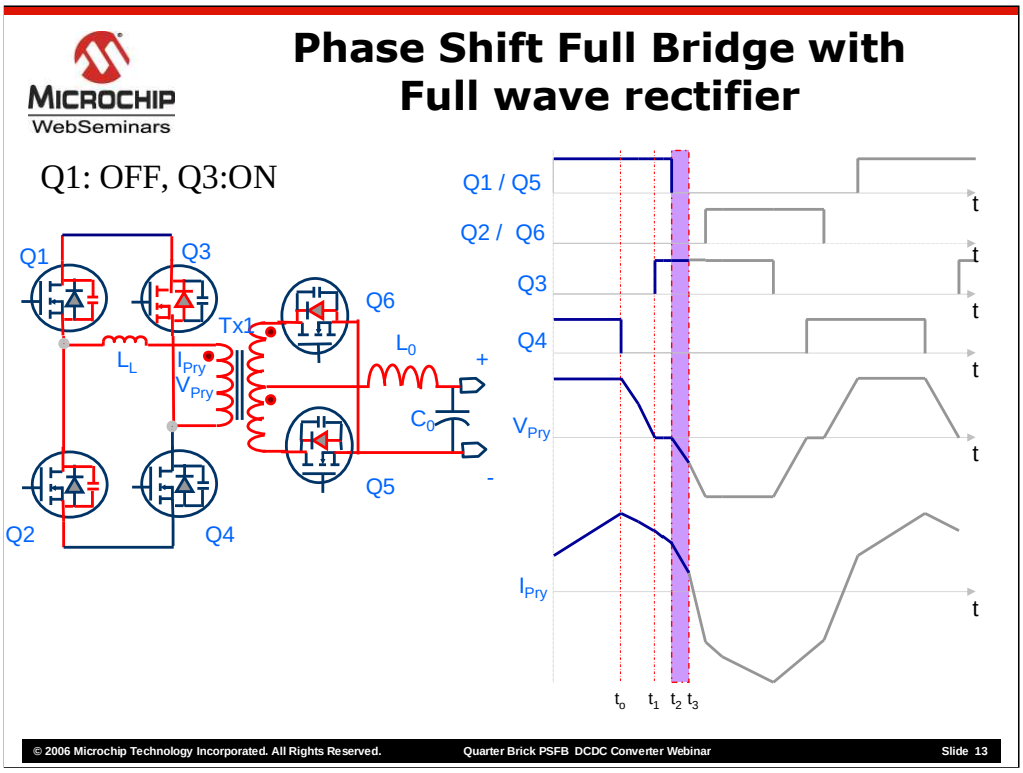

In this slide we see the diagonal switches Q1 and Q4 are conducting and power is delivered from primary to secondary of the transformer Tx1.



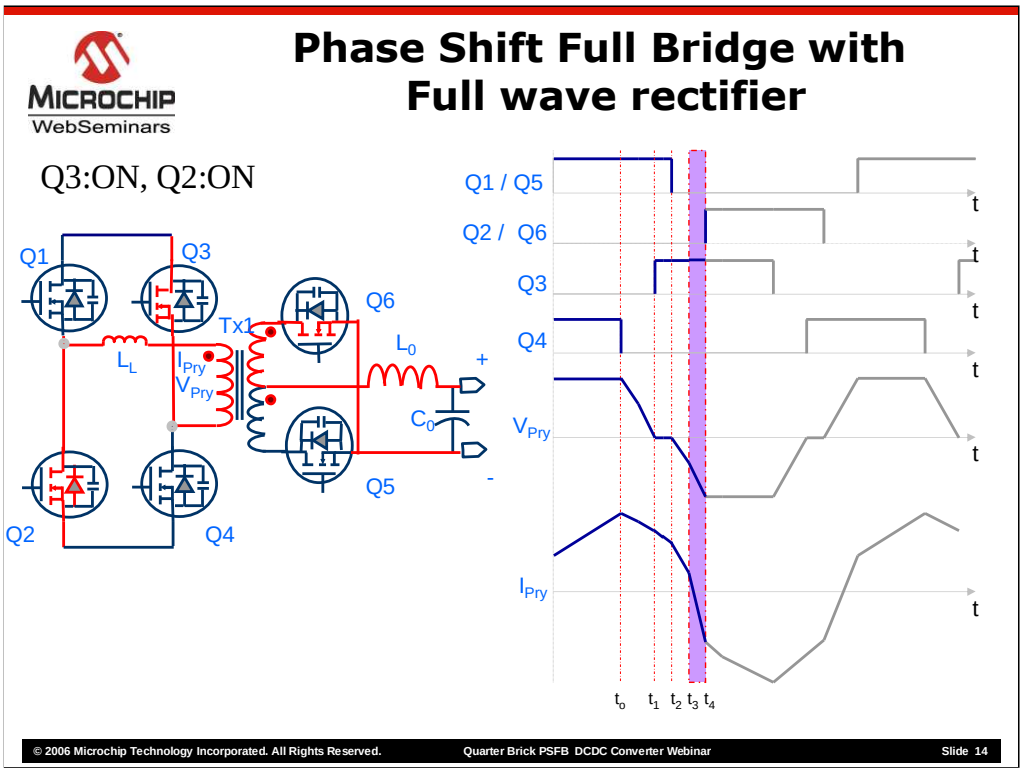

At $t_0$ MOSFET Q4 gate drive is turned OFF by the control circuitry which begins the resonant transition of the right hand leg of the converter. With MOSFET Q4 turned OFF, the primary current $I_{pry}$ continue to flow using the MOSFET Q4 output capacitance Coss and will provide the path. MOSFET Q4 output capacitance will be charged effectively from zero volts to the converter input voltage. At the same time MOSFET Q3 output capacitance and transformer Tx1 capacitance will be discharged since its source voltage raises to a higher voltage. This phenomenon positions MOSFET Q3 with no drain to source voltage before turning ON and facilitates Zero Voltage Transition.



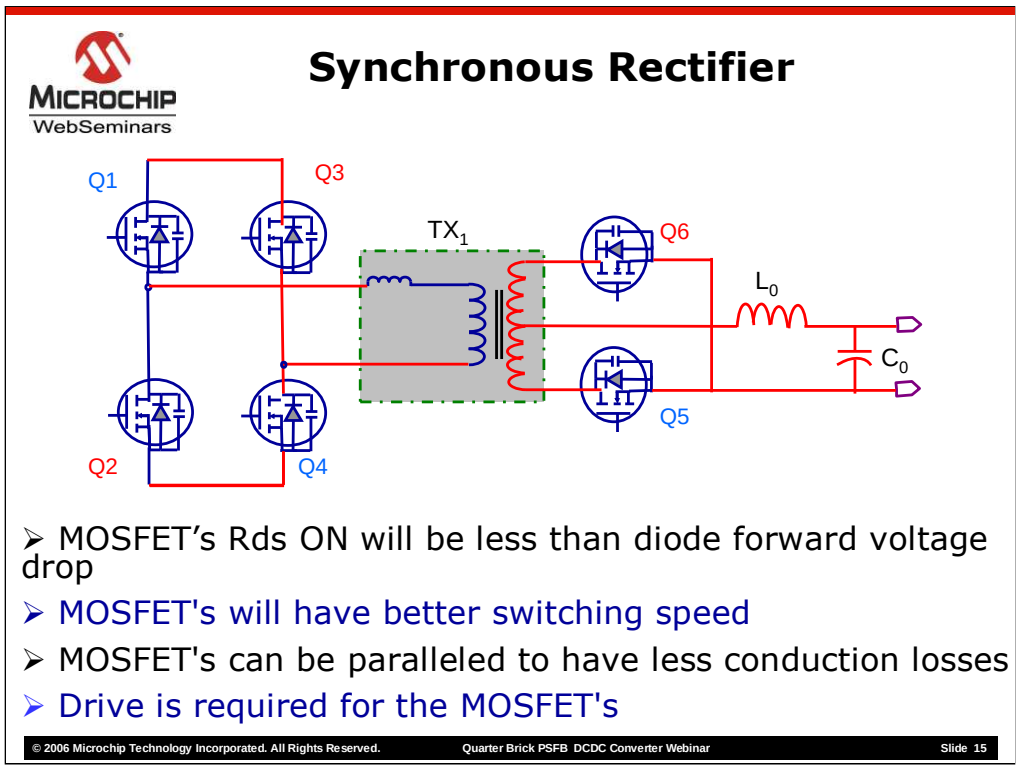

The primary current will be passing through MOSFET Q1 and the body diode of the MOSFET Q3. During this time MOSFET Q3 is turned ON and current takes the path of MOSFET Channel.




Now MOSFET Q1 is turned OFF and the primary current flow is through the MOSFET Q1's output capacitance. The current direction increases the drain to source voltage of MOSFET Q1 and decreases the drain to source voltage of the MOSFET Q2. This allows Zero Voltage transition for the MOSFET Q2.

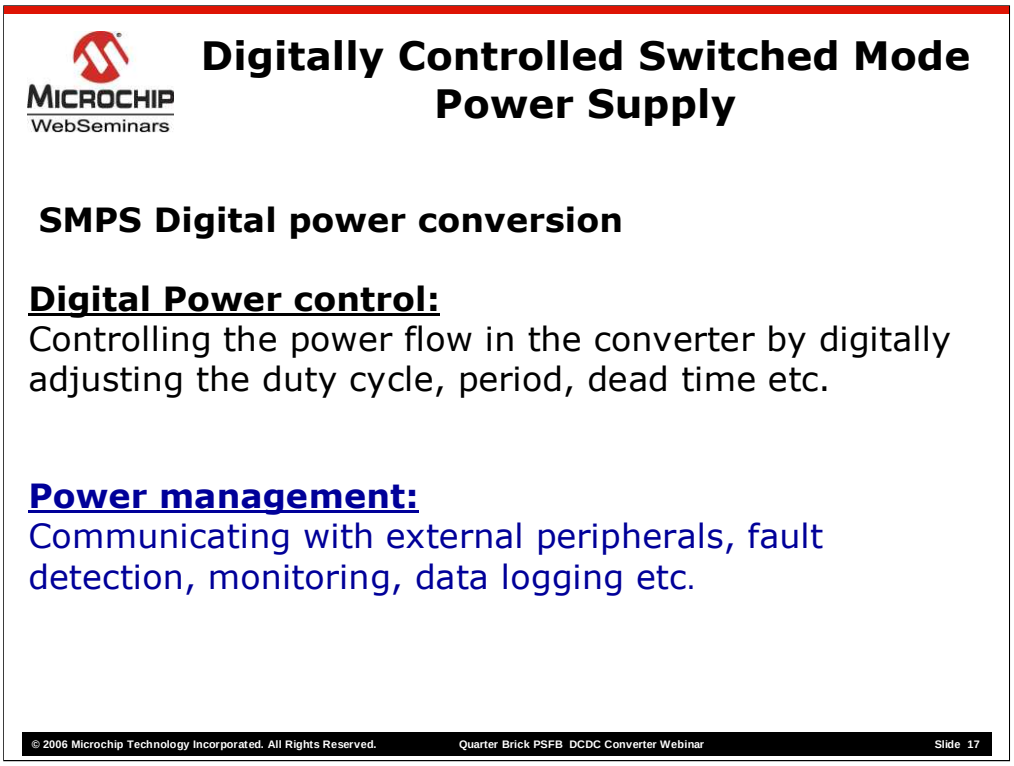



Once MOSFET Q2 is turned ON, again the power will be transferred from primary to secondary. Similar transition takes place in the left leg and this cycle repeats.

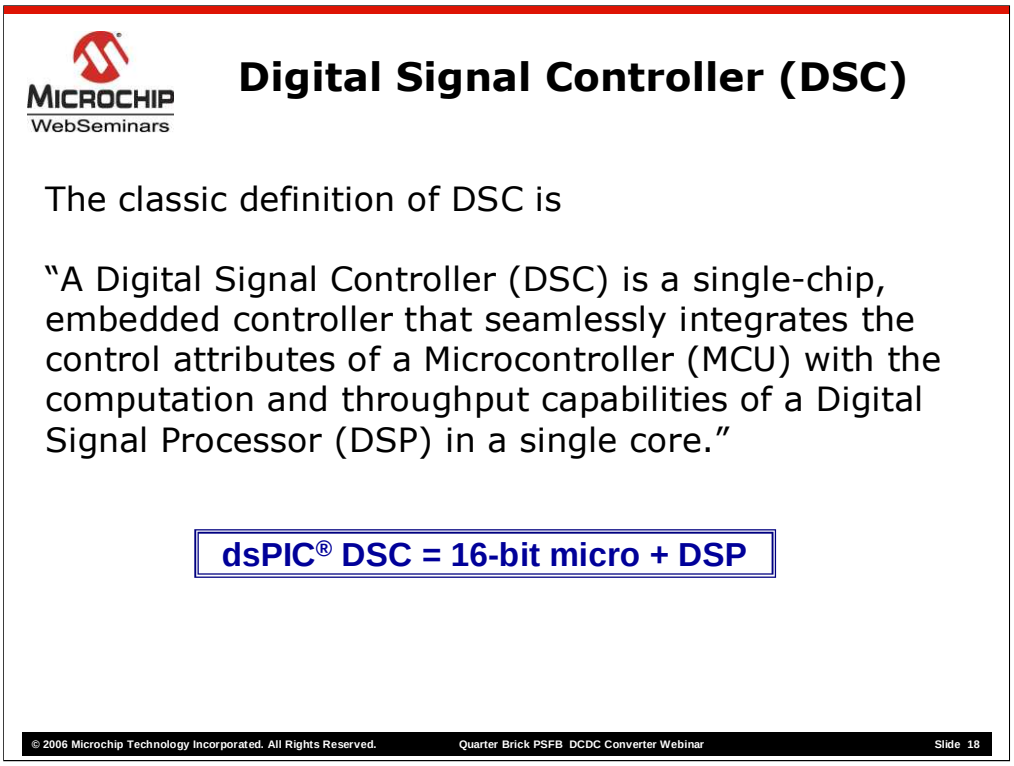



A mandatory design requirement to achieve high efficiency is to replace the secondary rectification diodes with Low RDS(ON) MOSFET's. The RDS(ON) losses and Switching losses of the Synchronous MOSFET's will be less compared to the forward diode losses of the secondary rectifiers. An additional gate drive circuit is required to control the Synchronous MOSFET's.

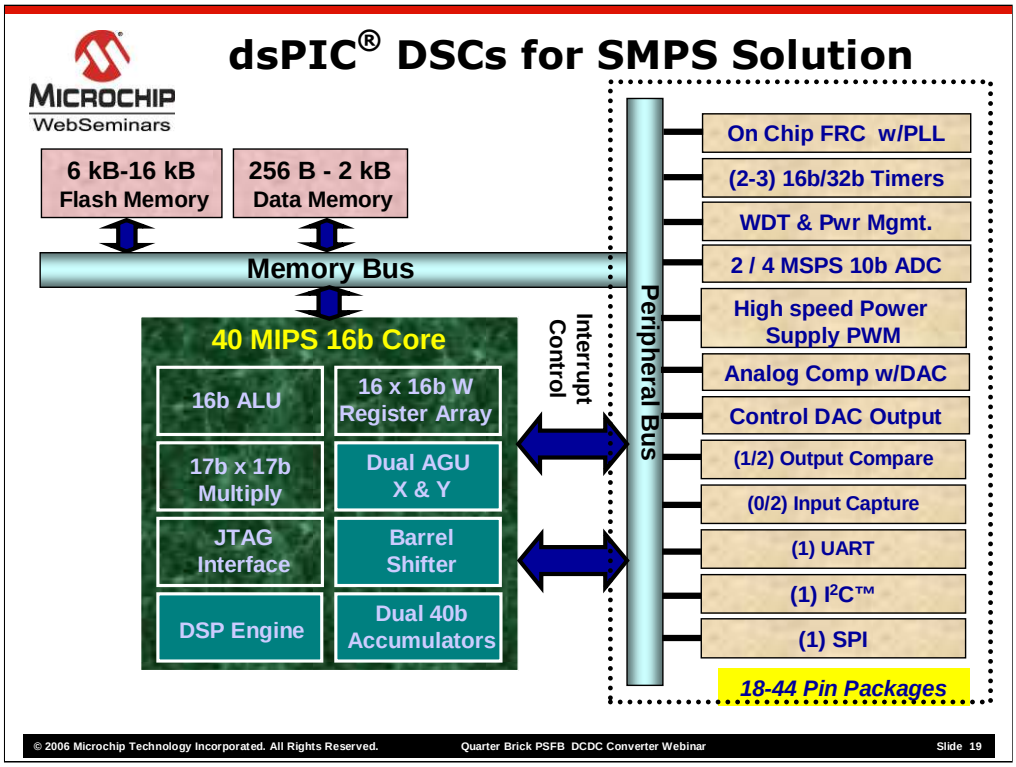

Now we will move into the design considerations for the 200W Digital Quarter Brick converter Design.



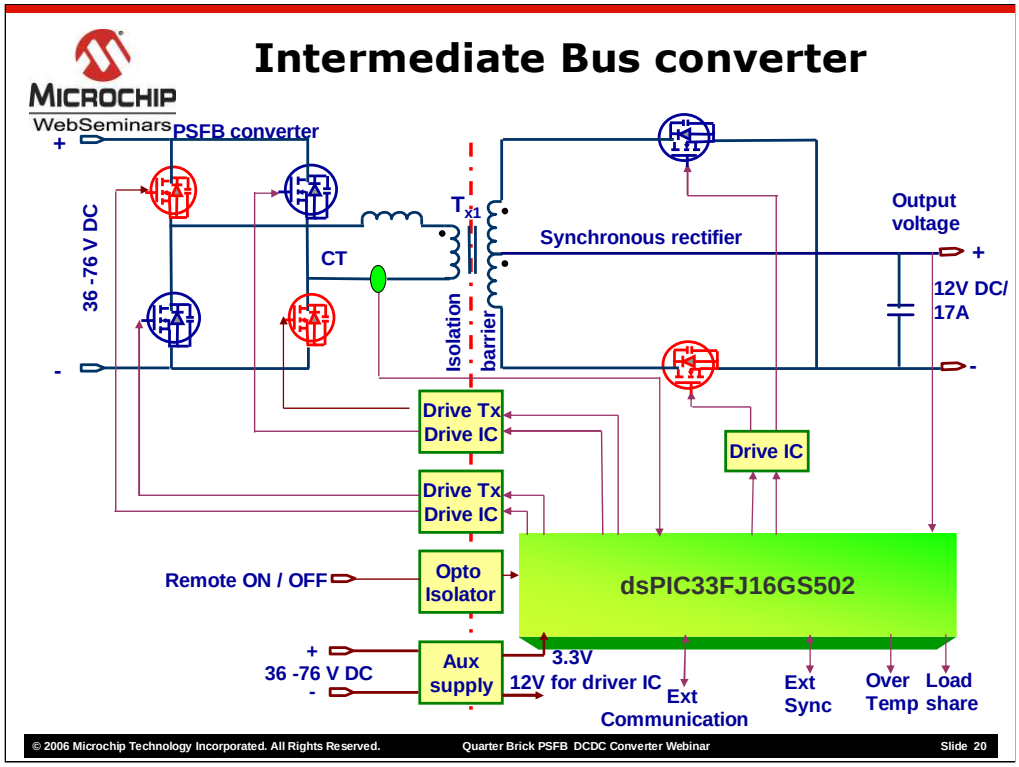

Converting the power flow in a Switched Mode Power Supply using a Digital Signal Controller is relatively a new trend in power conversion applications compared to power management. In the Digital Switched Mode Power Converter designs, the power flow in the converter is adjusted digitally and also external communication fault detection and data logging can be done with one Digital Signal Controller (DSC).




Digital Signal Controller (DSC) is a combination of a 16 bit micro controller with Digital Signal Processor. DSC seamlessly integrate the control attributes of a Microcontroller (MCU) with the computation and throughput capabilities of a Digital Signal Processor (DSP) in a single core."

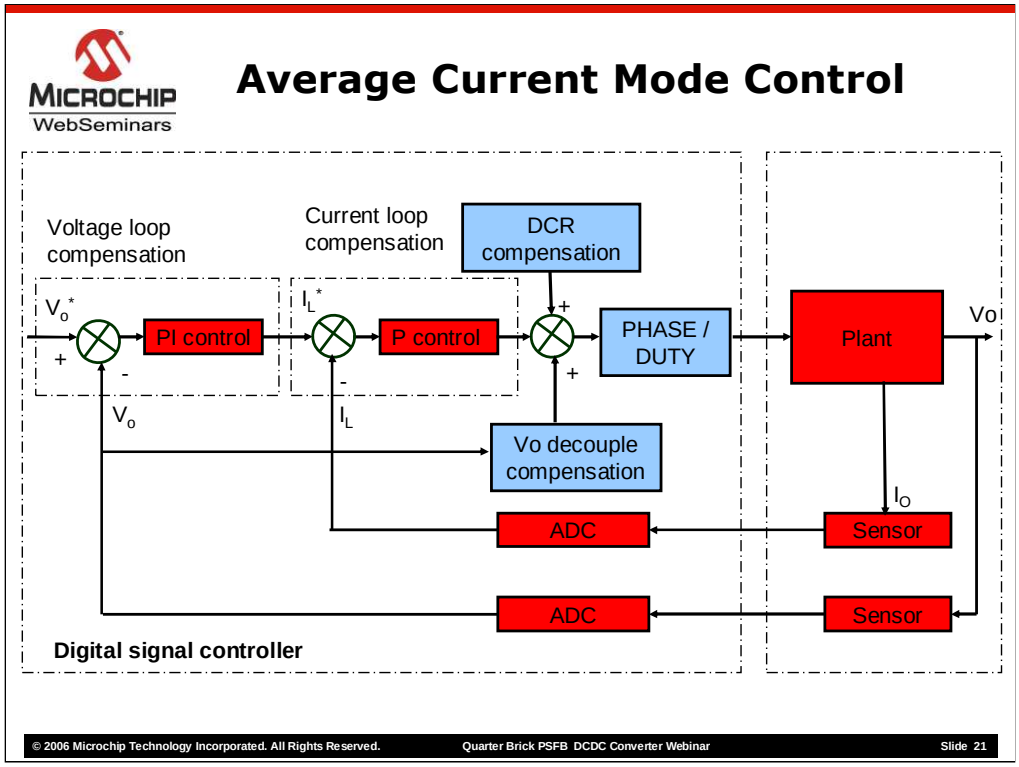



A typical dsPIC33F “GS” family of devices will have an on Chip FRC, program memory (ROM), data memory (RAM), DSP engine, Arithmetic logic Unit, 16x16 bit working registers, 16 Bit, 32 Bit timers, communication peripherals like, UART, I2C, SPI. The dsPIC33F “GS” family of SMPS devices include peripherals critical to power conversion like Pulse width modulators, Analog to Digital Converters, Analog comparators. “GS” family of SMPS devices are available in various pin count and packaging.




Here is the high level block diagram of the Phase Shifted Full Bridge converter on the primary side and Full Wave Center Tapped synchronous rectifier on the secondary side.

A single dsPIC33FJ16GS502 Digital Signal Controller is used in this application that controls primary and secondary MOSFET's, power management, fault management, external communications and load sharing.



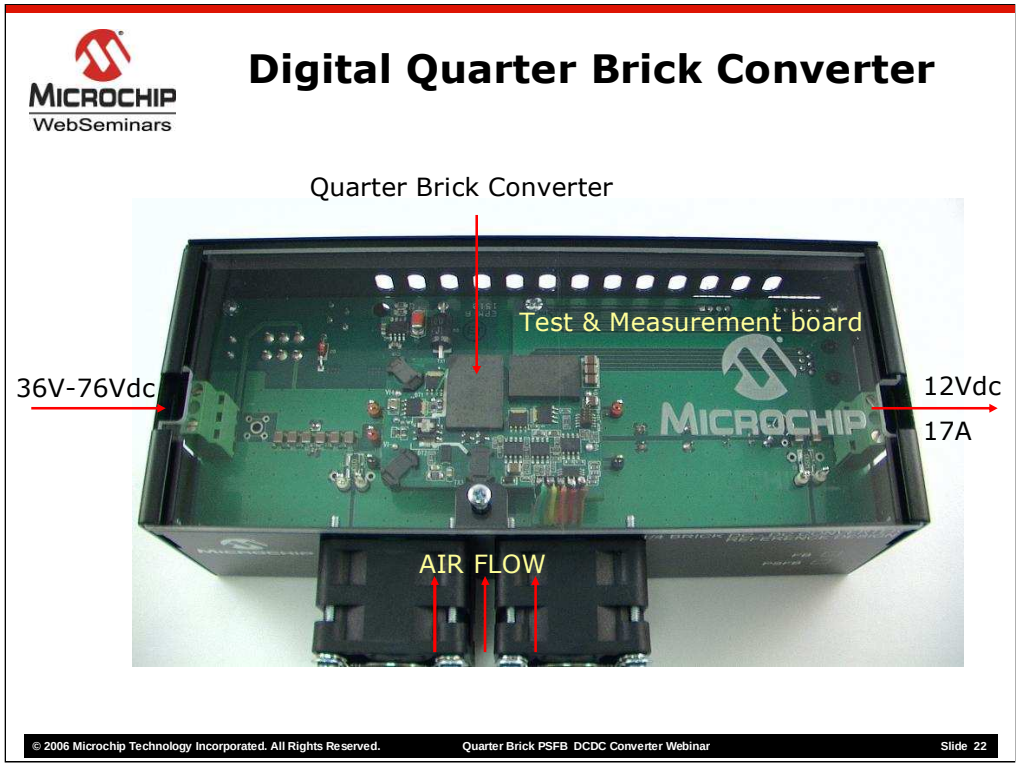

The Average Current Mode Control (CMC) strategy consists of two control loops. The inner current loop subtracts a scaled version of the inductor current $I_L$ from the current reference $I_L$*. The current error is further processed with the P compensator and the result is appropriately converted into duty or phase.

Any dynamic changes in the output load current directly modifies the duty or phase of the converter. The outer loop subtracts the scaled output voltage Vo from a reference Vo* and the error is processed using the PI compensator. The output of the compensator provides the current reference $I_L$* for the inner loop.

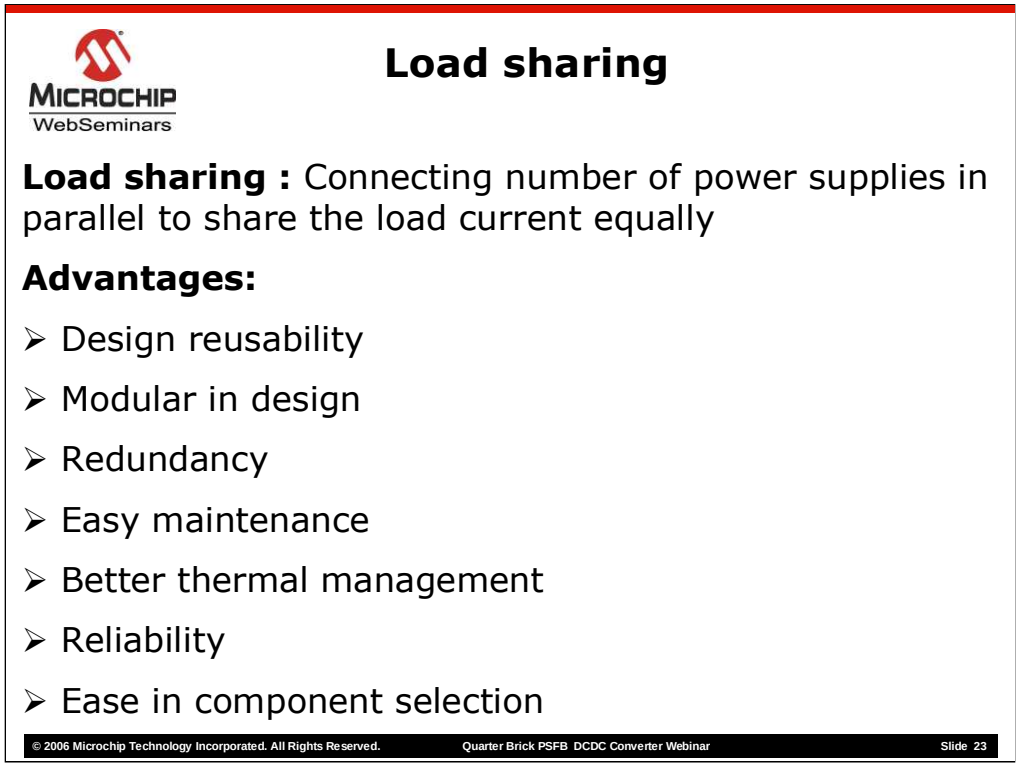
Current and voltage compensators allow tuning of the inner and outer loops to ensure converter stability and to achieve the desired transient response.

Voltage decouple compensation improves the dynamic performance and makes the design of control system easier. PI +P output performs only small changes to correct the load and line variations and most of the variation in duty/phase is contributed by Voltage decouple term.

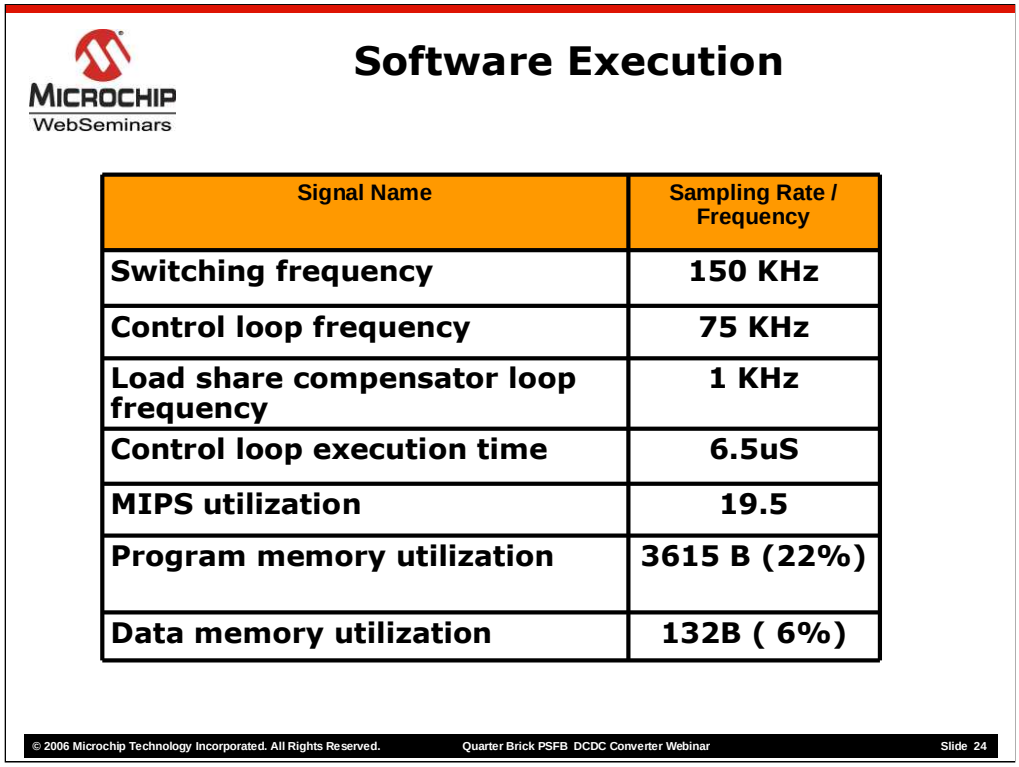
The voltage drops along the PCB traces and resistance in the windings of the magnetics are compensated with DCR compensation to make the system to function in linear manner.




The digital Quarter Brick Converter is mounted on the base board for test and measurement purpose. The base board facilitates to measure input power, output power, output voltage ripple, transient response , remote ON/OFF functionalities.



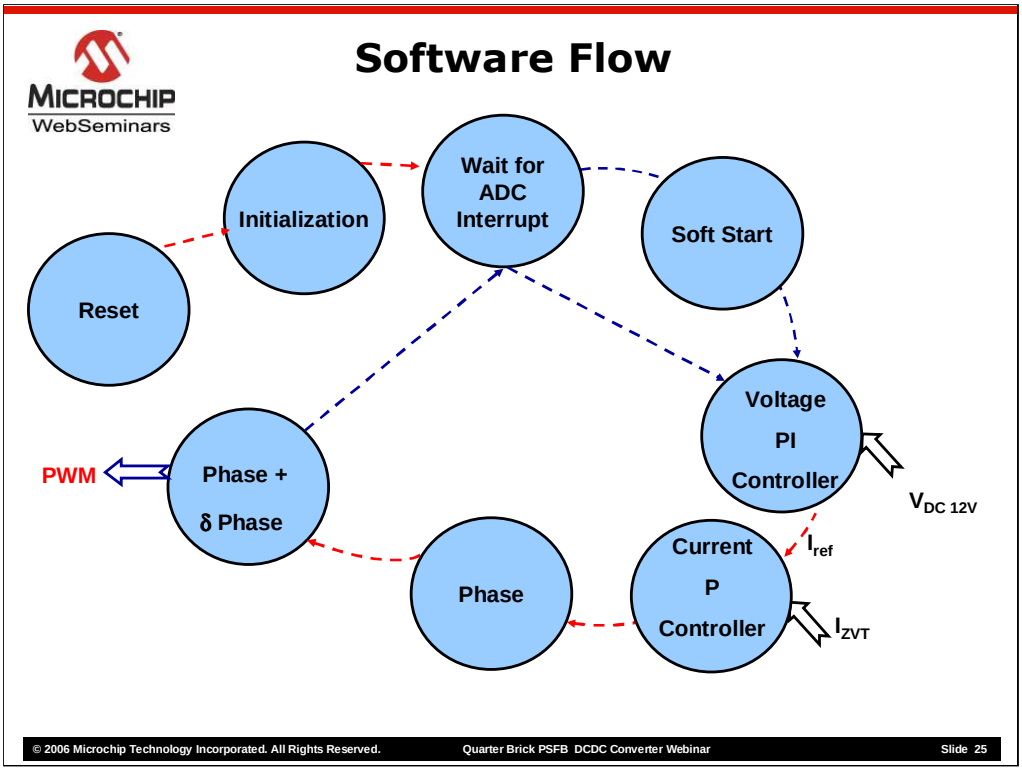

Ever increasing power supply densities for critical applications, calls for modular power supplies with greater reliability. This requires paralleling of power supplies to share the load current equally, which equalizes the stress and also allows easy maintenance, better thermal management, avoids redundancy, permits standardization of converter ratings, and minimizes component ratings. However, due to limited component tolerances and position of converters, individual power supply load currents might be notably different. Therefore, special provisions are usually necessary to balance the load current equally among the parallel modules.




These are the few critical frequencies, throughput and memory utilization of the dsPIC 33FJ16GS502.

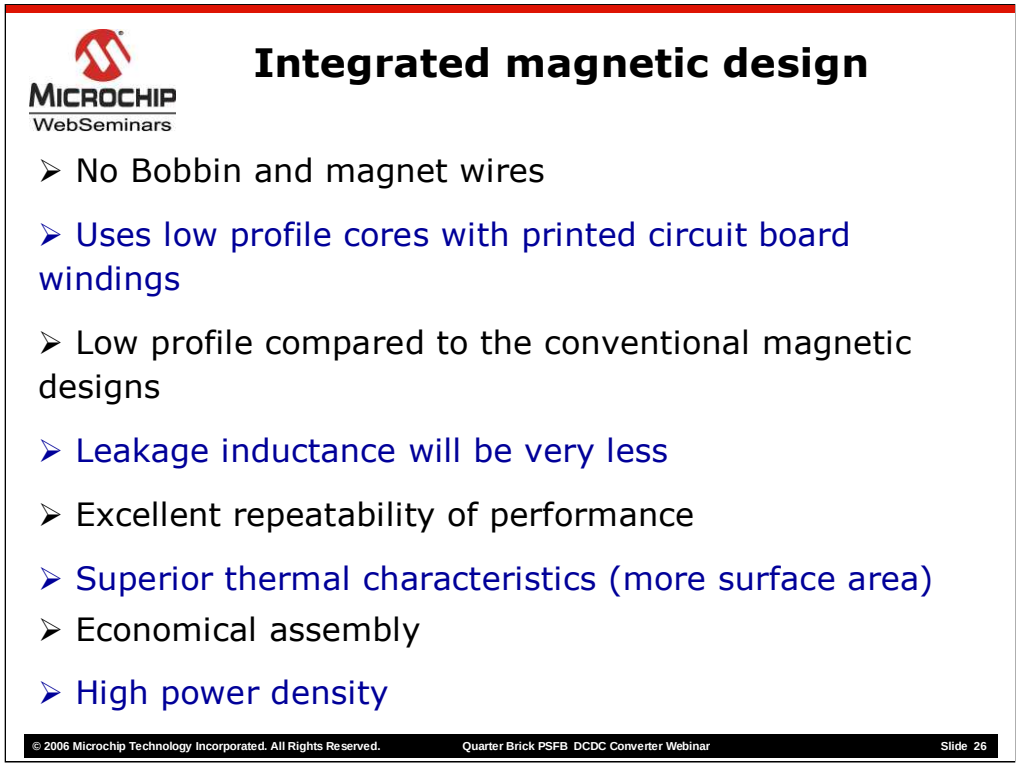
The switching frequency of the converter is 150KHz, control loop frequency (outer voltage PI compensator and inner current P compensator) is 75KHz and the load share compensator loop frequency is 1KHz. With this the total control loop execution time will be 6.5uSec.

The Total MIPS utilization is 50% of the device throughput. The program memory utilization is 22% and the data memory utilization is 6%.




In the Digitally controlled power converter SW execution will start with the reset and initialization sequences. Once the ADC interrupt is recognized, the process of controlling the Power converter begins by executing the compensator routines.

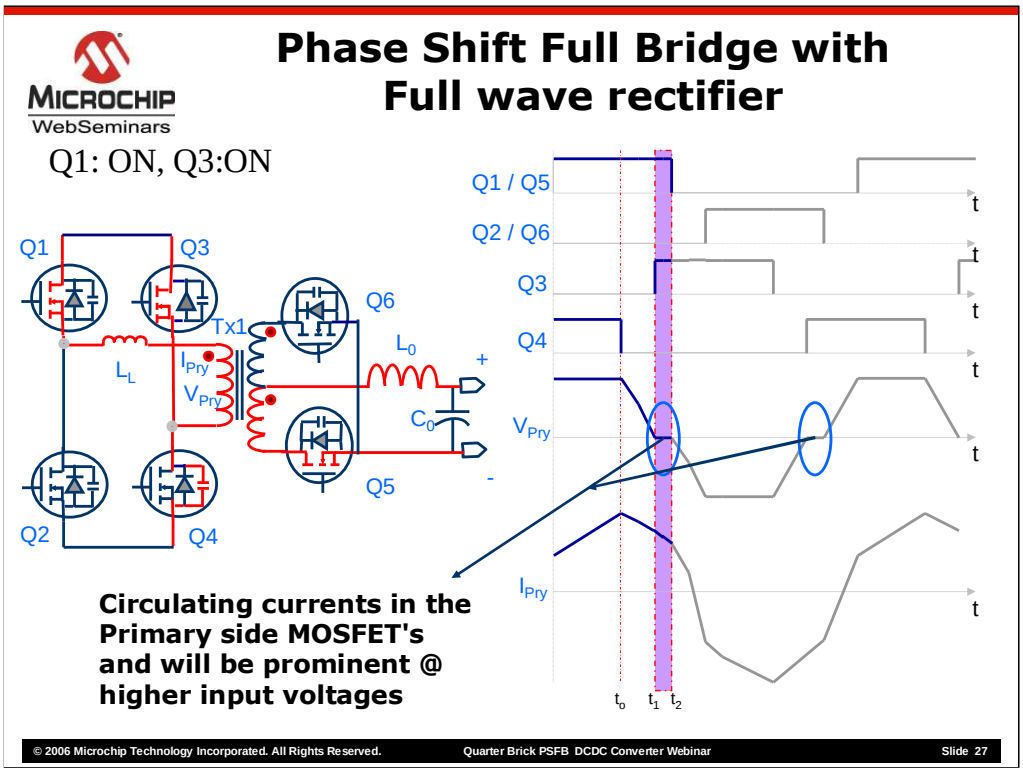
In this process it will provide soft start and provides the equivalent digital output voltage & current signals for the compensator loop.



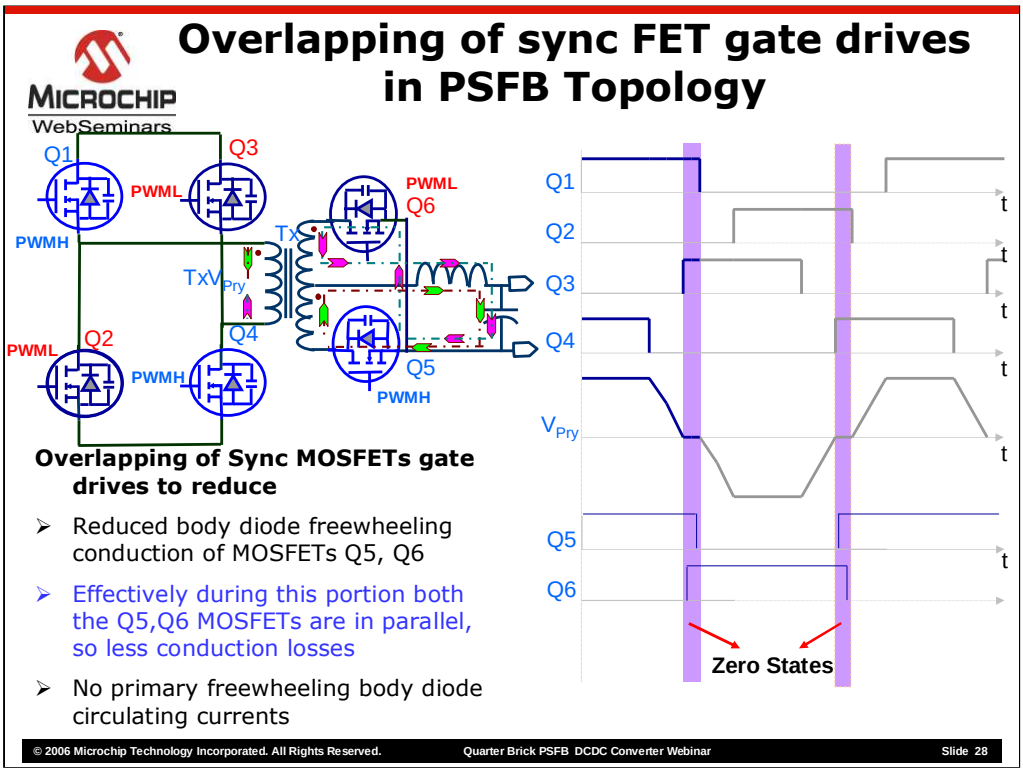

Planar magnetics is becoming popular in the high density power supply designs where the winding height is the thickness of the PCB. Planar magnetics' design can be constructed as a stand-alone stacked layer design or as a small multi-layer PCB or integrated into a multi-layer board of the power supply.

The advantages of planar magnetics are:

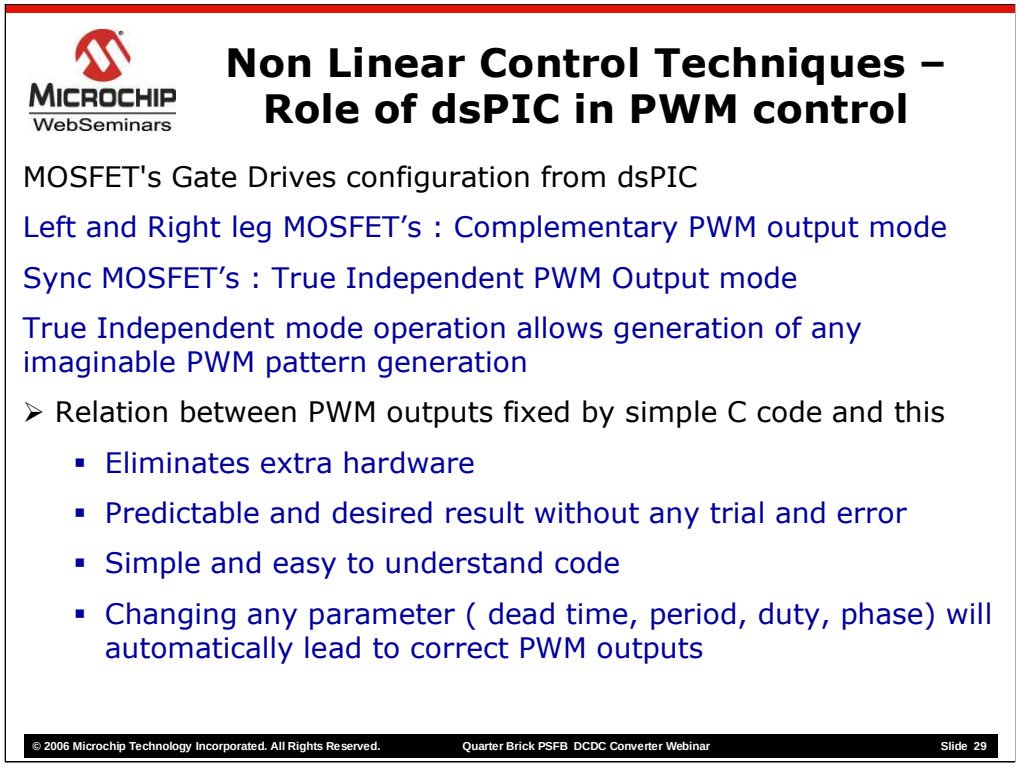
- Low leakage inductance
- Very low profile
- Excellent repeatability of performance
- Economical assembly
- Mechanical integrity
- Superior thermal characteristics



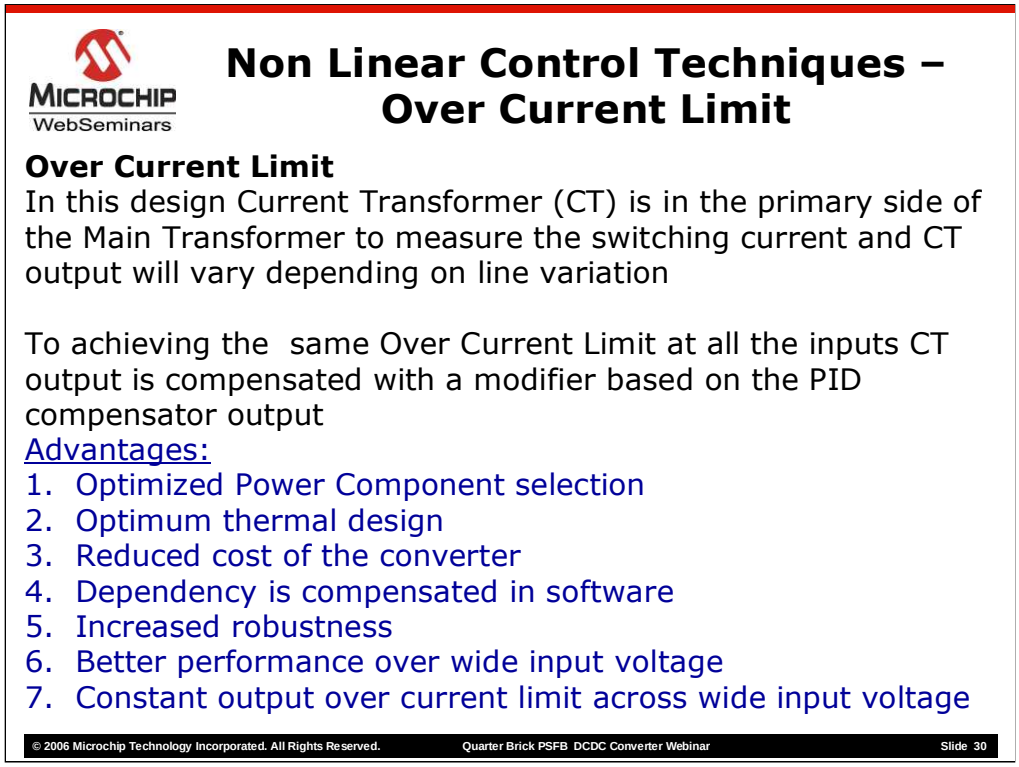

In the traditional method of controlling the synchronous MOSFET's, during the right hand leg transition a necessary condition is both the MOSFET's Q1 and Q2 will be ON. There is no power transfer from primary to secondary and the MOSFET Q5 is still ON . The energy in the output Inductor Lo is circulating through MOSFET Q5 and the Transformer Tx1 coil. This operation causes circulating currents in the primary side MOSFET's body diodes, which causes losses. These circulating current losses can be minimized by Over lapping the Synchronous MOSFET's gate drives and is discussed in the next slide..




In this method, synchronous MOSFET's gate drives are overlapped when there is no power transfer from primary to secondary of the transformer. This ensures reduced body diode freewheeling conduction of MOSFET's Q5, Q6. This ensures less conduction losses since both the MOSFET’s Q5 and Q6 are effectively in parallel.The primary freewheeling body diode circulating currents are absent.




In the Phase Shift Full Bridge configuration Left and right leg MOSFETs are configured in the complimentary mode and secondary synchronous MOSFETs are configured in True Independent mode. Any imaginable PWM output can be generated using the True independent mode. This flexible configuration can be done in the Software and eliminates need for extra hardware. Desired and predictable results can be achieved with out any error. Changing any PWM configuration parameters produces the desired PWM outputs.




Current Transformer (CT) in the primary side of the converter measures the switching current and this current will differ with the line voltage variation. Occurrence of over current my vary based on the line variations and is not desirable for efficient operation.

The set limit of over current at all the inputs can be achieved by modifying the measured current with a factor based on the input voltage.

This will optimize the components selection, thermal design and cost. This will also increase the system robustness and better performance over wide input voltage range.

## Non Linear Control Techniques – Output Voltage Rise / Fall times

**Output Voltage rise time:**
Desired output voltage rise time can set using the Software

Advantages:
1. Voltage and Current overshoots are controlled
2. Output voltage rise times control through SW

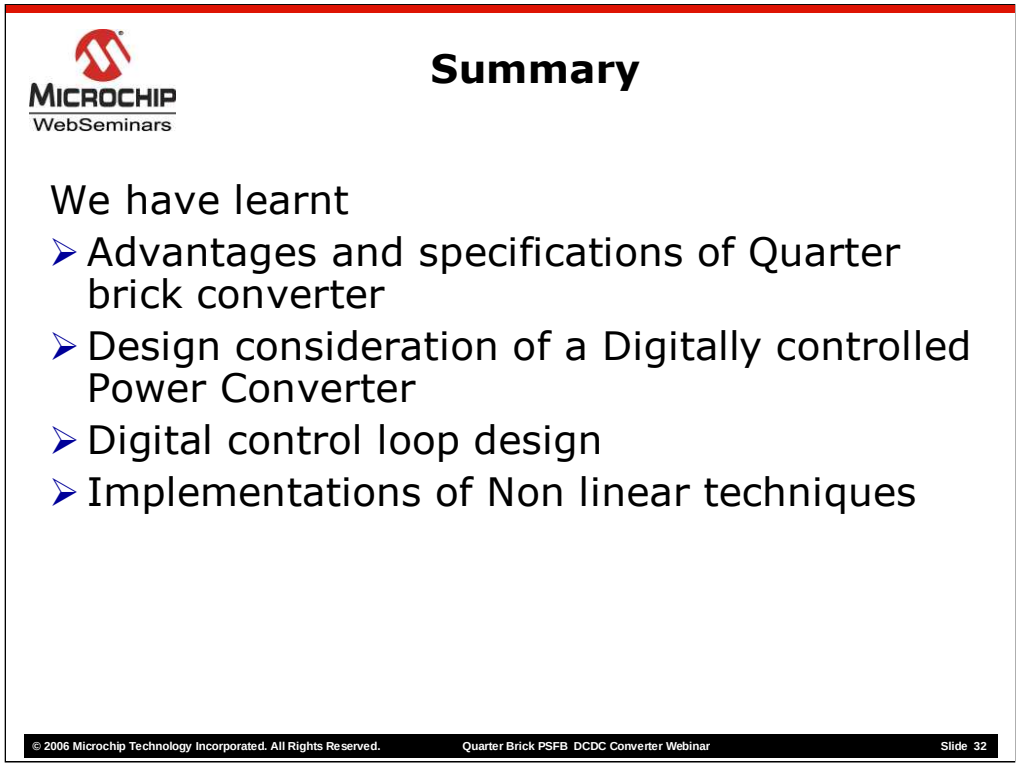
**Output Voltage fall time:**
To get the desired no load fall time when remote ON/OFF is deactivated the secondary synchronous MOSFET's will be turned OFF with delay compared to the primary MOSFET's.

Advantages:
1. Output voltage fall times control through SW
2. Improves on controllability, predictability and passive dynamics of system




Output voltage raise and fall times are also critical to meet the converter specifications. A programmable soft start can be incorporated in the software to limit the voltage / current overshoots and controlled output voltage rise times.

When the converter is operating on no load condition and Remote ON/OFF is enabled, the output capacitors will take a few seconds to discharge to 10% of the rated output voltage. The fall time can be reduced by turning OFF the synchronous MOSFET's with a specified delay compared to the primary MOSFET's.




In this web seminar we have discussed Advantages and specifications of Quarter Brick Converter, Design consideration of a Digitally controlled Power Converter, design of Digital compensator, advantages of single wire load sharing. In the end we have learnt implementations of Non linear techniques to get the higher system performance.


Thank you for joining with me in this Webinar on the Quarter Brick Phase Shifted Full Bridge DCDC Converter Reference Design using the dsPIC® DSC

Log on to www.microchip.com/smps for more design information.