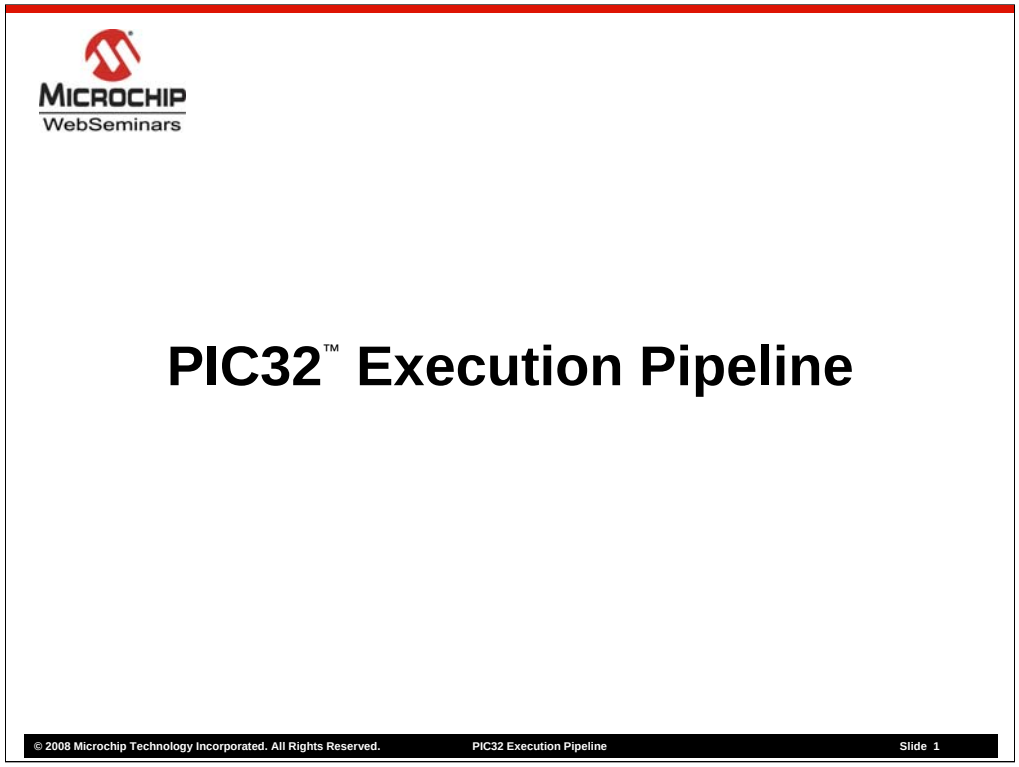
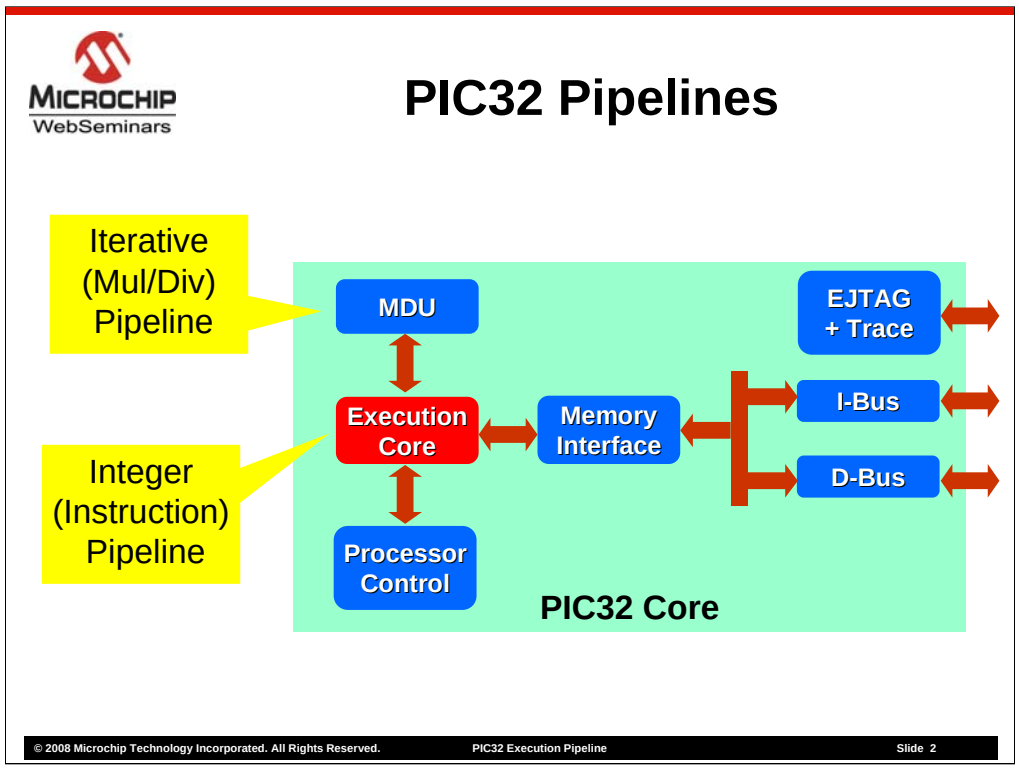


Hello and welcome to the PIC32 Execution Pipeline webinar.

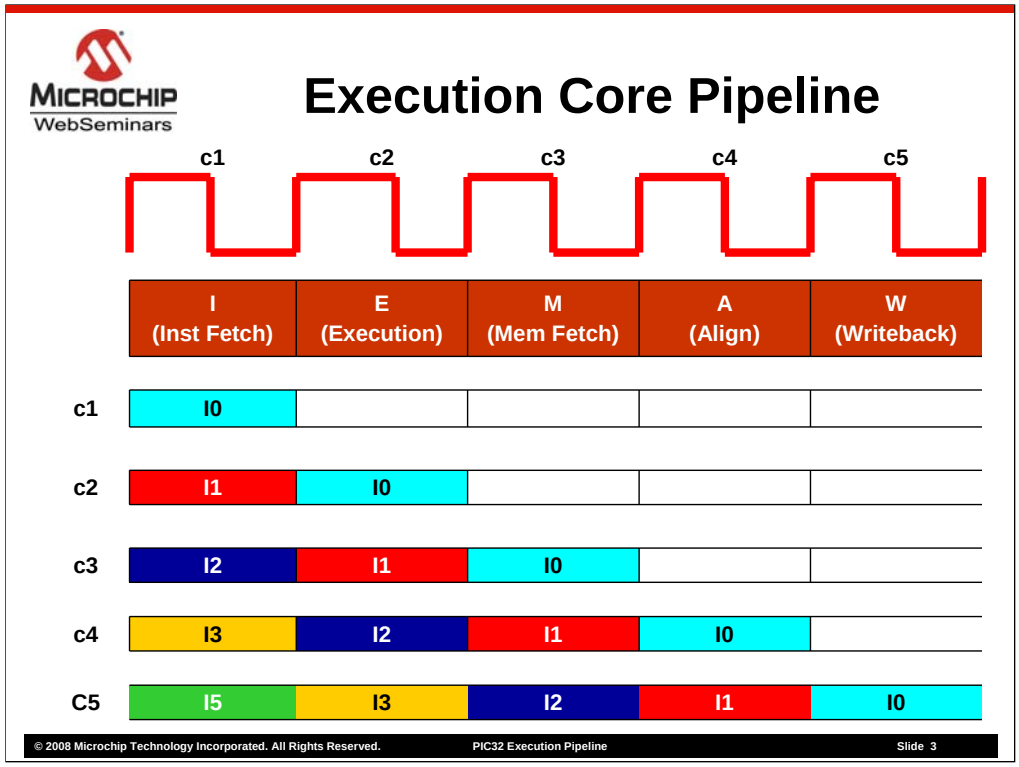
I am Nilesh Rajbharti, Applications Engineering Manager for PIC32 products.

In next few minutes, I will provide a quick overview of the PIC32 Execution Pipeline.

Let’s begin.



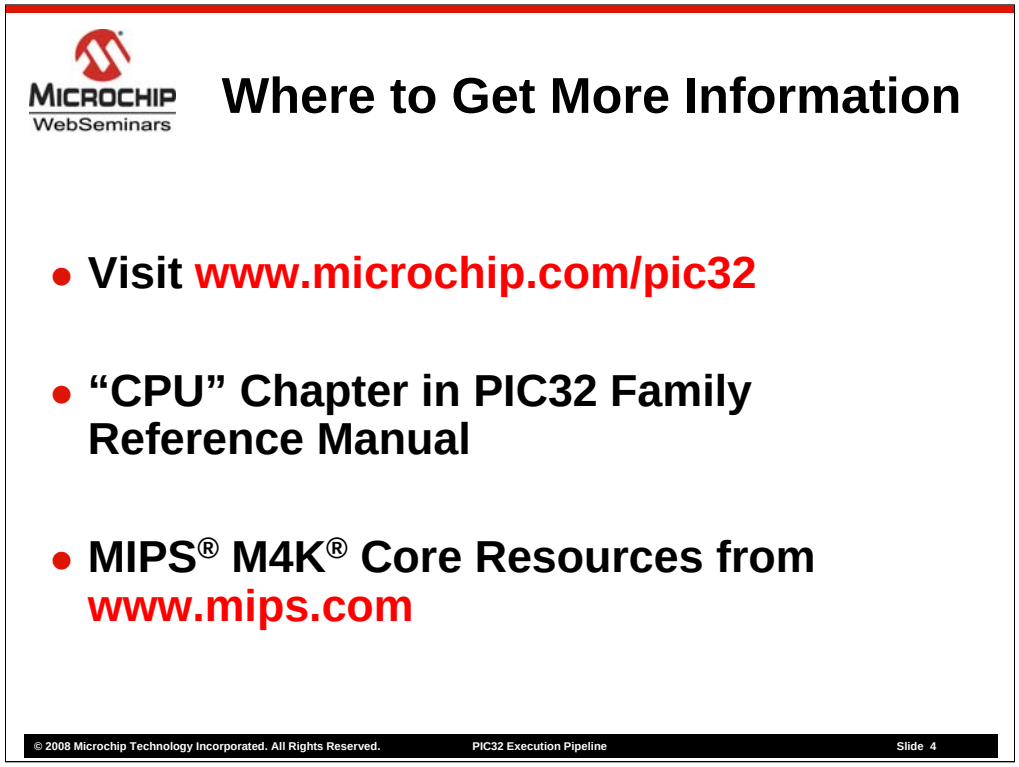
PIC32 core consists of two pipelines - An Integer Pipeline in the Execution Core and an Iterative pipeline in the Multiply Divide Unit. The Integer pipeline is a five stage pipeline to execute CPU instructions. While the Iterative pipeline is a multistage iterative pipeline to perform multiply and divide operations. In this presentation, I will focus on Integer pipeline only.



As I mentioned briefly in the previous slide, the PIC32 execution core employs 5-stage pipeline. This slide shows all of five stages and graphically describes how instructions proceed in the pipeline.

The five stages of the pipeline are 1) Instruction Fetch, 2) Execution, 3) Memory Fetch, 4) Memory Align, and 5) Memory Writeback. As the name suggests, in the Instruction fetch, an instruction is fetched. In stage E, the instruction is decoded and executed. In the M stage, memory operands are fetched from the on-chip memory – be it SRAM or Flash. In the A stage, the memory data is word aligned and in the W stage the result is written to the destination.

The bottom half of the slide illustrates how instructions proceed in the pipeline. Assume that ‘c1’ is the very first clock the CPU is executing. During ‘c1’ clock, an instruction ‘I0’ is fetched. During that clock, remaining four stages of the pipeline are empty. During ‘c2’ clock, the ‘I0’ instruction moves to ‘E’ stage and at the same time, next instruction ‘I1’ is fetched. The remaining three stages are still empty. During ‘c3’ clock, ‘I0’ and ‘I1’ move to ‘M’ and ‘E’ stage respectively, at the same time ‘I2’ is fetched. In ‘c4’, four stages of the pipeline are full. In ‘c5’ clock, all five stages are full. From now on, the pipeline will execute one instruction every clock cycle given that there are no stalls. You may learn about stalls and other details in a future webinar.



So, you now have a high level understanding of PIC32 Execution Pipeline scheme. To learn more, visit www.microchip.com/pic32. This site contains PIC32 Datasheet, Family Reference Manual and various other resources. For an abridged technical overview, see "CPU" chapter in PIC32 Family Reference Manual. If you want more detailed information, refer to www.mips.com and look for "MIPS® M4K® Core".

Thanks for your time.