Welcome to this Web seminar on Switch Mode Power Supply Topologies. In this webinar, we will analyze the Forward Converter. It is a transformer-isolated converter, based on the basic buck converter topology.
We will start with a brief description of the basic operation of the converter. We will then analyze the behaviour of the system in its various operating conditions, and we will derive the basic equations. We will then analyze how to determine and select the components to build such a converter.
This is the basic circuit of a forward converter.
The input to the circuit is a dc voltage (Vdc);
the output is again a dc voltage (Vout). The transformer allows implementation of the galvanic isolation between the primary and the secondary, that is between the input and output of the circuit. To transfer energy across the transformer barrier, the dc input voltage must be converted into an ac voltage and then back again to dc. The left side of the transformer has two windings:
Np is the primary winding,
which is basically responsible for the energy transfer and Nr, which is called reset winding and whose use will be explained in the following slides.
The right side of the transformer is named Ns, which is the secondary winding. Np, Nr and Ns are the number of turns in the transformers windings.
Diode D1 is used, with Nr, to create a path to discharge the energy stored into the transformer while the switch is open.
Q1 is a solid state switch operating at frequency Fpwm. This switch is normally driven by a pwm output from the smps dsPIC30F.
Diodes D2 and D3 rectify the secondary voltage; diode D3 is commonly called a freewheeling diode.
L and C implement a low pass filter which removes the high frequency components of voltage V2, letting only the dc component of V2 to appear at the output.

Switch Q1 is operated with a square wave signal. The ratio between the on and off period determine how much energy flows from the input to the output.

Therefore the desired output voltage can be obtained controlling the duty cycle of the pwm signal driving Q1.
Switch Q1 is operated as shown by the waveform. The command signal is a square wave with a duty cycle determined by the ratio $T_{ON}/T$. The output voltage, as we will see later, is proportional to this ratio. A very convenient way to generate such a signal is using the PWM peripheral in the SMPS dsPIC devices. Such components allow you to select a very wide range of values for the period $T$, that is for the PWM frequency.

Another important feature of the PWM peripherals on the SMPS dsPIC devices is the ability to fine tune the duty cycle. Since, as we have seen above, the output power is proportional to the duty ratio, this feature permits very fine trimming/regulation of the output voltage, which is often a required feature of converters.

As for the buck converter, we will follow the approach that is typical in the analysis of converters behavior. We look at the circuit voltage and current values only at steady state, when the transients have died out. Such an approach describes well the overall functionality of the system, meaning it is able to analytically describe the input/output relationship. Of course if we are interested in the behavior of the system during transients (when the input voltage or the output load change) such an approach is not enough. The best approach in these cases is to use software circuit simulation tools.
It is also worth remembering the equations that drive the behavior of a (ideal) transformer.

\[
\frac{V_S}{V_P} = \frac{N_S}{N_P} \\
\frac{I_S}{I_P} = \frac{N_P}{N_S}
\]
It is also worth remembering the equations that drive the behavior of a (ideal) transformer.
The ratio of the output voltage to the input voltage equals the ratio of the output to the input number of turns.
The ratio of the output current to the input current, instead, equals the input to the output turns ratio.

These two simple equations are basic in describing the behaviour of the transformer. They are not exact in the fact that they do not consider leakage and other phenomena, but in most cases they can be effectively used in the analysis of transformer circuits.
The analysis of the forward converter, because of the presence of the transformer, must be split, considering first what happens at the primary side and then the behaviour of the output circuit. This approach is therefore a little bit more complex than the case of a buck converter.

Moreover, we will see that, because of the specificity of the converter operation, time $T_{OFF}$ must be divided into two sub-intervals to get a full understanding of the circuit behavior.
Let’s analyze the primary circuit behavior during $T_{ON}$. 

Primary winding $N_P$ voltage:

$$V_{P,\text{on}} = V_{dc} - V_{Q,\text{on}}$$

Reset winding $N_R$ voltage:

$$V_R = \frac{N_R}{N_P} (V_{dc} - V_{Q,\text{on}})$$

Magnetizing current:

$$I_M(t) = \frac{V_{P,\text{dc}} - V_{Q,\text{on}}}{L_M}$$
that is when switch Q1 is closed.
Primary winding $N_P$ voltage:

$$V_{P,\text{on}} = V_{dc} - V_{Q,\text{on}}$$

Reset winding $N_R$ voltage:

$$V_R = \frac{N_R}{N_P} \left( V_{dc} - V_{Q,\text{on}} \right)$$

Magnetizing current:

$$I_M(t) = \frac{V_{P,\text{on}}}{L_M} = \frac{V_{dc} - V_{Q,\text{on}}}{L_M}$$

In this case the voltage on winding $N_P$ is as shown in the figure: the upper side of winding $N_P$ is more positive than the lower side.
The full input voltage $V_{dc}$ is applied to the primary winding minus the voltage drop on switch Q1. The voltage on the primary is constant during the whole $T_{ON}$ period.
Primary winding $N_P$ voltage:

$$V_{P, on} = V_{dc} - V_{Q, on}$$

Reset winding $N_R$ voltage:

$$V_R = \frac{N_R}{N_P}(V_{dc} - V_{Q, on})$$

Magnetizing current:

$$I(t) = \frac{V_{P, I}}{L_M} = \frac{V_{dc} - V_{Q, on}}{L_M}$$

As a consequence diode D2 is reverse biased and can be removed from the circuit analysis; no current flows in the upper (reset) winding of the transformer.
The voltage on the reset winding can be easily computed considering the basic equations of ideal transformers we have seen in a preceding slide: the voltage on \( N_r \) is the voltage on \( N_p \) times the turns ratio \( N_r/N_p \).

Also the voltage on the reset winding is constant through the whole \( T_{ON} \) period.

Let us also consider what happens to the current in the primary winding.
Because of the applied voltage, current starts flowing in the Np turns entering from the transformer terminal with the dot. Basically, it behaves as an inductor. This means that the current flowing into Np is a positive ramp. The relation between current and applied voltage is linear.

Be aware that this current is only one of the components of the total current flowing into the primary. It is called the magnetizing current. To compute the total current flowing into the primary we must take into consideration also the fact that, as we will see shortly, some current (the load current) is flowing into the secondary. A portion of such current (proportional to the number of turns ratio) is reflected back into the primary.
Let us now analyze what happens at the secondary,
Secondary winding voltage:
\[ V_S = \frac{N_S}{N_P} \left( V_{dc} - V_{Q,\text{on}} \right) \]

Output inductor voltage:
\[ V_L = \frac{N_L}{N_P} \left( V_{dc} - V_{Q,\text{on}} \right) - V_{D,\text{on}} - V_{\text{out}} \]

Output inductor current:
\[ i_L(t) = i_L(0) + \frac{V_L}{L} t \]

during \( T_{ON} \).
Secondary winding voltage:
\[ V_S = \frac{N_S}{N_P} (V_{dc} - V_{Q,on}) \]

Output inductor voltage:
\[ V_L = \frac{N_L}{N_P} (V_{dc} - V_{Q,on}) - V_{D,on} - V_{out} \]

Output inductor current:
\[ i_L(t) = i_L(0) + \frac{V_L}{L} t \]

The upper edge of the secondary winding is more positive (because of the voltage on the primary) than the lower edge,
Secondary winding voltage:

$$V_S = \frac{N_S}{N_P} (V_{dc} - V_{Q,on})$$

Output inductor voltage:

$$V_L = \frac{N_L}{N_P} (V_{dc} - V_{Q,on}) - V_{D,on} - V_{out}$$

Output inductor current:

$$i_L(t) = i_L(0) + \frac{V_L}{L} t$$

consequently diode D2 is forward biased and D3 is reverse biased (open circuit).
The secondary voltage is as shown, constant during the whole $T_{ON}$ period and equals the primary voltage times the turns ratio.

If we consider to be at steady state, we can assume that the output voltage $V_{out}$ is constant. It is then easy to determine the voltage on the output inductor $V_L$. 

Secondary winding voltage:

$$V_S = \frac{N_S}{N_P} \left( V_{dc} - V_{Q, on} \right)$$

Output inductor voltage:

$$V_L = \frac{N_S}{N_P} \left( V_{dc} - V_{Q, on} \right) - V_{D, on} - V_{out}$$

Output inductor current:

$$i_L(t) = i_L(0) + \frac{V_L}{L} t$$
Secondary winding voltage:

\[ V_S = \frac{N_S}{N_P} \left( V_{dc} - V_{Q,on} \right) \]

Output inductor voltage:

\[ V_L = \frac{N_S}{N_P} \left( V_{dc} - V_{Q,on} \right) - V_{D,on} - V_{out} \]

Output inductor current:

\[ i_L(t) = i_L(0) + \frac{V_L}{L} \times t \]

Because of the voltage signs on the primary and secondary, the voltage on the inductor is as shown, that is the left edge is more positive than the right edge.
During this period the inductor is storing energy into its magnetic field.
As we know, if the voltage on an inductor is constant, the current is a ramp; in this case it will be a rising ramp, starting from some initial value (generally not zero) and up to some final value $I_L$ at $T_{ON}$. Note that this current also flows into the output capacitor and load.
Let us go back for a moment to the primary winding
Primary winding total current:

\[ I_{p, \text{total}} = I_p(0) + I_{sl}(t) + \frac{N_S}{N_P} I_L(t) \]

to have a better understanding of the current flowing through it.
As we have seen in a previous slide, one component of the primary current is the magnetizing current, which is a ramp whose slope is directly proportional to the input voltage and inversely to the magnetizing inductance of the transformer.
The second component of the primary current is the load current reflected back into the primary, through the windings turn ratio (Ns/Np). As we have seen, the secondary current is a ramp starting from some value \( I_L(0) \).
The total current is then the sum of these two contributions. Note that the magnetizing current is somehow exaggerated to make it more visible on the plot. One of the design targets of the transformer is to keep its value as a small percentage (usually around 10%) of the total useful load current.
Voltage on the reset winding:
\[ V_R = -\left( V_{dc} + V_{D,on} \right) \]

Voltage on the primary winding:
\[ V_P = -\frac{N_P}{N_R} \left( V_{dc} + V_{D,on} \right) \]

Reset winding current:
\[ I_R = \frac{N_P}{N_R} I_M \]

Let us now analyze what happens during \( T_{OFF} \), when switch Q1 is open.
Voltage on the reset winding:

\[ V_R = -(V_{dc} + V_{D,\text{on}}) \]

Voltage on the primary winding:

\[ V_P = -\frac{N_P}{N_R}(V_{dc} + V_{D,\text{on}}) \]

Reset winding current:

\[ I_R = \frac{N_P}{N_R} I_M \]

We should remember that the current through an inductor (transformer) cannot change polarity (direction) immediately, but it tries to continue to flow in the same direction.
Voltage on the reset winding:

\[ V_R = - \left( V_{dc} + V_{D,on} \right) \]

Voltage on the primary winding:

\[ V_P = - \frac{N_P}{N_R} \left( V_{dc} + V_{D,on} \right) \]

Reset winding current:

\[ I_R = \frac{N_P}{N_R} I_M \]

When switch Q1 opens, the current no longer has a path through the primary winding Np.
Voltage on the reset winding:
\[ V_R = -\left( V_{dc} + V_{D,\text{on}} \right) \]

Voltage on the primary winding:
\[ V_P = -\frac{N_P}{N_R} \left( V_{dc} + V_{D,\text{on}} \right) \]

Reset winding current:
\[ I_R = \frac{N_P}{N_R} I_M \]

The voltage on Np is reversed in polarity (this is the attempt of the inductor to keep the current flowing),
Voltage on the reset winding:

\[ V_R = -\left( V_{dc} + V_{D,on} \right) \]

Voltage on the primary winding:

\[ V_P = -\frac{N_P}{N_R} \left( V_{dc} + V_{D,on} \right) \]

Reset winding current:

\[ I_R = \frac{N_P}{N_R} I_M \]

which forces the voltage on Nr to also reverse. At this point the upper edge of Nr is negative in respect to the lower edge, and consequently diode D1 starts conducting. This operation creates a path for the magnetizing current to flow even if the switch Q1 is open.

As we have seen the voltage on the reset winding reverses polarity (is now negative).
Voltage on the reset winding:

\[ V_R = -(V_{dc} + V_{D, on}) \]

Voltage on the primary winding:

\[ V_P = -\frac{N_P}{N_R}(V_{dc} + V_{D, on}) \]

Reset winding current:

\[ I_R = \frac{N_P}{N_R} I_M \]

As we have seen the voltage on the reset winding reverses polarity (is now negative). Its value can be easily computed from the input voltage.
Voltage on the reset winding:
\[ V_R = -\left( V_{dc} + V_{D,\text{on}} \right) \]

Voltage on the primary winding:
\[ V_P = -\frac{N_P}{N_R} \left( V_{dc} + V_{D,\text{on}} \right) \]

Reset winding current:
\[ I_R = \frac{N_P}{N_R} I_M \]

The voltage on the primary can then be obtained from the reset voltage multiplied by the \( N_R/N_P \) transformer turns ratio.

The effect of a negative voltage on the reset winding is to linearly reduce the magnetizing current that was previously flowing.
Voltage on the reset winding:

\[ V_R = -(V_{dc} + V_{D,on}) \]

Voltage on the primary winding:

\[ V_P = -\frac{N_P}{N_R} \left( V_{dc} + V_{D,on} \right) \]

Reset winding current:

\[ I_R = \frac{N_P}{N_R} I_M \]

The effect of a negative voltage on the reset winding is to linearly reduce the magnetizing current that was previously flowing. As shown, the current flowing into the reset winding has initially the same value of the magnetizing current which was flowing into the primary \( N_P \) winding. It is simply diverted to the reset circuit and its value ramps down to zero because of the applied (negative) voltage on \( N_R \).

As shown the magnetizing current reaches zero at time \((T_{ON} + T_R)\).
Voltage on the reset winding:
\[ V_R = -(V_{dc} + V_{D,on}) \]

Voltage on the primary winding:
\[ V_P = -\frac{N_P}{N_R}(V_{dc} + V_{D,on}) \]

Reset winding current:
\[ I_R = \frac{N_P}{N_R} I_M \]

In this presentation we suppose that \( T_{OFF} \) is longer than \( T_R \), so that the primary winding is completely deenergized before the next PWM cycle.
The last step in our analysis is the behavior of the secondary during $T_{OFF}$. 

Output inductor voltage:

$$V_L = -V_{out} - V_{D,on}$$

Output inductor current:

$$I_L(t) = I(T_{ON}) - \frac{V_{out} + V_{D,on}}{L} t$$
The last step in our analysis is the behavior of the secondary during $T_{OFF}$.

We have seen previously that the voltage on the primary reverses as soon as the switch Q1 opens; this is because the inductor tries to keep current flowing in the same direction in which it was previously flowing. If external voltage is no longer applied, the only way to sustain such a current is for the voltage to reverse its polarity (in other words the inductor is no longer a utilizer, as it becomes a generator).
The voltage on the secondary is then such that the upper edge of the winding Ns is more negative than the lower edge:
D2 become reverse biased (an open circuit) while D3 is forward biased and starts conducting. It is almost a short circuit and all the current flowing into the load passes through it (this is termed freewheeling functionality).

If we consider again to be at steady state it is easy to compute the voltage on the output inductor as shown in the equation.

Output inductor voltage:

$$V_L = -V_{out} - V_{D, on}$$

Output inductor current:

$$I_L(t) = I(T_{ON}) - \frac{V_{out} + V_{D, on}}{L} t$$
Forward Converter

Output inductor voltage:

\[ V_L = - V_{out} - V_{D,\text{on}} \]

Output inductor current:

\[ I_L(t) = I(T_{ON}) - \frac{V_{out} + V_{D,\text{on}}}{L} t \]

Please note that the voltage on this inductor changes polarity also: the right edge is now more positive than the left edge, the current continues flowing into the load and the inductor is now a generator, using the energy stored into its magnetic field during \( T_{ON} \) to supply the current to the output.
Output inductor voltage:

\[ V_L = -V_{out} - V_{D,\text{on}} \]

Output inductor current:

\[ I_L(t) = I(T_{\text{ON}}) - \frac{V_{out} + V_{D,\text{on}}}{L} t \]

Since the inductor voltage is constant,
the current in the inductor will be a (falling) ramp from the initial peak value reached at time $T_{ON}$ down to its value at time $T$. 

Output inductor voltage:

$$V_L = -V_{out} - V_{D,on}$$

Output inductor current:

$$I_L(t) = I(T_{ON}) - \frac{V_{out} + V_{D,on}}{L} \cdot t$$
One key point in the analysis is that the output inductor current at the beginning of the PWM period equals the current at the end of the period $I_L(T)$. This is required by the hypothesis we are in steady state. If this equality is not true, it means that the system has not yet reached the steady state operation, and we have to wait for this condition to apply all the analysis and results we have discussed so far.
In the time interval between \((T_{ON} + T_R)\) and \(T\),
In the time interval between \((T_{ON} + T_R)\) and \(T\), as soon as the magnetizing current has reached zero (at \(T_{ON} + T_R\)), all the energy that had been stored into the transformer has been released.
The voltage drop on $N_R$ becomes zero and the voltages at both ends of $N_R$ equal $V_{dc}$. Diode D1 becomes reverse biased and is no longer conducting.
The voltage drop on \( N_p \) becomes zero.

As for the output circuit, nothing changes compared to the time interval from \( T_{ON} \) to \( (T_{ON} + T_R) \).
At this point we can determine the input/output relationship.

As noted in the previous slide the output inductor current at time zero equals the output inductor current at time $T$. This means that the current increase during $T_{ON}$ must equal the current decrease during $T_{OFF}$.

Remembering the equations we have seen in previous slides, the current increase (or decrease) is directly proportional to the applied voltage and inversely proportional to the inductance value times the interval during which the voltage is applied. In other words the two areas $A1$ and $A2$ shown in the figure must be equal to each other.
Input-output relationship:

\[ V_o = \frac{N_S}{N_P} D V_{dc} \]

Where:

\[ D = \frac{T_{ON}}{T} \]

Using the equations computed before, we can easily obtain the relationship between the input and output voltages.
The relationship is linear and it is proportional to:

1. D, which is the duty cycle, and to
2. The ratio (Ns / Np), which is the transformer windings turns ratio.

This is an important result. It tells us that the transformer turns ratio can also be used to define, in the design step, the output voltage value.
Forward Converter

Design Equations: Transformer primary

Flux change during $T_{ON}$:

$$\Delta B = \frac{V_P T_{ON}}{N_P A_{core}}$$

Solving respect to $N_P$ and considering to run the system at maximum $T_{ON}$:

$$N_P = \frac{D_{max}}{F_{PWM} A_{core} \Delta B} V_{dc, min} \quad N_S = \frac{V_o}{F_{PWM} A_{core} \Delta B}$$

Design Equations.
We will now present the design equations.
Let us start with the selection of the magnetics. During a switching period the transformer core operates along its hysteresis curve in its B-H plot.
The change in magnetic flux can be determined by the Faraday law. It is proportional to the product of the voltage ($V_p$) applied to the primary winding during time $T_{ON}$ and time $T_{ON}$ itself. As you can see from the equation the change of magnetic flux is also inversely proportional to the product of the number of turns at the primary and to a constant ($A_{core}$) which depends on the specific transformer design and is published in the data sheets by the transformer manufacturer.

Practically, in this equation we know all the terms, a part from $N_p$ and $\Delta B$. The maximum $\Delta B$ value is obtained from the characteristic curves of the transformer, corresponding to a point on the hysteresis curve which is quite distant from the saturation region of the core. Once this value has been determined, it is easy to get the value $N_p$ of the number of turns at the primary.

At the end of a pwm period, we would like to have a total flux change equal to zero. This will guarantee that the system does not move along the B-H characteristic to saturation.

As a consequence of the relationship above, the maximum flux change occurs when the duty cycle is maximum, which is when $T_{ON}$ assumes its biggest value.

If we solve the previous equation with $T_{ON}$ replaced by $T_{ON,\text{max}}$ we get the number of required turns in the transformer.
Forward Converter

Design Equations: Transformer primary

Flux change during $T_{ON}$:

$$\Delta B = \frac{V_P T_{ON}}{N_P A_{core}}$$

Solving respect to $N_P$ and considering to run the system at maximum $T_{ON}$:

$$N_P = \frac{D_{max}}{F_{PWM} A_{core} \Delta B} V_{dc,min}$$

$$N_S = \frac{V_o}{F_{PWM} A_{core} \Delta B}$$

The dependance of the number of primary turns from the maximum value of the $T_{ON}$ period, is expressed in this equation by the term $D_{max}$.
Forward Converter

Design Equations: Transformer primary

Flux change during T\textsubscript{ON}:

\[ \Delta B = \frac{V_P T_{ON}}{N_P A_{core}} \]

Solving respect to N\textsubscript{P} and considering to run the system at maximum T\textsubscript{ON}:

\[ N_P = \frac{D_{max}}{F_{PWM} A_{core} \Delta B} V_{dc, min} \]

\[ N_S = \frac{V_o}{F_{PWM} A_{core} \Delta B} \]

Moreover using the input/output relationship we found in the previous slide, we can also easily determine the number of turns at the secondary to sustain the specified output voltage V\textsubscript{o}. 

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Design Equations: Mosfet

Voltage on Q1:

\[ V_{Q,off} = \left(1 + \frac{N_P}{N_R}\right) V_{dc} \]

With some margin:

\[ V_{Q,max} = 1.3 \ V_{Q,off} \]

Design Equations: Mosfet selection.
The selection of the MOSFET switch should be done analyzing the maximum voltage it has to withstand.
During $T_{ON}$, the voltage on the switch is almost zero, since the switch is closed.
Design Equations: Mosfet

Voltage on Q1:

\[ V_{Q,off} = \left(1 + \frac{N_p}{N_R}\right)V_{dc} \]

With some margin:

\[ V_{Q,max} = 1.3 \ V_{Q,off} \]

During \( T_R \) the switch is subject to a voltage which is proportional to the product of \( V_{dc} \) and the primary to reset turn ratio.
Forward Converter

Design Equations: Mosfet

Voltage on Q1:

\[ V_{Q\text{off}} = \left(1 + \frac{N_p}{N_R}\right)V_{dc} \]

With some margin:

\[ V_{Q\text{,max}} = 1.3 V_{Q\text{off}} \]

During the time interval from \((T_{ON} + T_R)\) to \(T\) the voltage on the switch is \(V_{dc}\).

The maximum current that is flowing through the switch is the sum of the magnetizing current and the load current reflected back into the primary.

The \(N_p / N_r\) ratio gives us an additional degree of freedom, to set the output voltage level. But on the other side it also is responsible for an increase on the voltage that must be sustained by the switch. In the case where \(N_p = N_R\), the voltage on Q1 is twice the input voltage (as shown in the figure).

Because of spikes due to leakage current, a margin of about 30% is normally used, so that the total voltage on the switch is greater than what is computed by the equation.
Design Equations: Mosfet

Voltage on Q1:

\[ V_{Q, off} = \left(1 + \frac{N_p}{N_R}\right)V_{dc} \]

With some margin:

\[ V_{Q, max} = 1.3 \, V_{Q, off} \]

Because of spikes due to leakage current, a margin of about 30% is normally used, so that the total voltage on the switch is greater than what is computed by the equation.
Design Equations: Diodes.
In order to select the diodes used in the forward converter we have to analyze the maximum current and voltage they have to sustain. Note that we can only be in one of the following two conditions at any time:

1. The diode is conducting: the voltage across the diode is close to 1V (its real value depends on the type of diode and the intensity of the flowing current). The current is determined by the rest of the external circuit (and the diode must be dimensioned in order to be able to sustain such a current).
2. The diode is not conducting: The current through the diode is zero (because it operates as an open circuit), but the voltage is imposed by the rest of the circuit. And, as for the current, we must ensure that the diode can withstand such a voltage.

If we consider the three intervals of time in which the PWM period is split, we see that:

\[
V_{D1,\text{max}} = \left(1 + \frac{N_R}{N_P}\right)V_{dc,\text{max}}
\]

\[
V_{D2,\text{max}} = -\frac{N_S}{N_R}V_{dc,\text{max}}
\]

\[
V_{D3,\text{max}} = -\frac{N_S}{N_P}V_{dc,\text{max}}
\]
Diodes selection:

\[ V_{D1,\text{max}} = \left(1 + \frac{N_R}{N_P}\right)V_{dc,\text{max}} \]

\[ V_{D2,\text{max}} = -\frac{N_S}{N_R}V_{dc,\text{max}} \]

\[ V_{D3,\text{max}} = -\frac{N_S}{N_P}V_{dc,\text{max}} \]

Interval 0, \( T_{ON} \)

Diode D1 is reversed biased. The max voltage on it is proportional to the maximum possible input voltage times the factor \((1 + N_R / N_P)\). Current is zero.

Diode D2 is forward biased. The voltage is around 1V.
Diodes selection:

\[ V_{D1,\text{max}} = \left(1 + \frac{N_R}{N_P}\right)V_{dc,\text{max}} \]

\[ V_{D2,\text{max}} = \frac{N_S}{N_R}V_{dc,\text{max}} \]

\[ V_{D3,\text{max}} = \frac{N_S}{N_P}V_{dc,\text{max}} \]

Diode D3 is reverse biased. The voltage is proportional to the product of the input voltage and the ratio \( \frac{N_S}{N_P} \).
Diodes selection:

\[ V_{D1,\text{max}} = \left(1 + \frac{N_R}{N_P}\right)V_{dc,\text{max}} \]

\[ V_{D2,\text{max}} = \frac{N_S}{N_R}V_{dc,\text{max}} \]

\[ V_{D3,\text{max}} = -\frac{N_S}{N_P}V_{dc,\text{max}} \]

Interval \( T_{ON}, T_{ON} + T_R \)

Diode D1 is forward-biased. The voltage is close to 1V and the current is the magnetizing current.

Diode D2 is reverse biased and its maximum value is proportional to the product of \( V_{dc,\text{max}} \) and the ratio \( \frac{N_S}{N_R} \).

Diode D3 is forward-biased. The voltage is close to 1V.

Interval \( T_{ON} + T_R, T \)

Diode D1 is reverse biased and the maximum voltage is \( V_{dc,\text{max}} \).

Diodes D2 and D3 are reverse biased and the voltage on them is almost zero.
Forward Converter

Minimum inductor current (critical mode):\
\[ I_{o,\text{min}} = \frac{I_{\text{out, ripple}}}{2} \]

Inductor value:
\[ L = \frac{N_s}{N_p} \frac{V_{dc,\text{min}} - V_{out}}{2 F_{PWM} I_{o,\text{min}} D_{\text{max}}} \]

Design Equations: output LC filter selection
In the forward converter, the output inductor together with the output capacitor make a low-pass filter that removes the ripple components from the output current and voltage.
As in all topologies that present such an output stage, the inductor value is chosen so that the inductor current never goes below zero.
As shown by the plot the inductor current has two components: the average value, which is also the output current, and the superimposed ripple current which is filtered away by the capacitor, whose impedance is supposed to be low at the PWM switching frequency. If this is true, the capacitor behaves as a short circuit (low impedance path) to ground for the ripple current.

If the inductor current only goes to zero at the beginning and at the end of the PWM period, we say the system is working in critical mode. It is easy to see from the figure that in this case the average output current is exactly one half of the inductor peak current.
The inductor value can than be determined by the equation that gives the current increase in the inductor as a consequence of the applied, constant voltage, during $T_{ON}$. Solving such an equation for $L$, dividing both numerator and denominator by $T$, with some easy computation we get the expression that can be used to determine the inductor value. Note that in this equation $I_{o,min}$ is known, since it is the minimum output current requested by the design specifications.
Design Equations: Output Capacitor

Contributions:
1. Capacitor model equivalent resistance ($R_{ESR}$):

$$V_{r,ESR} = R_{ESR} (I_2 - I_1) = R_{ESR} \Delta I_L$$

2. Voltage drop on the capacitor ($V_{r,Co}$):

$$V_{r,Co} = \frac{1}{C} \int i_c(t) \, dt$$

Summing and rearranging terms, we have:

$$C_0 = \frac{\Delta I_L D}{F_{PWM} [\Delta V_{r,\text{total}} - R_{ESR} \Delta I_L]}$$

Design Equations: Output Capacitor
As we have seen in the previous slide the capacitor impedance should be as low as possible to appear as a short circuit to ground for the ripple current flowing into the inductor.
The selection of the output capacitor is related to the maximum amount of ripple voltage allowed by the design specifications. We consequently have to analyze with some detail, what are the contributions to the output ripple. To do so, we should consider the capacitor equivalent circuit, where we have an ideal capacitor, plus a resistor. In the model you can also normally find an inductor but its value is normally such that it does not significantly influence the output ripple amplitude.
Forward Converter

Design Equations: Output Capacitor

Contributions:
1. Capacitor model equivalent resistance ($R_{ESR}$):

\[
V_{r,ESR} = R_{ESR} (I_2 - I_1) = R_{ESR} \Delta I_L
\]

2. Voltage drop on the capacitor ($V_{r,c0}$):

\[
V_{r,c0} = \frac{1}{C} \int i_c(t) dt
\]

Summing and rearranging terms, we have:

\[
C_0 = \frac{\Delta I_L D}{F_{PWM} \left[ \Delta V_{r,total} - R_{ESR} \Delta I_L \right]}
\]

The presence of a resistor in the model ($R_{ESR}$), has as a consequence that the inductor ripple current will generate a ripple voltage at its terminals.
Design Equations: Output Capacitor

Contributions:

1. Capacitor model equivalent resistance \( R_{\text{ESR}} \):

\[
V_{r,\text{ESR}} = R_{\text{ESR}} (I_2 - I_1) = R_{\text{ESR}} \Delta I_L
\]

2. Voltage drop on the capacitor \( V_{r,C_0} \):

\[
V_{r,C_0} = \frac{1}{C} \int i_c(t) \, dt
\]

Summing and rearranging terms, we have:

\[
C_0 = \frac{\Delta I_L D}{\bar{V}_{r,\text{total}} - R_{\text{ESR}} \Delta I_L}
\]

The second contribution directly comes from the capacitor. Current flowing into the capacitor will generate a voltage drop which can be computed as the integral over time of the current itself. The capacitor value appears in this equation as a proportionality factor.

Summing these two contributions gives the maximum ripple voltage that will be developed at the capacitor terminals. This value must be lower than the maximum acceptable ripple voltage, as defined by design specifications.
Forward Converter

Design Equations: Output Capacitor

Contributions:
1. Capacitor model equivalent resistace \( R_{ESR} \):
   \[
   V_{r,ESR} = R_{ESR} (I_2 - I_1) = R_{ESR} \Delta I_L
   \]

2. Voltage drop on the capacitor \( V_{r,Co} \):
   \[
   V_{r,Co} = \frac{1}{C} \int i_c(t) \, dt
   \]

Summing and rearranging terms, we have:

\[
C_0 = \frac{\Delta I_L D}{F_{PWM} \left[ \Delta V_{r,\text{total}} - R_{ESR} \Delta I_L \right]}
\]

With some computation, it is easy to determine the value of the capacitor as shown by the last equation.
Thank you for attending this WebSeminar. For more information please visit the microchip website at www.microchip.com