PCN #: JAON-25VHDK219

Date:
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Qualification of an additional fabrication site for DMOS 2.5 Supertex products

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Test Conditions

Tests are performed in accordance with Microchip specification QCI-39000, “Worldwide Quality Conformance Requirements”. The various conditions are listed below with specifics of the SuperTex specification testing.

TEST	METHOD	CONDITIONS	ACTUAL SAMPLE SIZE RUN	CRITERIA (Min Samples) (Fail /Pass)
High Temperature Operating Life	MIL-STD 750-1 Method 1042.4	150°C, 1000 Hrs Electrical Test at +25°C	100, 100, 100	0/90 per lot 3 Lots ½ for HTRB, ½ for HTGB
High Temp Reverse Bias	AEC-Q101, MIL-STD-750-1 Method M1042.1 Condition A	1000 hours at TJ(max) rating, with device biased to 100% of the rated drain-source breakdown voltage Electrical Test: +25°C	50, 50, 50	0/45 per lot Note 1
High Temp Gate Bias	AEC-Q101 MIL-STD-750-1 Method M1042.1 Condition B	1000 hours at TJ(max) rating, with device biased to 100% of maximum rated gate-source voltage Electrical Test: +25°C	50, 50, 50	0/45 per lot Note 1
ESD Human Body Model	Mil-Std 750, M1020	1.5K Ohm, 100 pF Electrical Test at +25°C, Class 0	27 / lot	By part

Actual sample size includes the Minimum requires samples + spares.

Note 1: Acceptance criteria

a) Pass DC data sheet specifications
b) ΔI_{GSS} = ±10nA DC or 100% of the initial value, whichever is greater
c) ΔI_{DSS} = ±1uA DC or 100% of the initial value, whichever is greater
d) $\Delta R_{DS(ON)}$ = ±10% of the initial value
e) $\Delta V_{GS(TH)}$ = ±10% of the initial value
f) ΔB_{VDSS} = ±5% of the initial value

Qualification Material

Information regarding the devices that were used in this qualification is shown in the table below.

LOT	LOT 1	LOT 2	LOT 3
DEVICE	TN0610N3-G, (TN25A)	TN0620N3-G, (TN25C)	TP0620N3-G, (TP25C)
MASK, (REV)	63003, (EA)	63003, (EA)	63003, (EA)
WAFER FAB	Microchip Tempe	Microchip Tempe	Microchip Tempe
WAFER PROCESS	DMOS2.5, 8”	DMOS2.5, 8”	DMOS2.5, 8”
MSL	2007	2021	2022
WAFER LOT	TMPE 215055187.000	TMPE 215055188.000	TMPE 215065381.000
ASSEMBLY LOT	E05518701	E05518801	E06538101
PACKAGE	3L T0-92	3L T0-92	3L T0-92
ASSEMBLY SITE	Cirtek	Cirtek	Cirtek
REL TESTED	Microchip Sunnyvale	Microchip Sunnyvale	Microchip Sunnyvale
FINAL TEST	Microchip HKDC	Microchip HKDC	Microchip HKDC
QUAL #	14Qual-006	14Qual-007	14Qual-031
QUAL TESTS	HTOL-(HTRB / HTGB) / ESD	HTOL-(HTRB / HTGB) / ESD	HTOL-(HTRB / HTGB) / ESD

Die Level Results

The results of die level testing are shown below.

HIGH TEMPERATURE OPERATING LIFE TESTING @ 150°C

	1000 Hours (Fail/Pass)
Lot 1 Total Parts	0/100
Lot 2 Total Parts	0/100
Lot 3 Total Parts	0/100

HIGH TEMPERATURE REVERSE BIAS (HTRB) @ 150°C

	168 Hours (Fail/Pass)	500 Hours (Fail/Pass)	1,000 Hours (Fail/Pass)
Lot 1	0/50	0/50	0/50
Lot 2	0/50	0/50	0/50
Lot 3	0/50	0/50	0/50

HIGH TEMPERATURE GATE BIAS (HTGB) @ 150°C

	168 Hours (Fail/Pass)	500 Hours (Fail/Pass)	1,000 Hours (Fail/Pass)
Lot 1	0/50	0/50	0/50
Lot 2	0/50	0/50	0/50
Lot 3	0/50	0/50	0/50

ELECTROSTATIC DISCHARGE TESTS

Human Body Model	Domain	Pass Voltage
Lot 1 & 2	Drain to Gate/Source	Up to ± 2.2kV
	Source to Drain/Gate	Up to ± 2.1kV
	Gate to Source	Up to ± 0.2kV
	Gate to Drain	Up to ± 0.2kV
	Drain to Source	Up to ± 8.0kV
Lot 3	Drain to Gate/Source	Up to ± 1.7kV
	Source to Drain/Gate	Up to ± 1.5kV
	Gate to Source	Up to ± 0.16kV
	Gate to Drain	Up to± 0.16kV
	Drain to Source	Up to ± 8.0kV