VC-827

Differential (LVPECL, LVDS) Crystal Oscillator

Features

- Ultra-Low Jitter Performance: 3rd OT or Fundamental Crystal Design
- Extended Operating Temperature Range: –40°C to +105°C
- Excellent Power Supply Rejection Ratio
- Enable/Disable
- 1.8V (LVDS), 2.5V, or 3.3V Supply Voltage
- Hermetically Sealed 3.2 mm x 2.5 mm Ceramic Package
- Product is Compliant to RoHS Directive and Fully Compatible with Lead Free Assembly (Excluding Solder Dipped, _SNPB, Option)

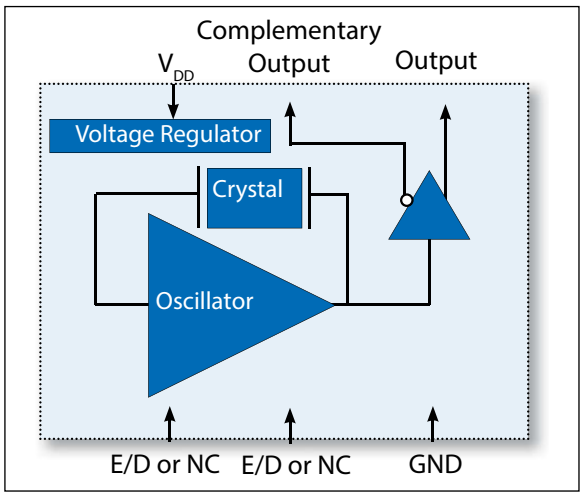
Applications

- Ethernet, GbE, Synchronous Ethernet
- PCIe
- Fibre Channel
- Enterprise Servers and Storage
- Clock Source for ADCs, DACs, FPGAs
- Test and Measurement
- GPON

General Description

The VC-827 crystal oscillator is a quartz-stabilized, differential output oscillator that operates off a 1.8V (LVDS), 2.5V, or 3.3V supply in a hermetically sealed 3.2 mm x 2.5 mm ceramic package.

Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

ELECTRICAL PERFORMANCE, LVPECL OPTION

Parameter	Sym.	Min.	Typ.	Max.	Units	Conditions
Supply Voltage (Note 1)	V_{DD}	3.135	3.3	3.465	V	—
		2.375	2.5	2.625		—
Current Consumption	I_{DD}	—	—	69	mA	3.3V
		—	—	61		2.5V
Frequency						
Nominal Frequency	f_{NOM}	20	—	220	MHz	Ordering Option
Frequency Stability (Note 2)	f_{STAB}	—	—	±25	ppm	Ordering Option
		—	—	±50		
		—	—	±100		
Outputs						
Output Logic Level High	V_{OH}	V_{DD} – 1.025	—	V_{DD} – 0.880	V	Note 3
Output Logic Level Low	V_{OL}	V_{DD} – 1.810	—	V_{DD} – 1.650	V	Note 3
Output Rise and Fall Time	t_R/t_F	—	—	500	ps	Note 3, Note 4
Load	—	50Ω into V_{DD} – 2.0V				—
Duty Cycle (Note 5)	DC	45	—	55	%	—
Phase Noise, 3.3V, 156.25 MHz (Note 6)	ϕ_N	—	–80	—	dBc/Hz	10 Hz
		—	–111	—		100 Hz
		—	–134	—		1 kHz
		—	–147	—		10 kHz
		—	–153	—		100 kHz
		—	–155	—		1 MHz
		—	–156	—		20 MHz
		—	–156	—		40 MHz
Phase Jitter, 156.25 MHz (Note 6)	ϕ_J	—	95	130	fs	12 kHz to 20 MHz
Enable/Disable						
Outputs Enabled	V_{IH}	0.7*V_{DD}	—	—	V	Note 7
Outputs Disabled	V_{IL}	—	—	0.3*V_{DD}	V	—
Disable Time	t_{DIS}	—	—	200	ns	—
Enable/Disable Leakage Current	$I_{E/D}$	—	—	±200	µA	—

Note 1: The VC-827 power supply pin should be filtered (e.g. a 10 µF, 0.1 µF, and 0.01 µF capacitor).

2: Includes calibration tolerance, operating temperature, supply voltage variations, aging, and IR reflow.

3: Figure 1-1 defines the test circuit and Figure 1-2 defines these parameters.

4: Output rise and fall time is 600 ps (max.) for the –40°C to +105°C operating temperature range.

5: Duty Cycle is defined as the On-Time divided by Period.

6: Measured using an Agilent E5052 Signal Source Analyzer at +25°C.

7: Outputs will be enabled if Enable/Disable is left open.

ELECTRICAL PERFORMANCE, LVPECL OPTION (CONTINUED)

Parameter	Sym.	Min.	Typ.	Max.	Units	Conditions
Start-Up Time	t_{SU}	—	—	10	ms	—
Operating Temperature	T_{OP}	–10	—	+70	°C	Ordering Option
		–40	—	+85		
		–40	—	+105		

Note 1: The VC-827 power supply pin should be filtered (e.g. a 10 µF, 0.1 µF, and 0.01 µF capacitor).

2: Includes calibration tolerance, operating temperature, supply voltage variations, aging, and IR reflow.

3: Figure 1-1 defines the test circuit and Figure 1-2 defines these parameters.

4: Output rise and fall time is 600 ps (max.) for the –40°C to +105°C operating temperature range.

5: Duty Cycle is defined as the On-Time divided by Period.

6: Measured using an Agilent E5052 Signal Source Analyzer at +25°C.

7: Outputs will be enabled if Enable/Disable is left open.

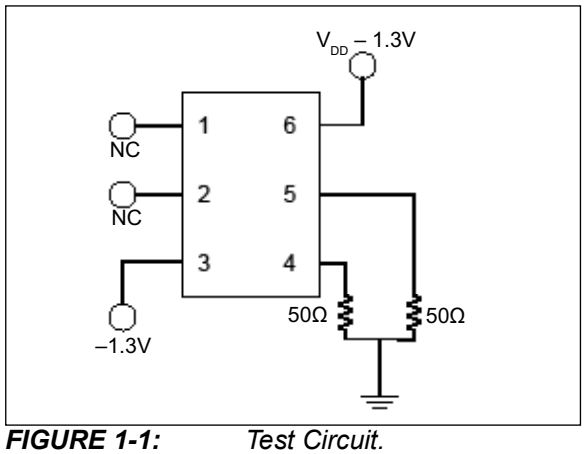


FIGURE 1-1: *Test Circuit.*

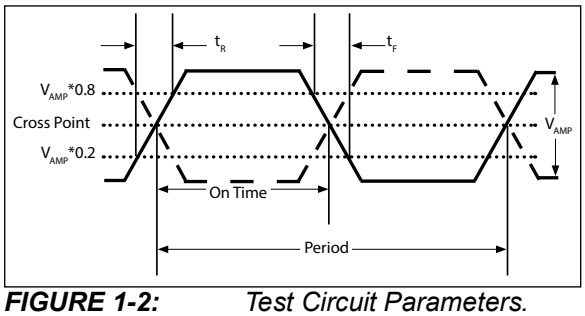


FIGURE 1-2: *Test Circuit Parameters.*

ELECTRICAL PERFORMANCE, LVDS OPTION

Parameter	Sym.	Min.	Typ.	Max.	Units	Conditions
Supply Voltage (Note 1)	V_{DD}	3.135	3.3	3.465	V	Ordering Option
		2.375	2.5	2.625		
		1.71	1.8	1.89		
Current Consumption	I_{DD}	—	—	33	mA	3.3V
		—	—	29		2.5V
		—	—	21		1.8V
Frequency						
Nominal Frequency (Ordering Option)	f_{NOM}	20	—	220	MHz	3.3V, 2.5V
		100	—	175		1.8V
Frequency Stability (Note 2)	f_{STAB}	—	—	±25	ppm	Ordering Option
		—	—	±50		
		—	—	±100		
Outputs						
Output Logic Level High	V_{OH}	—	1.43	1.6	V	Note 3
Output Logic Level Low	V_{OL}	0.9	1.10	—	V	Note 3
Output Amplitude	—	247	330	454	mV	—
Differential Output Error	—	—	—	50	mV	—
Offset Voltage	V_{OFF}	1.125	1.25	1.375	V	—
Offset Voltage Error	—	—	—	50	mV	—
Output Leakage Current	—	—	—	10	µA	Outputs Disabled
Output Rise and Fall Time (Note 3, Note 4)	t_R/t_F	—	—	500	ps	—
Load	—	100Ω Differential				—
Duty Cycle (Note 5)	DC	45	—	55	%	—
Phase Noise, 3.3V, 156.25 MHz (Note 6)	ϕ_N	—	–77	—	dBc/Hz	10 Hz
		—	–107	—		100 Hz
		—	–134	—		1 kHz
		—	–148	—		10 kHz
		—	–154	—		100 kHz
		—	–156	—		1 MHz
		—	–157	—		20 MHz
		—	–157	—		40 MHz

Note 1: The VC-827 power supply pin should be filtered (e.g. a 10 µF, 0.1 µF, and 0.01 µF capacitor).

2: Includes calibration tolerance, operating temperature, supply voltage variations, aging, and IR reflow.

3: Figure 1-3 defines the test circuit and Figure 1-2 defines these parameters.

4: Output rise and fall time is 600 ps (max.) for the –40°C to +105°C operating temperature range.

5: Duty Cycle is defined as the On-Time divided by Period.

6: Measured using an Agilent E5052 Signal Source Analyzer at +25°C.

7: Outputs will be enabled if Enable/Disable is left open.

ELECTRICAL PERFORMANCE, LVDS OPTION (CONTINUED)

Parameter	Sym.	Min.	Typ.	Max.	Units	Conditions
Phase Jitter, 156.25 MHz (Note 6)	ϕ_J	—	90	125	fs	12 kHz to 20 MHz
Enable/Disable						
Outputs Enabled (Note 7)	V_{IH}	0.7*V_{DD}	—	—	V	—
Outputs Disabled	V_{IL}	—	—	0.3*V_{DD}	V	—
Disable Time	t_{DIS}	—	—	200	ns	—
Enable/Disable Leakage Current	$I_{E/D}$	—	—	±200	µA	—
Start-Up Time	t_{SU}	—	—	10	ms	—
Operating Temperature	T_{OP}	–10	—	+70	°C	Ordering Option
		–40	—	+85		
		–40	—	+105		

Note 1: The VC-827 power supply pin should be filtered (e.g. a 10 µF, 0.1 µF, and 0.01 µF capacitor).

2: Includes calibration tolerance, operating temperature, supply voltage variations, aging, and IR reflow.

3: Figure 1-3 defines the test circuit and Figure 1-2 defines these parameters.

4: Output rise and fall time is 600 ps (max.) for the –40°C to +105°C operating temperature range.

5: Duty Cycle is defined as the On-Time divided by Period.

6: Measured using an Agilent E5052 Signal Source Analyzer at +25°C.

7: Outputs will be enabled if Enable/Disable is left open.

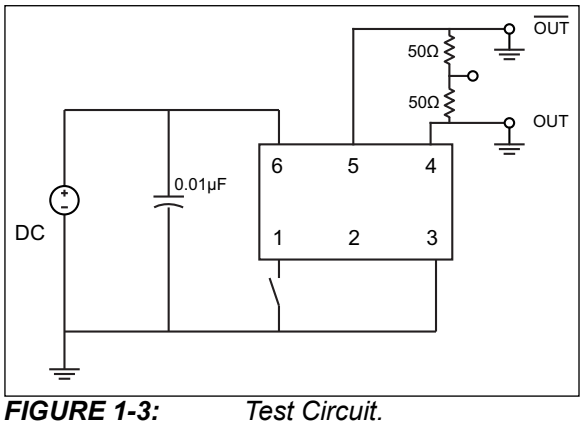


FIGURE 1-3: *Test Circuit.*

Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can permanently damage the device. Functional operation is not implied at these or any other conditions in excess of conditions represented in the operational sections of this data sheet. Exposure to absolute maximum ratings for extended periods may adversely affect device reliability.

Parameter	Symbol	Value
Storage Temperature	$T_{STORAGE}$	–55°C to +125°C
Maximum Junction Temperature	$T_{J(MAX)}$	+150°C
Supply Voltage	V_{DD}	–0.5V to +5.0V
Enable/Disable Voltage	$V_{E/D}$	–0.5V to V_{DD} + 0.5V

Handling Precautions

Although ESD protection circuitry has been designed into the VC-827, proper precautions should be taken when handling and mounting. Microchip employs a Human Body Model and a Charged Device Model (CDM) for ESD susceptibility testing and design protection evaluation. ESD thresholds are dependent on the circuit parameters used to define the model. Although no industry standard has been adopted for the CDM, a standard HBM of resistance = 1.5 kΩ and capacitance = 100 pF is widely used and therefore can be used for comparison purposes.

TABLE 1-1: ESD RATINGS

Model	Minimum	Conditions
Human Body Model	1500V	—
Charged Device Model	1500V	—

2.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 2-1 and the optional Enable/Disable function is detailed in Table 2-2.

TABLE 2-1: PIN FUNCTION TABLE

Pin Number	Pin Name	Description
1	E/D or NC	Enable/Disable or No Connection. (Note 1)
2	E/D or NC	Enable/Disable or No Connection. (Note 1)
3	GND	Electrical and Lid Ground.
4	f_O	Output Frequency.
5	Cf_O	Complementary Output Frequency.
6	V_{DD}	Supply Voltage.

Note 1: E/D can be provided on Pin 1 or Pin 2.

TABLE 2-2: ENABLE/DISABLE FUNCTION (OPTIONAL)

Pin 1 or 2	Pin 4, 5 Output
High	Clock Output
Open	Clock Output
Low	High Impedance

3.0 RELIABILITY

TABLE 3-1: ENVIRONMENTAL COMPLIANCE

Parameter	Conditions
Mechanical Shock	MIL-STD-883, Method 2002
Mechanical Vibration	MIL-STD-883, Method 2007
Temperature Cycle	MIL-STD-883, Method 1010
Solderability	MIL-STD-883, Method 2003
Fine and Gross Leak	MIL-STD-883, Method 1014
Resistance to Solvents	MIL-STD-883, Method 2015
Moisture Sensitivity Level	MSL1
Contact Pads	Gold (0.3 µm to 1.0 µm) over Nickel
θ_{JC} (bottom of case)	23°C/W
Maximum Junction Temperature	150°C
Weight	28 mg

4.0 LVPECL APPLICATION DIAGRAMS

The VC-827 incorporates a standard PECL output scheme, which are unterminated FET drains. There are numerous application notes on terminating and interfacing PECL logic. The two most common methods are a single resistor to ground (Figure 4-1) and a pull-up/pull-down scheme (Figure 4-2). AC-coupling capacitors are optional, depending on the application and the input logic requirements of the next stage.

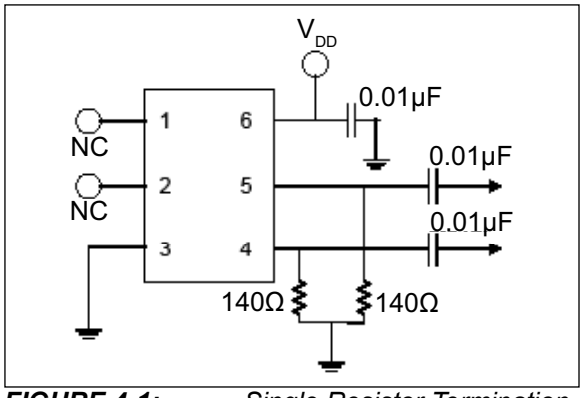


FIGURE 4-1: *Single Resistor Termination Scheme.*

Resistor values are typically 140Ω for 3.3V operation and 84Ω for 2.5V operation.

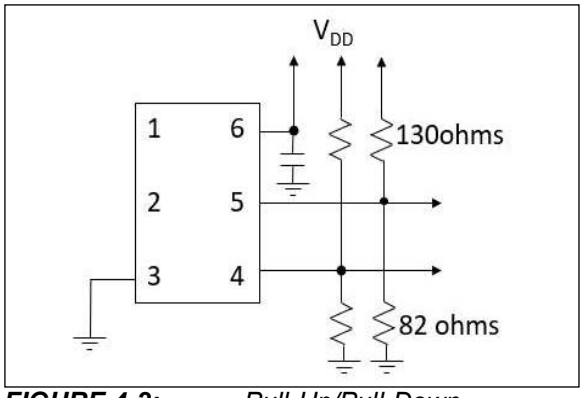


FIGURE 4-2: *Pull-Up/Pull-Down Termination Scheme.*

Resistor values shown are typical for 3.3V operation. For 2.5V operation, the resistor to ground is 62Ω and the resistor to supply is 250Ω. AC-blocking capacitors can be used if the DC levels are incompatible.

5.0 LVDS APPLICATION DIAGRAMS

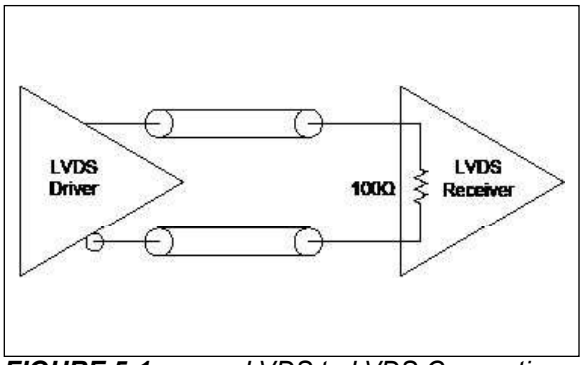


FIGURE 5-1: *LVDS to LVDS Connection, Internal 100Ω Resistor.*

Some LVDS structures have an internal 100Ω resistor on the input and do not need additional components.

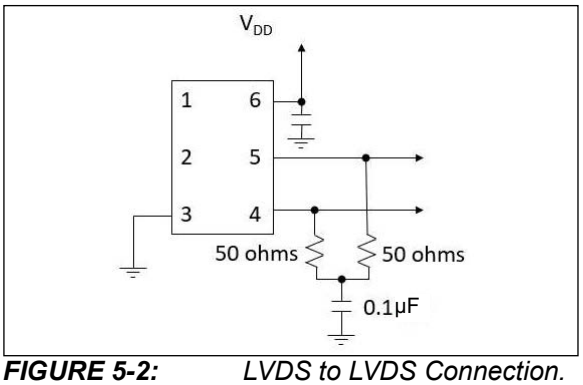


FIGURE 5-2: *LVDS to LVDS Connection.*

Some input structures might not have an internal 100Ω resistor on the input and will need an external 100Ω resistor for impedance matching. Also, the input may have an internal DC bias that may not be compatible with LVDS levels. AC-blocking capacitors can be used.

One of the most important considerations is terminating the Output and Complementary Output equally. An unused output should not be left unterminated, and if one of the two outputs is left open, it will result in excessive jitter on both. PCB layout must take this and 50Ω impedance matching into account. Load matching and power supply noise are the main contributors to jitter related problems.

6.0 IR REFLOW

The VC-827 is built using lead-free epoxy and can be subjected to standard lead-free IR reflow conditions shown in Table 6-1. Contact pads are gold over nickel and lower maximum temperatures can also be used, such as 220°C.

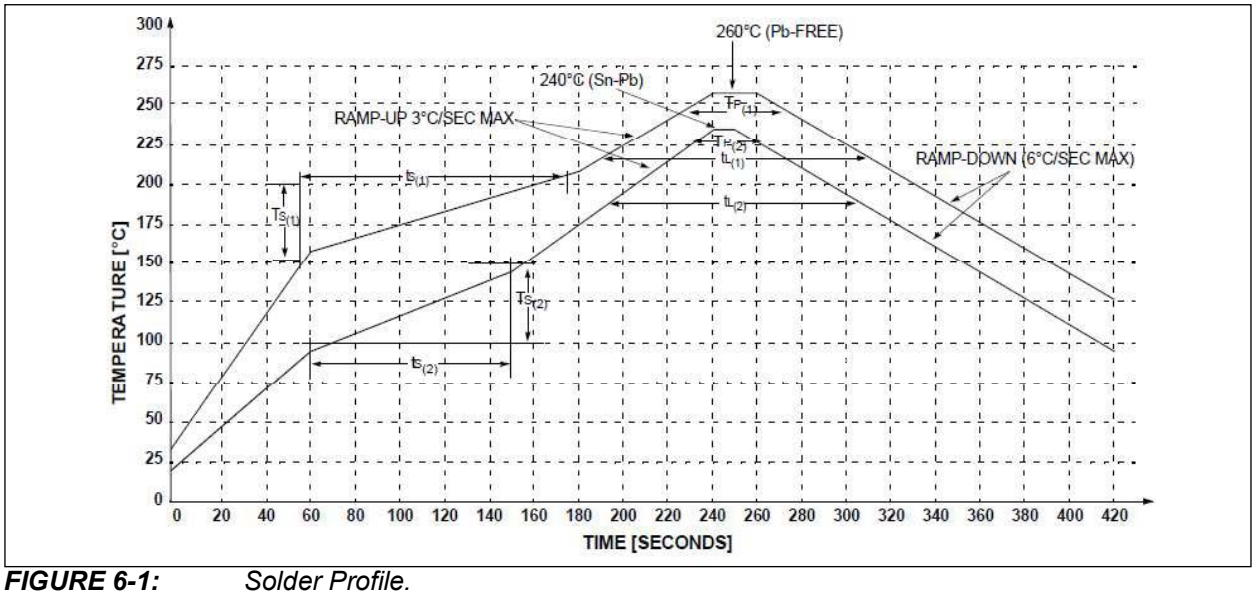


FIGURE 6-1: *Solder Profile.*

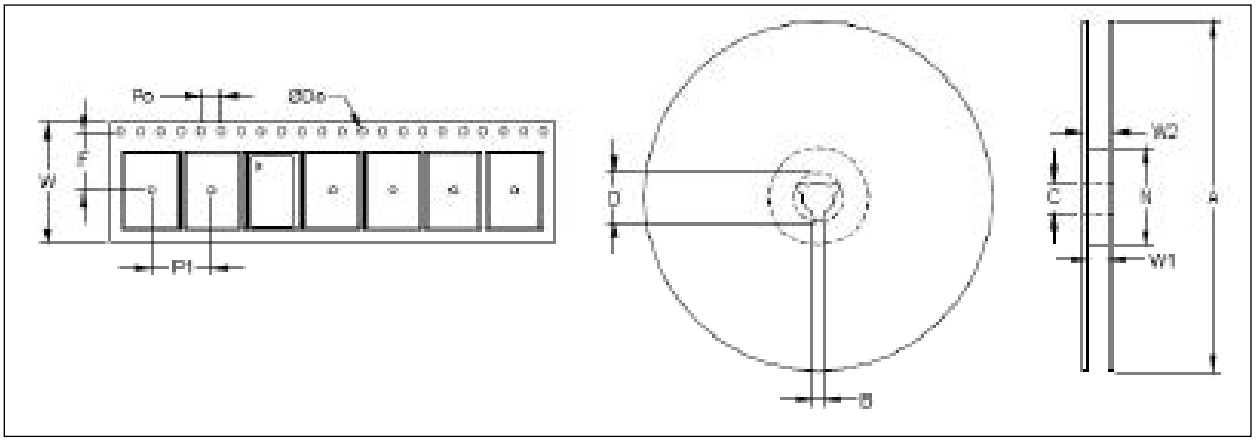
TABLE 6-1: REFLOW PROFILE

Symbol	Min.	Max.	Conditions
$Ts_{(1)}$	150°C	200°C	Pb-free Option
$Ts_{(2)}$	100°C	150°C	_SNPB Option
$ts_{(1)}$	60°C	180°C	Pb-free Option
$ts_{(2)}$	60°C	120°C	_SNPB Option
$tl_{(1)}$	60°C	150°C	Pb-free Option
$tl_{(2)}$	60°C	150°C	_SNPB Option
$Tp_{(1)}$	245°C	260°C	Pb-free Option
$Tp_{(2)}$	225°C	240°C	_SNPB Option

7.0 TAPE AND REEL

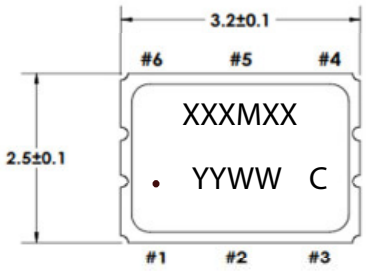
TABLE 7-1: TAPE AND REEL DIMENSIONS

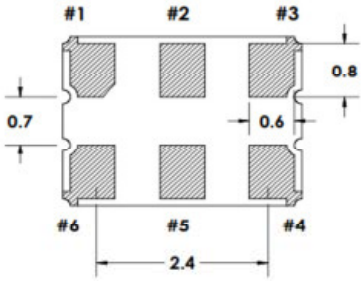
Tape Dimensions (mm)						Reel Dimensions (mm)							
Part No.	W	F	Do	Po	P1	A	B	C	D	N	W1	W2	# per Reel
VC-827	8	3.5	1.5	4	4	178	2	13	21	60	110	14	3000

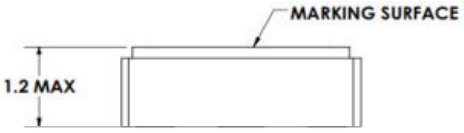


8.0 PACKAGING INFORMATION

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



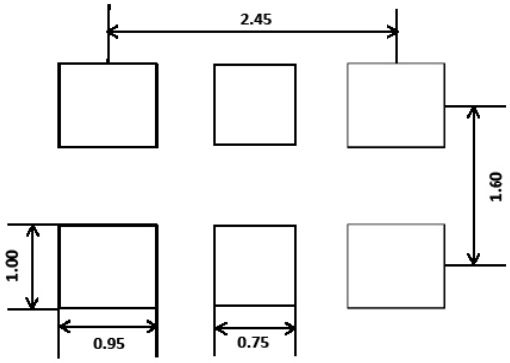




Dimensions in mm

Marking Information:
XXXMXX = Frequency (example: 100M00 = 100.000MHz and 10M000 = 10.000MHz)
YY = Year of Manufacture
WW = Week of the Year
C = Manufacturing Location
• = Pin 1 Indicator

Recommended Pad Layout



NOTES:

APPENDIX A: REVISION HISTORY

Revision A (April 2025)

- Converted Vectron data sheet VC-827 to Microchip document DS20007003A.
- Minor text edits throughout.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

Device	-X	X	X	-X	X	X	X	-XXXXXXXXXX	XX
Part No.	Voltage	Output	Temp. Range	Temp. Stability	Enable/Disable Logic	Enable/Disable Pin	Other (Future Use)	Frequency (in MHz)	Packaging

Device:	VC-827:		Crystal Oscillator in 3.2 mm x 2.5 mm Ceramic Package
Voltage:	E H J	= = =	3.3V ±5% 2.5V ±5% 1.8V ±5% (LVDS option only)
Output:	C D	= =	LVPECL LVDS
Temperature Range:	W E F	= = =	–10°C to +70°C –40°C to +85°C –40°C to +105°C
Temperature Stability:	F K S	= = =	±25 ppm ±50 ppm ±100 ppm
Enable/Disable Logic:	A	=	Output Enabled with a Logic High or Open. Output is Disabled with a Logic Low.
Enable/Disable Pin:	A B	= =	Pin 1 (Pin 2 = No Connection) Pin 2 (Pin 1 = No Connection)
Other (Future Use):	N	=	Standard
Frequency:	xxxMxxxxxx=Frequency in MHz (10 digits)		
Packaging:	TR <blank>= _SNPB=	= = =	Tape & Reel Cut Tape/ non-TR quantities Tin Lead Solder Dipped

Examples:

a) VC-827-ECE-SAAN-156M2500000TR

VC-827, 3.3V ±5%, LVPECL Output, –40°C to +85°C Temp. Range, ±100 ppm Stability, Output Enabled with a Logic High or Open, Pin 1 Enable/Disable, 156.25 MHz, Tape & Reel

b) VC-827-JDW-KABN-125M0000000

VC-827, 1.8V ±5%, LVDS Output, –10°C to +70°C Temp. Range, ±50 ppm Stability, Output Enabled with a Logic High or Open, Pin 2 Enable/Disable, 125 MHz, Cut Tape

c) VC-827-HCF-FAAN-200M0000000TR_SNPB

VC-827, 2.5V ±5%, LVPECL Output, –40°C to +105°C Temp. Range, ±25 ppm Stability, Output Enabled with a Logic High or Open, Pin 1 Enable/Disable, 200 MHz, Tape & Reel, Tin Lead Solder Dipped

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

Note: Not all combinations of options are available. Other specifications may be available upon request.

NOTES:

Microchip Information

Trademarks

The “Microchip” name and logo, the “M” logo, and other names, logos, and brands are registered and unregistered trademarks of Microchip Technology Incorporated or its affiliates and/or subsidiaries in the United States and/or other countries (“Microchip Trademarks”). Information regarding Microchip Trademarks can be found at https://www.microchip.com/en-us/about/legal-information/microchip-trademarks.

ISBN: 979-8-3371-1058-5

Legal Notice

This publication and the information herein may be used only with Microchip products, including to design, test, and integrate Microchip products with your application. Use of this information in any other manner violates these terms. Information regarding device applications is provided only for your convenience and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. Contact your local Microchip sales office for additional support or, obtain additional support at www.microchip.com/en-us/support/design-help/client-support-services.

THIS INFORMATION IS PROVIDED BY MICROCHIP "AS IS". MICROCHIP MAKES NO REPRESENTATIONS OR WARRANTIES OF ANY KIND WHETHER EXPRESS OR IMPLIED, WRITTEN OR ORAL, STATUTORY OR OTHERWISE, RELATED TO THE INFORMATION INCLUDING BUT NOT LIMITED TO ANY IMPLIED WARRANTIES OF NON-INFRINGEMENT, MERCHANTABILITY, AND FITNESS FOR A PARTICULAR PURPOSE, OR WARRANTIES RELATED TO ITS CONDITION, QUALITY, OR PERFORMANCE.

IN NO EVENT WILL MICROCHIP BE LIABLE FOR ANY INDIRECT, SPECIAL, PUNITIVE, INCIDENTAL, OR CONSEQUENTIAL LOSS, DAMAGE, COST, OR EXPENSE OF ANY KIND WHATSOEVER RELATED TO THE INFORMATION OR ITS USE, HOWEVER CAUSED, EVEN IF MICROCHIP HAS BEEN ADVISED OF THE POSSIBILITY OR THE DAMAGES ARE FORESEEABLE. TO THE FULLEST EXTENT ALLOWED BY LAW, MICROCHIP'S TOTAL LIABILITY ON ALL CLAIMS IN ANY WAY RELATED TO THE INFORMATION OR ITS USE WILL NOT EXCEED THE AMOUNT OF FEES, IF ANY, THAT YOU HAVE PAID DIRECTLY TO MICROCHIP FOR THE INFORMATION.

Use of Microchip devices in life support and/or safety applications is entirely at the buyer's risk, and the buyer agrees to defend, indemnify and hold harmless Microchip from any and all damages, claims, suits, or expenses resulting from such use. No licenses are conveyed, implicitly or otherwise, under any Microchip intellectual property rights unless otherwise stated.

Microchip Devices Code Protection Feature

Note the following details of the code protection feature on Microchip products:

- Microchip products meet the specifications contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is secure when used in the intended manner, within operating specifications, and under normal conditions.
- Microchip values and aggressively protects its intellectual property rights. Attempts to breach the code protection features of Microchip product is strictly prohibited and may violate the Digital Millennium Copyright Act.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of its code. Code protection does not mean that we are guaranteeing the product is “unbreakable”. Code protection is constantly evolving. Microchip is committed to continuously improving the code protection features of our products.