VC-806A

Crystal Oscillator

Features

- 13.5 MHz to 220 MHz Output Frequencies
- LVPECL, LVDS, or HCSL Output Logic
- 150 fs_{RMS} Typical Phase Jitter, 12 kHz to 20 MHz
- Extended Operating Temperature Range, –40°C to +125°C
- Excellent Power Supply Rejection Ratio
- Hermetically Sealed 5.0 mm x 3.2 mm Ceramic Package
- Product is Compliant to RoHS Directive and Fully Compatible with Lead Free Assembly (excluding solder dipped, _SNPB, option)

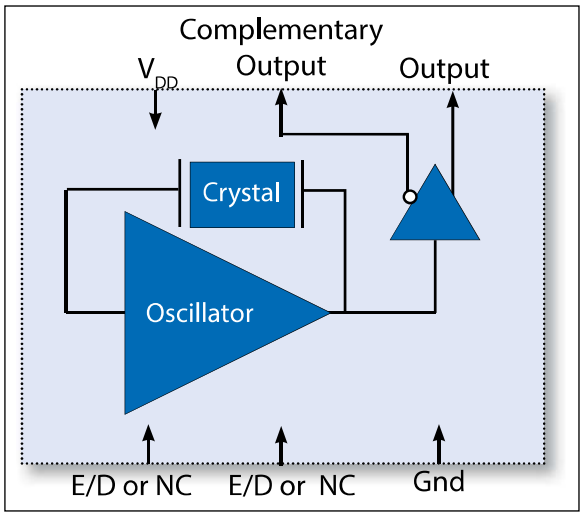
Applications

- Medical, Ultrasound
- Ethernet, GbE, SyncE
- Fibre Channel
- PON
- Clock Source for A/Ds, D/As, FPGAs
- Test and Measurement
- Storage Area Networking

General Description

The VC-806A crystal oscillator is a quartz-stabilized, differential output oscillator that operates off a 1.8V (LVDS and HCSL), 2.5V, or 3.3V supply in a hermetically sealed 5.0 mm x 3.2 mm ceramic package.

Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

ELECTRICAL PERFORMANCE, LVPECL OPTION

Parameter	Sym.	Min.	Typ.	Max.	Units	Conditions
Supply Voltage (Note 1)	V_{DD}	3.135	3.3	3.465	V	—
		2.375	2.5	2.625		—
Current (Note 2)	I_{DD}	—	—	50	mA	—
Frequency						
Nominal Frequency	f_{NOM}	13.5	—	220.0	MHz	—
Frequency Stability (Note 3)	f_{STAB}	—	—	±25	ppm	Ordering Option
		—	—	±35		
		—	—	±50		
		—	—	±100		
Outputs						
Output Logic Level High	V_{OH}	V_{DD} – 1.025	—	V_{DD} – 0.880	V	—
Output Logic Level Low	V_{OL}	V_{DD} – 1.810	—	V_{DD} – 1.650	V	—
Output Rise and Fall Time	t_R/t_F	—	—	400	ps	—
Load	—	50Ω into V_{DD} – 2.0V				—
Duty Cycle (Note 4)	DC	45	—	55	%	—
		40	—	60		at +125°C
Jitter, 156.250 MHz (Note 5)	Φ_J	—	—	200	fs	12 kHz to 50 MHz
		—	—	150		12 kHz to 20 MHz
		—	—	100		10 kHz to 1 MHz
Period Jitter, 156.250 MHz (Note 6)	Φ_J	—	1.1	2.2	ps	RMS
		—	10.5	21.0		Peak-to-peak
Cycle-to-Cycle Jitter (Note 6)	Φ_J	—	1.9	3.8	ps	RMS
		—	17.7	35.4		Peak-to-peak
Random Jitter (Note 6)	Φ_J	—	2.2	4.4	ps	—
Deterministic Jitter (Note 6)	Φ_J	—	0	—	ps	—
Enable/Disable						
Outputs Enabled (Note 7)	V_{IH}	0.7*V_{DD}	—	—	V	—
Outputs Disabled	V_{IL}	—	—	0.3*V_{DD}	V	—
Disable Time	t_{DIS}	—	—	200	ns	—

Note 1: The VC-806A power supply pin should be filtered (e.g. a 10 µF, 0.1 µF, and 0.01 µF capacitor).

2: Figure 1-1 defines the test circuit and Figure 1-2 defines these parameters.

3: Includes calibration tolerance, operating temperature, supply voltage variations, aging, and IR reflow.

4: Duty Cycle is defined as the On-Time divided by Period.

5: Measured using an Agilent E5052 Signal Source Analyzer at +25°C.

6: Measured using a Wavecrest SIA3300C, 90k samples.

7: Outputs will be enabled if Enable/Disable is left open. There is an oscillation detection circuit that ensures glitch free output upon power-up or enable.

ELECTRICAL PERFORMANCE, LVPECL OPTION (CONTINUED)

Parameter	Sym.	Min.	Typ.	Max.	Units	Conditions
Enable/Disable Leakage Current	$I_{E/D}$	—	—	±200	µA	—
Start-Up Time	t_{SU}	—	—	10	ms	—
Operating Temperature	T_{OP}	–10	—	+70	°C	Ordering Option
		–40	—	+85		
		–40	—	+105		
		–40	—	+125		

Note 1: The VC-806A power supply pin should be filtered (e.g. a 10 µF, 0.1 µF, and 0.01 µF capacitor).

2: Figure 1-1 defines the test circuit and Figure 1-2 defines these parameters.

3: Includes calibration tolerance, operating temperature, supply voltage variations, aging, and IR reflow.

4: Duty Cycle is defined as the On-Time divided by Period.

5: Measured using an Agilent E5052 Signal Source Analyzer at +25°C.

6: Measured using a Wavecrest SIA3300C, 90k samples.

7: Outputs will be enabled if Enable/Disable is left open. There is an oscillation detection circuit that ensures glitch free output upon power-up or enable.

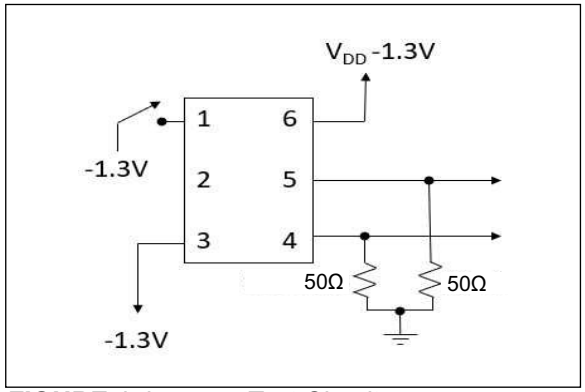


FIGURE 1-1: *Test Circuit.*

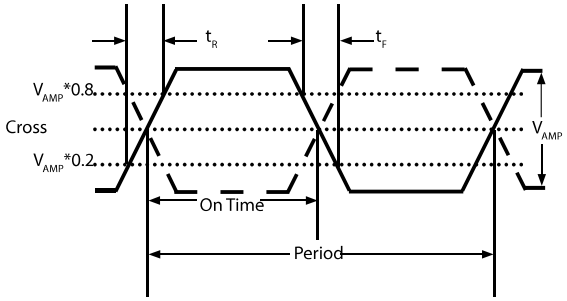


FIGURE 1-2: *Test Circuit Parameters.*

ELECTRICAL PERFORMANCE, LVDS OPTION

Parameter	Sym.	Min.	Typ.	Max.	Units	Conditions
Supply Voltage (Note 1)	V_{DD}	3.135	3.3	3.465	V	—
		2.375	2.5	2.625		
		1.71	1.8	1.89		
Current (Note 2)	I_{DD}	—	—	20	mA	—
Frequency						
Nominal Frequency	f_{NOM}	13.5	—	220.0	MHz	—
Frequency Stability (Note 3)	f_{STAB}	—	—	±25	ppm	Ordering Option
		—	—	±35		
		—	—	±50		
		—	—	±100		
Outputs						
Output Logic Level High	V_{OH}	—	1.43	1.6	V	—
Output Logic Level Low	V_{OL}	0.9	1.10	—	V	—
Output Amplitude	—	247	330	454	mV	—
Differential Output Error	—	—	—	50	mV	—
Offset Voltage	V_{OFF}	1.125	1.25	1.375	V	—
Offset Voltage Error	—	—	—	50	mV	—
Output Leakage Current	—	—	—	10	µA	Outputs Disabled
Output Rise and Fall Time (Note 3)	t_R/t_F	—	—	400	ps	3.3V, 2.5V
		—	—	500		1.8V
Load	—	100Ω Differential				—
Duty Cycle (Note 4)	DC	45	—	55	%	—
		40	—	60		at +125°C
Jitter, 156.250 MHz (Note 5)	Φ_J	—	—	200	fs	12 kHz to 50 MHz
		—	—	150		12 kHz to 20 MHz
		—	—	100		10 kHz to 1 MHz
Period Jitter, 156.250 MHz (Note 6)	Φ_J	—	1.1	2.2	ps	RMS
		—	10.5	21.0		Peak-to-peak
Cycle-to-Cycle Jitter (Note 6)	Φ_J	—	1.9	3.8	ps	RMS
		—	17.7	35.4		Peak-to-peak
Random Jitter (Note 6)	Φ_J	—	2.2	4.4	ps	—
Deterministic Jitter (Note 6)	Φ_J	—	0	—	ps	—

Note 1: The VC-806A power supply pin should be filtered (e.g. a 10 µF, 0.1 µF, and 0.01 µF capacitor).

2: Figure 1-3 defines the test circuit and Figure 1-2 defines these parameters.

3: Includes calibration tolerance, operating temperature, supply voltage variations, aging, and IR reflow.

4: Duty Cycle is defined as the On-Time divided by Period.

5: Measured using an Agilent E5052 Signal Source Analyzer at +25°C.

6: Measured using a Wavecrest SIA3300C, 90k samples.

7: Outputs will be enabled if Enable/Disable is left open. There is an oscillation detection circuit that ensures glitch free output upon power-up or enable.

ELECTRICAL PERFORMANCE, LVDS OPTION (CONTINUED)

Parameter	Sym.	Min.	Typ.	Max.	Units	Conditions
Enable/Disable						
Outputs Enabled (Note 7)	V_{IH}	0.7*V_{DD}	—	—	V	—
Outputs Disabled	V_{IL}	—	—	0.3*V_{DD}	V	—
Disable Time	t_{DIS}	—	—	200	ns	—
Enable/Disable Leakage Current	$I_{E/D}$	—	—	±200	µA	—
Start-Up Time	t_{SU}	—	—	10	ms	—
Operating Temperature	T_{OP}	–10	—	+70	°C	Ordering Option
		–40	—	+85		
		–40	—	+105		
		–40	—	+125		

Note 1: The VC-806A power supply pin should be filtered (e.g. a 10 µF, 0.1 µF, and 0.01 µF capacitor).

2: Figure 1-3 defines the test circuit and Figure 1-2 defines these parameters.

3: Includes calibration tolerance, operating temperature, supply voltage variations, aging, and IR reflow.

4: Duty Cycle is defined as the On-Time divided by Period.

5: Measured using an Agilent E5052 Signal Source Analyzer at +25°C.

6: Measured using a Wavecrest SIA3300C, 90k samples.

7: Outputs will be enabled if Enable/Disable is left open. There is an oscillation detection circuit that ensures glitch free output upon power-up or enable.

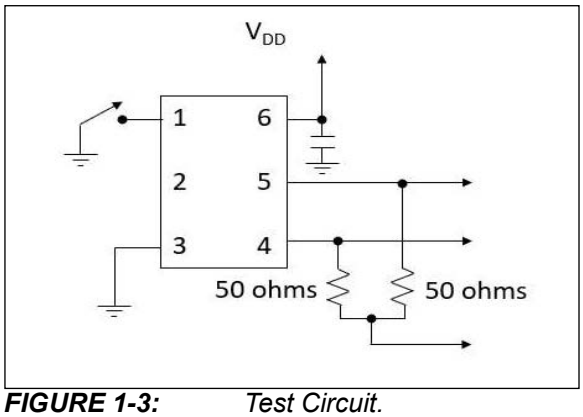


FIGURE 1-3: *Test Circuit.*

ELECTRICAL PERFORMANCE, HCSL OPTION

Parameter	Sym.	Min.	Typ.	Max.	Units	Conditions
Supply Voltage (Note 1)	V_{DD}	3.135	3.3	3.465	V	—
		2.375	2.5	2.625		
		1.71	1.8	1.89		
Current (Note 2)	I_{DD}	—	—	39	mA	—
Frequency						
Nominal Frequency	f_{NOM}	13.5	—	170.0	MHz	—
Frequency Stability (Note 3)	f_{STAB}	—	—	±25	ppm	Ordering Option
		—	—	±35		
		—	—	±50		
		—	—	±100		
Outputs						
Output High Voltage	V_{OH}	550	—	900	V	—
Output Low Voltage	V_{OL}	–150	—	150	V	—
Output Logic Swing, 3.3V	V_{OPP}	0.600	—	—	V	—
Output Logic Swing, 2.5V, 1.8V		0.500	—	—	V	—
Output Rise and Fall Time	t_R/t_F	—	—	600	ps	1.8V
		—	—	500	ps	2.5V or 3.3V
Load	—	50Ω to ground				—
Duty Cycle (Note 4)	DC	45	—	55	%	—
		40	—	60		at +125°C
Jitter, 100.000 MHz (Note 5)	Φ_J	—	—	300	fs	12 kHz to 20 MHz
Jitter, 100.000 MHz	Φ_J	PCIe Gen1 - Gen5 Compliant				—
Enable/Disable						
Outputs Enabled (Note 6)	V_{IH}	0.7*V_{DD}	—	—	V	—
Outputs Disabled	V_{IL}	—	—	0.3*V_{DD}	V	—
Disable Time	t_{DIS}	—	—	200	ns	—
Enable/Disable Leakage Current	$I_{E/D}$	—	—	±200	µA	—
Start-Up Time	t_{SU}	—	—	10	ms	—
Operating Temperature	T_{OP}	–10	—	+70	°C	Ordering Option
		–40	—	+85		
		–40	—	+105		
		–40	—	+125		

Note 1: The VC-806A power supply pin should be filtered (e.g. a 10 µF, 0.1 µF, and 0.01 µF capacitor).

2: Figure 1-4 defines the test circuit and Figure 1-5 defines these parameters.

3: Includes calibration tolerance, operating temperature, supply voltage variations, aging, and IR reflow.

4: Duty Cycle is defined as the On-Time divided by Period.

5: Measured using an Agilent E5052.

6: Outputs will be enabled if Enable/Disable pad is left open.

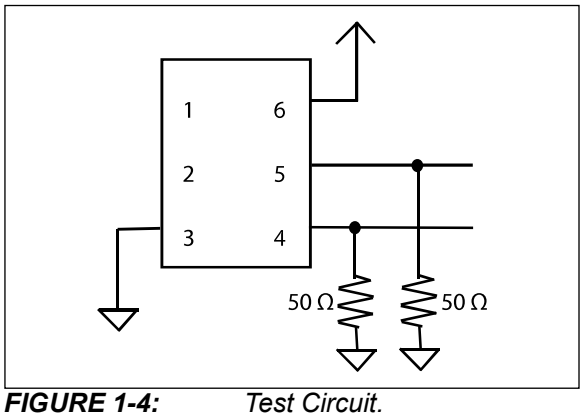


FIGURE 1-4: *Test Circuit.*

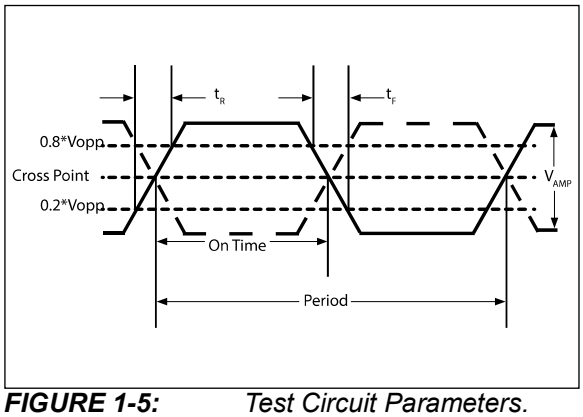


FIGURE 1-5: *Test Circuit Parameters.*

Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can permanently damage the device. Functional operation is not implied at these or any other conditions in excess of conditions represented in the operational sections of this data sheet. Exposure to absolute maximum ratings for extended periods may adversely affect device reliability.

Parameter	Symbol	Value
Storage Temperature	$T_{STORAGE}$	–55°C to +125°C
Supply Voltage	V_{DD}	–0.5V to +5.0V
Enable/Disable Voltage	$V_{E/D}$	–0.5V to V_{DD} + 0.5V

Handling Precautions

Although ESD protection circuitry has been designed into the VC-806A, proper precautions should be taken when handling and mounting. Microchip employs a Human Body Model and a Charged Device Model (CDM) for ESD susceptibility testing and design protection evaluation. ESD thresholds are dependent on the circuit parameters used to define the model. Although no industry standard has been adopted for the CDM, a standard HBM of resistance = 1.5 kΩ and capacitance = 100 pF is widely used and therefore can be used for comparison purposes.

TABLE 1-1: ESD RATINGS

Model	Minimum	Conditions
Human Body Model	1500V	—
Charged Device Model	1500V	—

2.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 2-1 and the optional Enable/Disable function is detailed in Table 2-2.

TABLE 2-1: PIN FUNCTION TABLE

Pin Number	Pin Name	Description
1	E/D or NC	Enable/Disable or No Connection. Note 1
2	E/D or NC	Enable/Disable or No Connection. Note 1
3	GND	Electrical and Lid Ground.
4	f_O	Output Frequency.
5	Cf_O	Complementary Output Frequency.
6	V_{DD}	Supply Voltage.

Note 1: E/D can be provided on either Pin 1 or Pin 2.

TABLE 2-2: ENABLE/DISABLE FUNCTION (OPTIONAL)

Pin 1 or 2	Pin 4, 5 Output
High	Clock Output
Open	Clock Output
Low	High Impedance

3.0 RELIABILITY

TABLE 3-1: ENVIRONMENTAL COMPLIANCE

Parameter	Conditions
Mechanical Shock	MIL-STD-883, Method 2002
Mechanical Vibration	MIL-STD-883, Method 2007
Temperature Cycle	MIL-STD-883, Method 1010
Solderability	MIL-STD-883, Method 2003
Fine and Gross Leak	MIL-STD-883, Method 1014
Resistance to Solvents	MIL-STD-883, Method 2015
Moisture Sensitivity Level	MSL1
Contact Pads	Gold over nickel
Contact Pads (_SNPB Option)	Tinned using Sn63Pb37 solder alloy in accordance with J-STD-006
Weight	57 mg

4.0 LVPECL APPLICATION DIAGRAMS

The VC-806A incorporates a standard PECL output scheme, which are unterminated FET drains. There are numerous application notes on terminating and interfacing PECL logic. The two most common methods are a single resistor to ground (Figure 4-1) and a pull-up/pull-down scheme (Figure 4-2). AC-coupling capacitors are optional, depending on the application and the input logic requirements of the next stage.

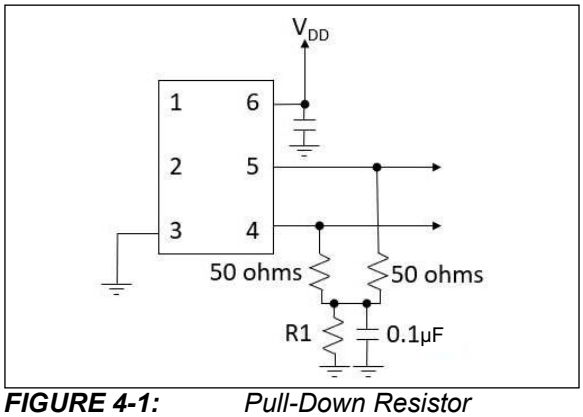


FIGURE 4-1: *Pull-Down Resistor Termination Scheme.*

Figure 4-1 shows one option to terminate LVPECL outputs and is optimized to reduce common mode noise. R1 is 50Ω for 3.3V supply voltage and 18Ω for 2.5V.

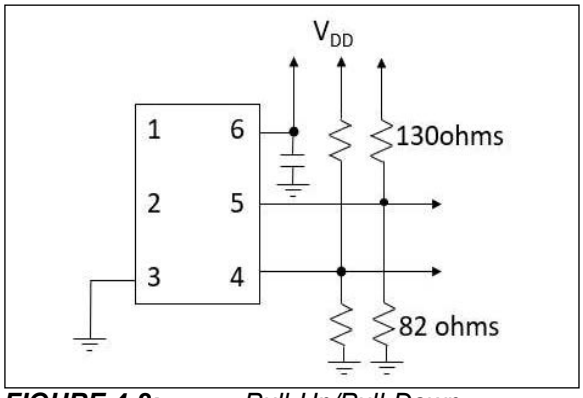


FIGURE 4-2: *Pull-Up/Pull-Down Termination Scheme.*

Resistor values shown are typical for 3.3V operation. For 2.5V operation, the resistor to ground is 62Ω and the resistor to supply is 250Ω. AC-blocking capacitors can be used if the DC levels are incompatible with the receiver input.

5.0 LVDS APPLICATION DIAGRAMS

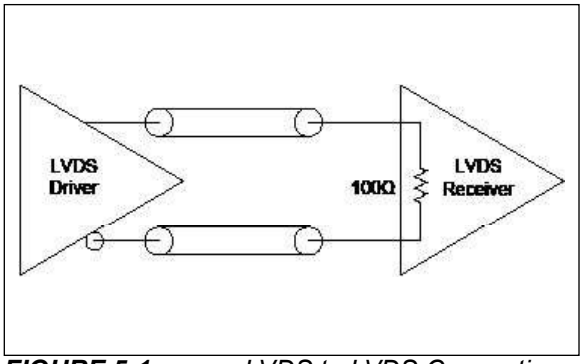


FIGURE 5-1: *LVDS to LVDS Connection, Internal 100Ω Resistor.*

Some LVDS structures have an internal 100Ω resistor on the input and do not need additional components. AC-blocking capacitors can be used if the DC levels are incompatible.

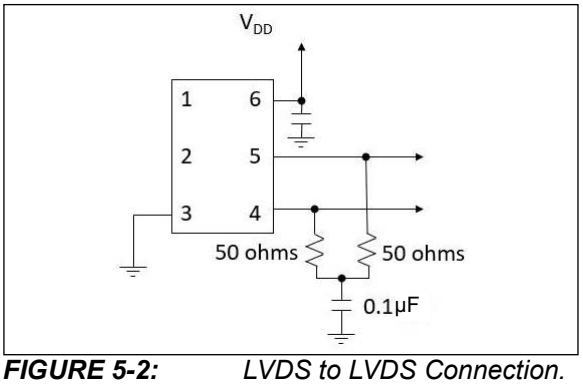


FIGURE 5-2: *LVDS to LVDS Connection.*

Some input structures might not have an internal 100Ω resistor on the input and will need an external 100Ω resistor at the receiver for impedance matching. Also, the input may have an internal DC bias that may not be compatible with LVDS levels. AC-blocking capacitors can be used.

6.0 HCSL APPLICATION DIAGRAMS

The VC-806A incorporates a High Speed Current Steering Logic (HCSL) output scheme that is a 15 mA current source between the Output and Complementary Output. Being unterminated drains, as shown in Figure 6-1, they require external 50Ω resistors to ground as shown in Figure 6-2. HCSL is a high impedance output with quick switching times. It can be advantageous to use a 10Ω to 30Ω series resistor as shown in Figure 6-3 to help reduce overshoot/ringing.

One of the most important considerations is terminating the Output and Complementary Output equally. An unused output should not be left unterminated, and if one of the two outputs is left open, it will result in excessive jitter on both. PCB layout must take this and 50Ω impedance matching into account. Load matching and power supply noise are the main contributors to jitter related problems.

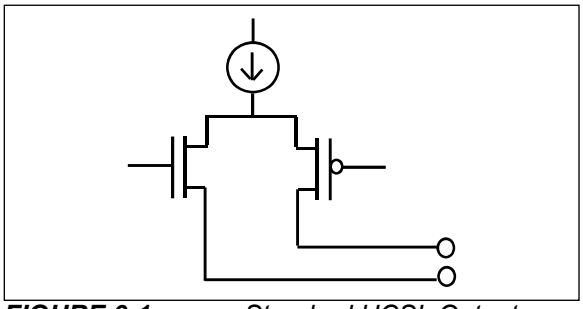


FIGURE 6-1: *Standard HCSL Output Configuration.*

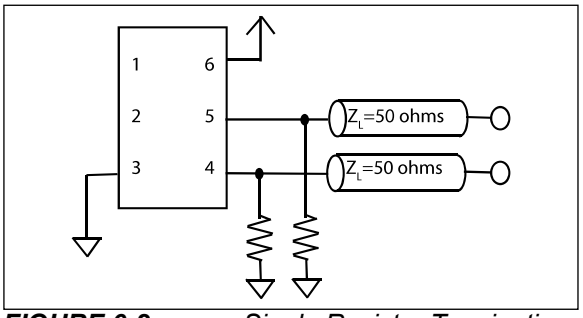


FIGURE 6-2: *Single Resistor Termination Scheme.*

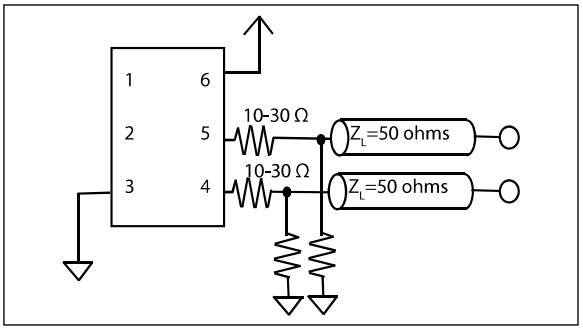


FIGURE 6-3: *Reducing Overshoot with 10Ω to 30Ω Series Resistors.*

7.0 IR REFLOW

The VC-806A is built using lead-free epoxy and can be subjected to standard lead-free IR reflow conditions shown in Table 7-1. Lower maximum temperatures can also be used, such as 220°C.

Note: Devices that have been solder dipped, _SNPB option, are not Pb-free.

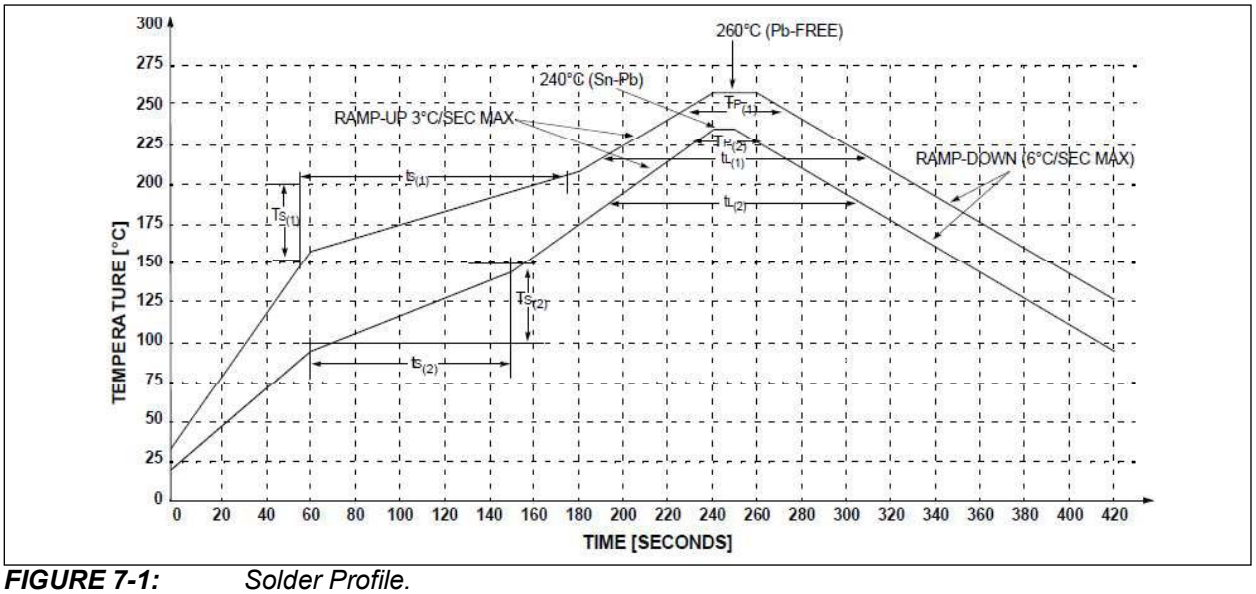


FIGURE 7-1: *Solder Profile.*

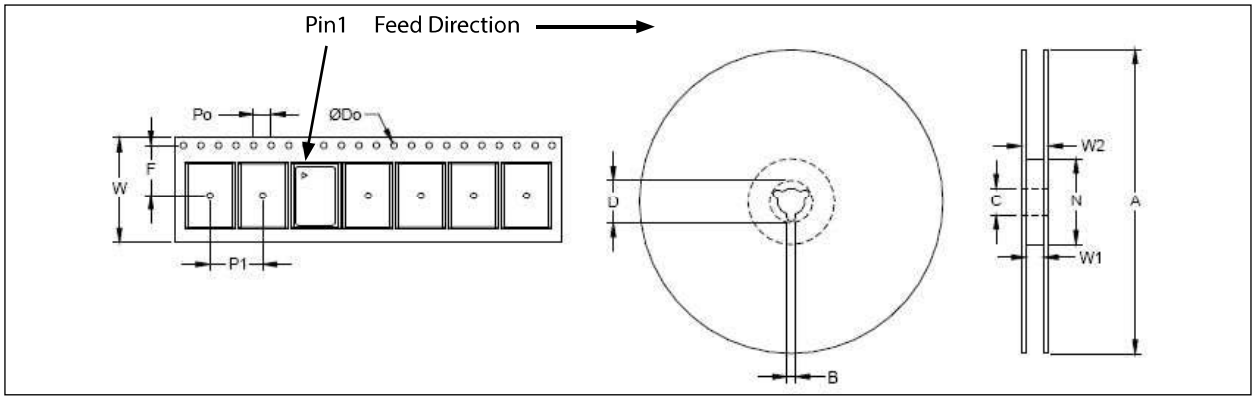
TABLE 7-1: REFLOW PROFILE

Symbol	Min.	Max.	Conditions
$Ts_{(1)}$	150°C	200°C	Pb-free Option
$Ts_{(2)}$	100°C	150°C	_SNPB Option
$ts_{(1)}$	60°C	180°C	Pb-free Option
$ts_{(2)}$	60°C	120°C	_SNPB Option
$tl_{(1)}$	60°C	150°C	Pb-free Option
$tl_{(2)}$	60°C	150°C	_SNPB Option
$Tp_{(1)}$	245°C	260°C	Pb-free Option
$Tp_{(2)}$	225°C	240°C	_SNPB Option

8.0 TAPE AND REEL

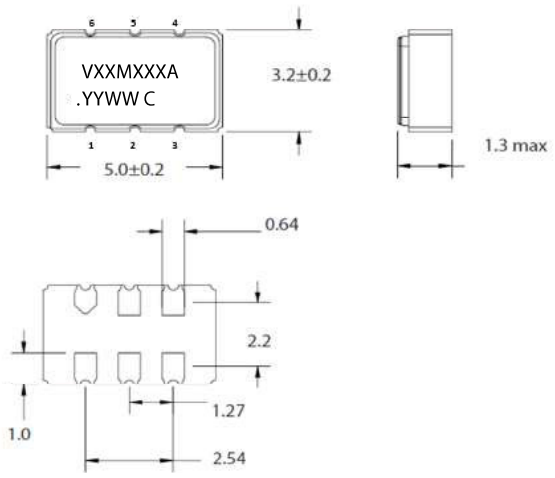
TABLE 8-1: TAPE AND REEL DIMENSIONS

Tape Dimensions (mm)						Reel Dimensions (mm)							
Part No.	W	F	Do	Po	P1	A	B	C	D	N	W1	W2	# per Reel
VC-806A	12	5.5	1.5	4	8	180	2	13	21	60	13	15.4	1000

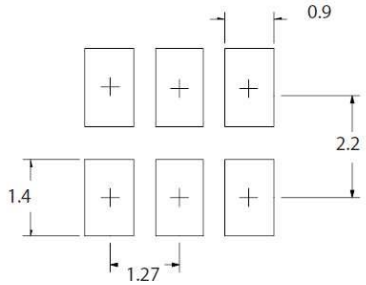


9.0 PACKAGING INFORMATION

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Dimensions in mm



Marking Information:
V: Vectron
XXMXX: Frequency in MHz (Example: 25M000 or 125M00)
A: VC-806A version
YYWW: Year and Week (2242: Year 2022 and Week 42)
C: Manufacturing Location

APPENDIX A: REVISION HISTORY

Revision A (April 2025)

- Initial release of the VC-806A data sheet as Microchip document DS20007002A.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

Device	-X	X	X	-X	X	X	X	-XXXXXXXXXX	XX
Part No.	Voltage	Output	Temp. Range	Temp. Stability	Enable/Disable Logic	Enable/Disable Pin	Other (Future Use)	Frequency (in MHz)	Packaging

Device:	VC-806A:		Crystal Oscillator in 5.0 mm x 3.2 mm Ceramic Package
Voltage:	E	=	3.3V ±5%
	H	=	2.5V ±5%
	J	=	1.8V ±5%
Output:	C	=	LVPECL
	D	=	LVDS
	H	=	HCSL
Temperature Range:	W	=	–10°C to +70°C
	E	=	–40°C to +85°C
	F	=	–40°C to +105°C
	G	=	–40°C to +125°C
Temperature Stability:	F	=	±25 ppm
	H	=	±35 ppm
	K	=	±50 ppm
	S	=	±100 ppm
Enable/Disable Logic:	A	=	Output Enabled with a Logic High or Open
Enable/Disable Pin:	A	=	Pin 1 (Pin 2 = No Connection)
	B	=	Pin 2 (Pin 1 = No Connection)
Other (Future Use):	N	=	Standard
Frequency:	xxxMxxxxxx=Frequency in MHz (10 digits)		
Packaging:	TR	=	Tape & Reel
	<blank>=		Cut Tape/ non-TR quantities
	_SNPB=		Tin Lead Solder Dipped

Examples:

a) VC-806A-ECE-FABN-32M00000000TR

VC-806A, 3.3V ±5%, LVPECL Output, –40°C to +85°C Temp. Range, ±25 ppm Stability, Output Enabled with a Logic High or Open, Pin 2 Enable/Disable, 32 MHz, Tape & Reel

b) VC-806A-HHG-KAAN-100M0000000

VC-806A, 2.5V ±5%, HCSL Output, –40°C to +125°C Temp. Range, ±50 ppm Stability, Output Enabled with a Logic High or Open, Pin 1 Enable/Disable, 100 MHz, Cut Tape

c) VC-806A-JDF-HABN-125M5000000TR_SNPB

VC-806A, 1.8V ±5%, LVDS Output, –40°C to +105°C Temp. Range, ±35 ppm Stability, Output Enabled with a Logic High or Open, Pin 2 Enable/Disable, 125.50 MHz, Tape & Reel, Tin Lead Solder Dipped

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

Note: Not all combinations of options are available. Other specifications may be available upon request.

NOTES:

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