

## SPI Communication with the AR1020 Controller

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### INTRODUCTION

The AR1020 controller's SPI (Serial Peripheral Interface) communicates as a slave mode device with 3-5 interface pins.

### INTERFACE PIN FUNCTIONALITY

**SCK "Serial Clock"** – The AR1020 controller's SCL/SCK/TX pin receives Serial Clock (SCK), controlled by the host.

- The Idle state of the SCK should be low.
- Data is transmitted on the falling edge of SCK.

**SDI "Serial Data In"** – The AR1020 controller's SDI/SDA/RX pin reads Serial Data Input (SDI), sent by the host.

**SDO "Serial Data Out"** – The AR1020 controller's SDO pin presents Serial Data Output (SDO) to the host.

**SIQ "SPI Interrupt"** – The AR1020 controller's SIQ pin provides an OPTIONAL interrupt output from the controller to the host.

- The SIQ pin is asserted high when the controller has data available (a touch report or a command response) for the host.
- The SIQ pin is de-asserted after the host clocks out the first byte of the data packet.

**SS "Slave Select"** – The AR1020 controller's SS pin provides OPTIONAL "Slave Select" functionality.

- The AR1020 controller is SPI selected (active) when the SS pin is host driven to the controller's Vss level.
- The AR1020 controller's SPI is deselected (inactive) when the SS pin is host driven to the controller's VDD level. In this state, the controller's SDO pin presents a high impedance in order to prevent bus contention with another device on the SPI bus.
- If host control over "selecting" the AR1020 controller is not desired, then the SS pin should be hardware connected to the controller's Vss level.

**TABLE 1: PIN VOLTAGE LEVEL CHARACTERISTICS<sup>(1)</sup>**

Function	Pin	Input	Output
SCK	SCL/SCK/TX	$V_{SS} \leq V_{IL} \leq 0.2 \cdot V_{DD}$ $0.8 \cdot V_{DD} \leq V_{IH} \leq V_{DD}$	—
SDI	SDI/SDA/RX	$V_{SS} \leq V_{IL} \leq 0.2 \cdot V_{DD}$ $0.8 \cdot V_{DD} \leq V_{IH} \leq V_{DD}$	—
SDO	SDO	—	$V_{SS} \leq V_{OL}^{(2)} \leq (1.2V - 0.15 \cdot V_{DD}^{(3)})$ $(1.25 \cdot V_{DD} - 2.25V)^{(4)} \leq V_{OH}^{(1)} \leq V_{DD}$
SS	SS	$V_{SS} \leq V_{IL} \leq 0.2 \cdot V_{DD}$ $0.8 \cdot V_{DD} \leq V_{IH} \leq V_{DD}$	—

- Note 1:** Operating voltage:  $3.15V \leq V_{DD} \leq 5.25V$   
**2:** These parameters are characterized but not tested.  
**3:** At 10 mA.  
**4:** At -4 mA.

## DATA FLOW

SPI data is transferred by the host clocking the AR1020 controller's Serial Clock (SCK) pin.

Each host driven clock cycle simultaneously shifts a bit of data into and out from the AR1020 controller.

- Out from the AR1020 controller's Serial Data Out (SDO) line.
- Into the AR1020 controller's Serial Data In (SDI) line.

The data is shifted Most Significant bit (MSb) first.

If the host clocks data out from the AR1020 controller when no valid data is available, then a byte value of 0x4d will be presented by the controller.

## TOUCH REPORT PROTOCOL

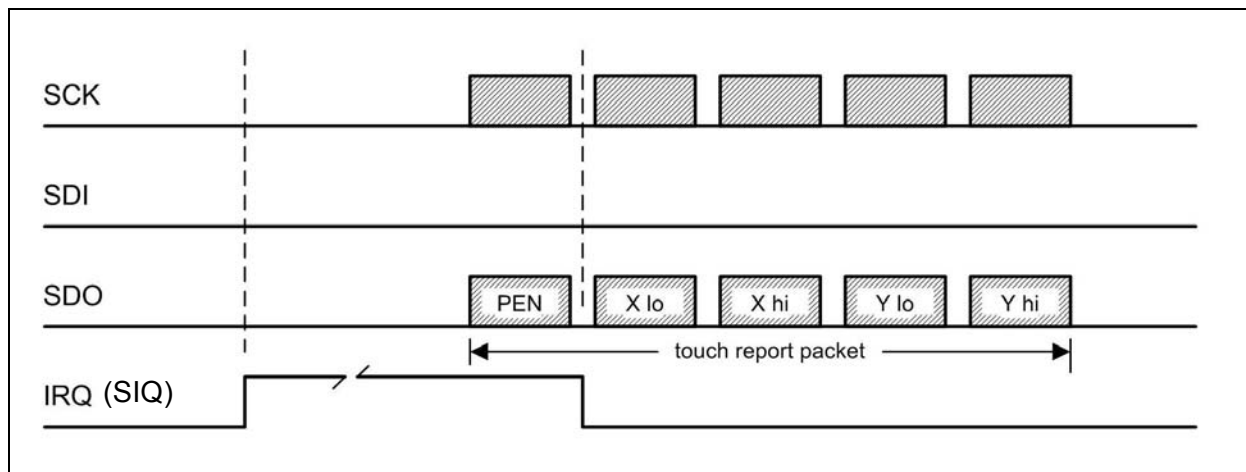
The AR1020 controller's touch reporting is interrupt driven.

1. The AR1020 controller asserts the SIQ interrupt pin high when a touch report is ready.
2. The host clocks out the bytes of the touch report packet from the AR1020 controller.

The AR1020 controller clears the SIQ interrupt pin low, after the first byte of the touch report packet has been clocked out by the host.

The communication protocol for the AR1020 controller reporting touches to the host is shown in Figure 1.

**FIGURE 1: AR1020 COMMUNICATION PROTOCOL**



## COMMAND PROTOCOL

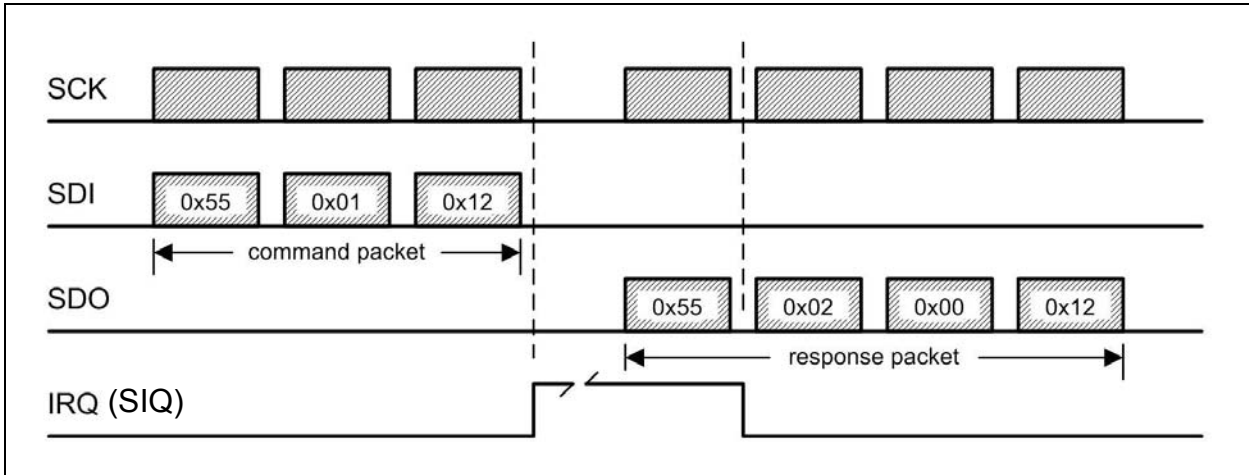
The AR1020 controller receives commands from the host as follows:

1. The host clocks the bytes of a command to the AR1020 controller.
2. The AR1020 controller asserts the SIQ interrupt pin high when it is ready with a response to the command sent by the host.
3. The host clocks out the bytes of the command response from the AR1020 controller.

The AR1020 controller clears the SIQ interrupt pin low, after the first byte of the command response has been clocked out by the host.

The communication protocol for the host sending a command to the AR1020 controller is shown in Figure 2.

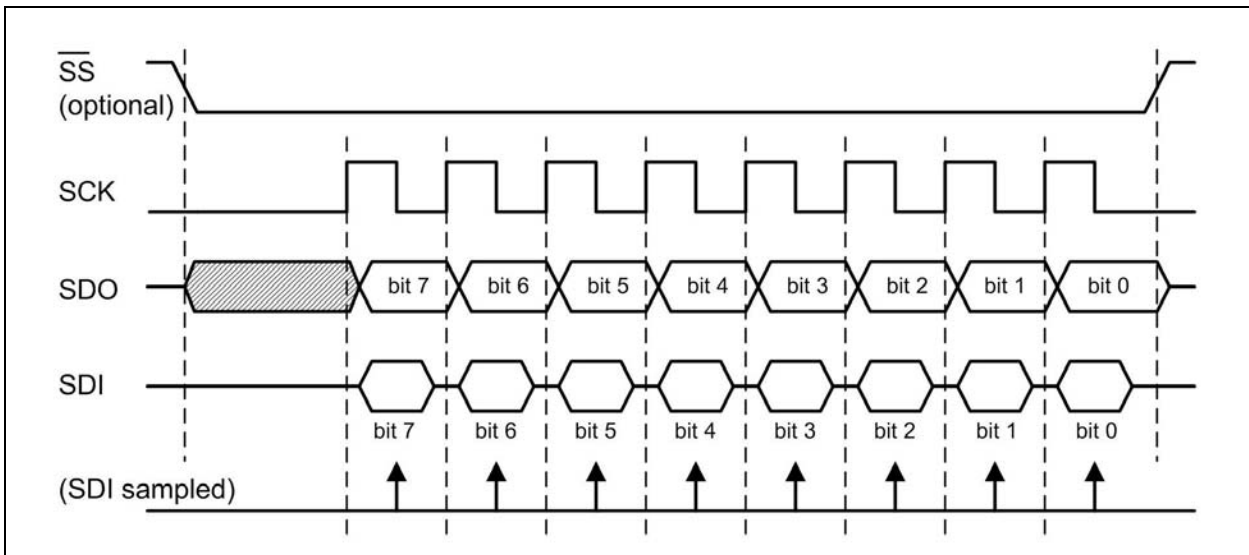
**FIGURE 2: COMMAND PROTOCOL FOR HOST SENDING A COMMAND**



## TIMING – GENERAL WAVEFORM

General timing waveforms are shown in Figure 3.

**FIGURE 3: GENERAL TIMING WAVEFORMS**



# TB3063

## TIMING – BIT DETAILS

### Bit Rate

The SPI standard does not specify a maximum data rate for the serial bus. In general, SPI data rates can be in the MHz. Peripherals devices, such as the AR1020 controller, specify their own unique maximum SPI data rates.

The maximum SPI bit rate for the AR1020 controller is ~900 KHz.

Characterization has been performed at bit rates of ~39 KHz and ~156 KHz.

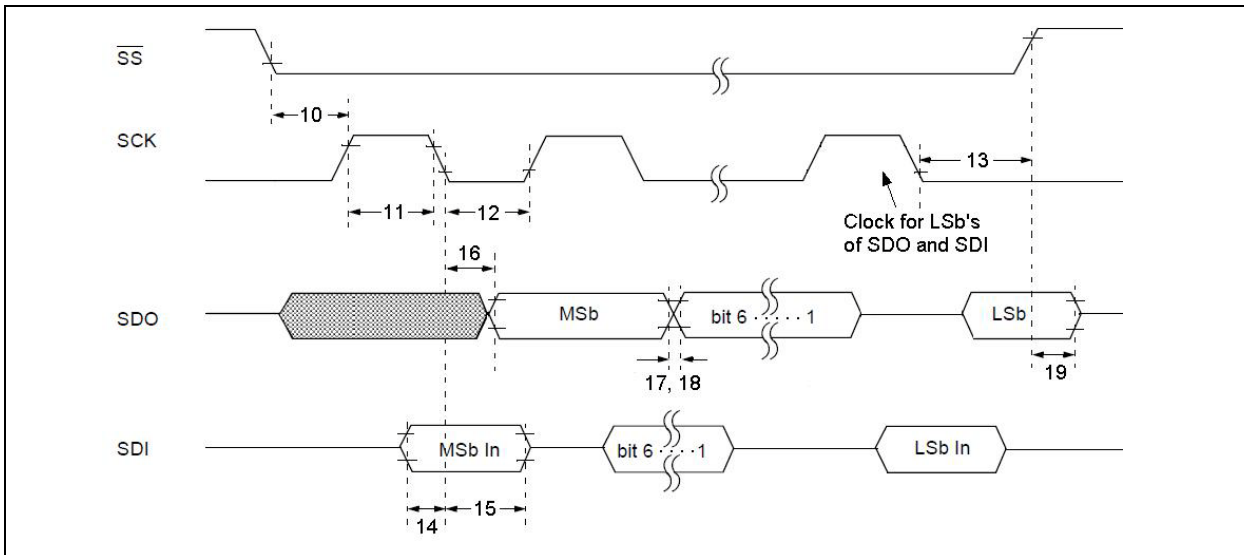
### Inter-Byte Delay

The AR1020 controller requires an inter-byte delay of ~50 us. This means the host should wait ~50 us between the end of clocking a given byte, and the start of clocking the next byte.

### Characterized Timing

Characterized timing details are shown in Figure 4 and Table 2.

**FIGURE 4: CHARACTERIZED TIMING DETAILS**



**TABLE 2: CHARACTERIZED TIMING DETAILS**

Parameter Number <sup>(1)</sup>	Parameter Description	Minimum	Maximum	Units
10	SS ↓ (select) to SCK ↑ (initial)	500	—	ns
11	SCK high	550	—	ns
12	SCK low	550	—	ns
13	SCK ↓ (last) to SS ↑ (deselect)	800	—	ns
14	SDI setup before SCK↓	100	—	ns
15	SDI hold after SCK↓	100	—	ns
16	SDO valid after SCK↓	—	150	ns
17	SDO↑ rise	—	50	ns
18	SDO↓ fall	—	50	ns
19	SS↑ (deselect) to SDO Hi-z	10	50	ns

**Note 1:** Parameters are characterized, but not tested.

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