

# Application Note

## PL671 – Spread Spectrum Modulation

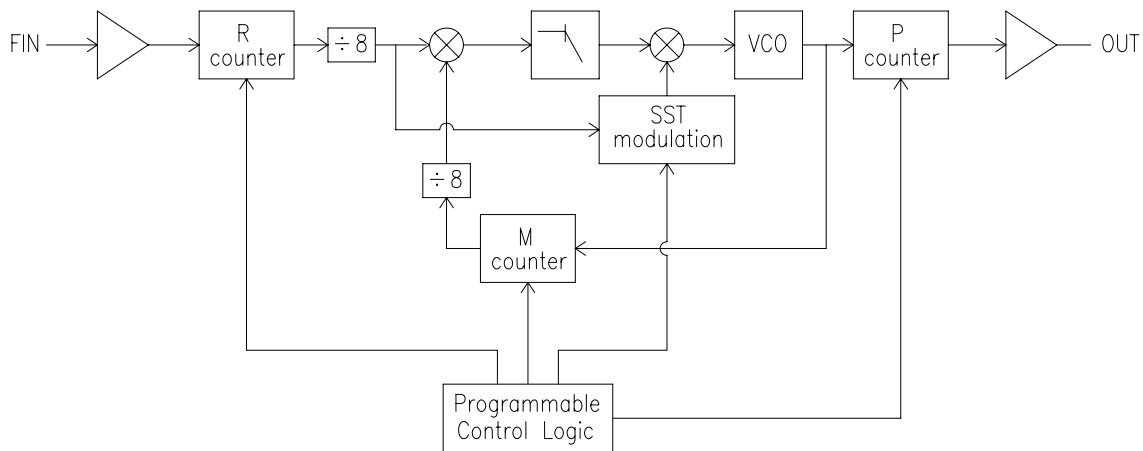
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The PL671 series of chips has programmable spread spectrum modulation for EMI reduction. The triangular modulation (“SST”) will spread the power of the output carrier and its harmonics, effectively lowering the peak power observed in the whole spectrum.

PL671 block diagram:



In essence the PL671 is a phase locked loop that transfers a certain input frequency into a certain output frequency, depending upon settings in the programmable control logic. The formula for the frequency conversion is as follows:

$$F_{out} = F_{in} \times M / (P \times R)$$

$F_{out}$ : Output Center Frequency

$F_{in}$ : Input reference frequency

M, P, R: Counter settings

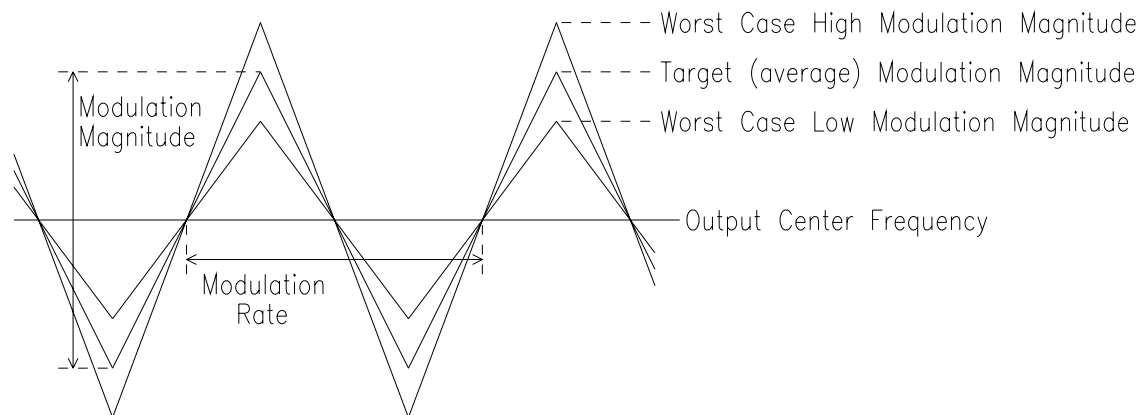
The output center frequency has the same accuracy and stability as the input frequency because the frequency conversion is perfect. The phase locked loop will keep the center output frequency at exactly  $M/(P \times R)$  ratio from the input frequency.

The spread spectrum modulation is introduced in the VCO in such a way that it is invisible to the phase locked loop. This is done by making the modulation rate the same

as the PLL phase detector sampling frequency. Every time the phase detector updates the VCO frequency, the modulation is passing through the center.

When measuring the frequency of a signal with SST modulation with a frequency counter, the measured value will be the output center frequency as it is the average frequency of the output signal. This is provided the frequency counter gate time is long enough for good averaging.

### Modulation Waveform:



The PLL maintains the output center frequency at exactly  $F_{in} \times M / (P \times R)$ .

As mentioned above the modulation rate is the same as the PLL phase detector sampling frequency:

$$\text{Modulation Rate} = F_{in} / (R \times 8)$$

The modulation magnitude can be set through programming in the range  $\pm 0.125\%$  to  $\pm 2.0\%$  with  $\pm 0.125\%$  steps.

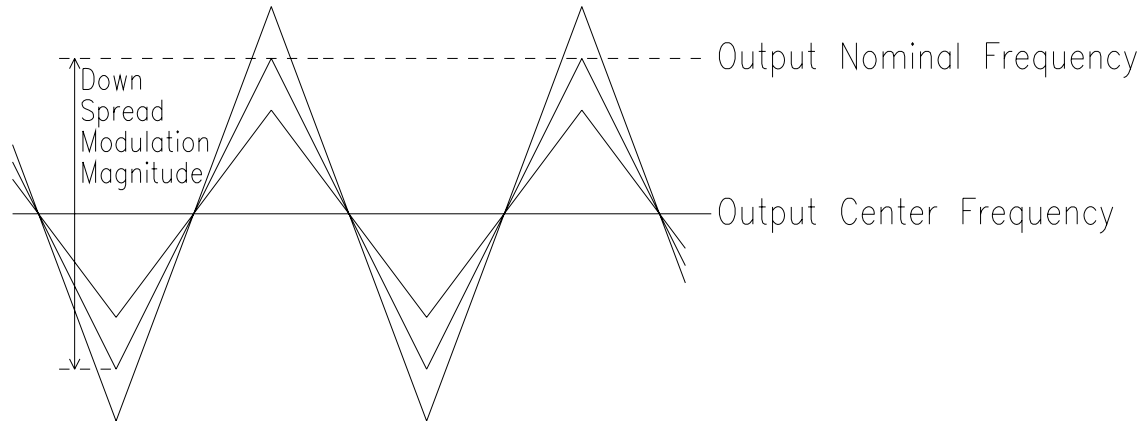
The input to output frequency conversion and the modulation rate accuracy depend only upon the input frequency accuracy. The SST modulator is an analog circuit and therefore dependent upon process spread. The worst case “raw” modulation magnitude variation is  $\pm 30\%$  from the target setting. This means for example that a target magnitude setting for  $\pm 1.0\%$  can result in devices with a worst case low magnitude of  $\pm 0.7\%$  and devices with a worst case high magnitude of  $\pm 1.3\%$ .

For applications that require a tighter controlled modulation magnitude there is a calibration procedure. The PL671 is first programmed to a specific configuration during the production final test. The final test measures the default modulation magnitude and then programs certain bits to fine tune the magnitude closer to the intended target. This way a tighter magnitude tolerance can be achieved of  $\pm 20\%$  or  $\pm 15\%$ . Final test limits will assure that no device is shipped with a modulation magnitude outside the desired tolerance.

## Down Spread

The above modulation waveform describes “Center Spread” where the output frequency sweeps symmetrically around a certain output center frequency. If the center frequency happens to be the application maximum frequency then half the time, when the output frequency is in the top half of the modulation cycle, the output frequency is too high. The answer to this problem is “down spread” where the modulation only sweeps down from a certain desired output nominal frequency.

### Down spread modulation wave form:



Technically the PL671 can only generate modulation symmetrically around a certain output center frequency. However, this center frequency can be chosen more or less freely by setting certain counter values. So we can effectively make down spread by choosing an output center frequency that is half the modulation magnitude below the desired output nominal frequency.

Lets take for example an output nominal frequency of 100MHz with -1.0% down spread. To achieve this we set an output center frequency 0.5% below 100MHz, at 99.5MHz and set the modulation magnitude to  $\pm 0.5\%$ . This way the modulation sweeps from  $99.5\text{MHz} - 0.5\% = 99.0\text{MHz}$  (= 1.0% below 100MHz) to  $99.5\text{MHz} + 0.5\% = 100.0\text{MHz}$ .

The output center frequency is accurately set through synthesis from the input frequency. The highest peaks of the triangular modulation will have the additional process spread from the modulation magnitude and will be less accurate. Assuming  $\pm 20\%$  tolerance on the modulation magnitude, the highest peaks of the modulation go up to  $99.5\text{MHz} + 0.6\% = 100.1\text{MHz}$  which is 0.1% above the 100MHz nominal output frequency.

## Appendix 1: PL671-29-A58, Specific case for Foxconn

Input frequency is 65MHz with  $\pm 50$ ppm tolerance

Desired output frequency is 65MHz with -0.75% down spread.

Configuration: R=258, M=1028, P=4.

Modulation Rate =  $65,000 / (258 \times 8) = 31.492\text{KHz}$

Output center frequency =  $65.0000 \times 1028 / (258 \times 4) = 64.748062\text{MHz}$

The expected output center frequency is  $65 - 0.75\%/2 = 64.756250\text{MHz}$

So the actual output center frequency is at  $65\text{MHz} - 0.3876\%$  instead of the expected  $65\text{MHz} - 0.3750\%$ . This is 8.188KHz lower.

With a  $\pm 20\%$  tolerance on the modulation magnitude the worst case high peak of the triangular modulation reaches up to:

$64.748062 + (0.375\%) \times 1.2 = 64.748062 + 0.450\% = 65.039428\text{MHz}$  or 0.06% above 65MHz.

The tolerance of  $\pm 50$ ppm on the input frequency influences the output center frequency:

At -50ppm the input frequency is 64.996750MHz and the output center frequency is  $64.996750 \times 1028 / (258 \times 4) = 64.744825\text{MHz}$ . This is 11.425KHz lower than the expected output center frequency.

At +50ppm the input frequency is 65.003250MHz and the output center frequency is  $65.003250 \times 1028 / (258 \times 4) = 64.751299\text{MHz}$ . This is 4.951KHz lower than the expected output center frequency.