PL611-01-F93 Power Supply Decoupling

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Author: Eddy van Keulen

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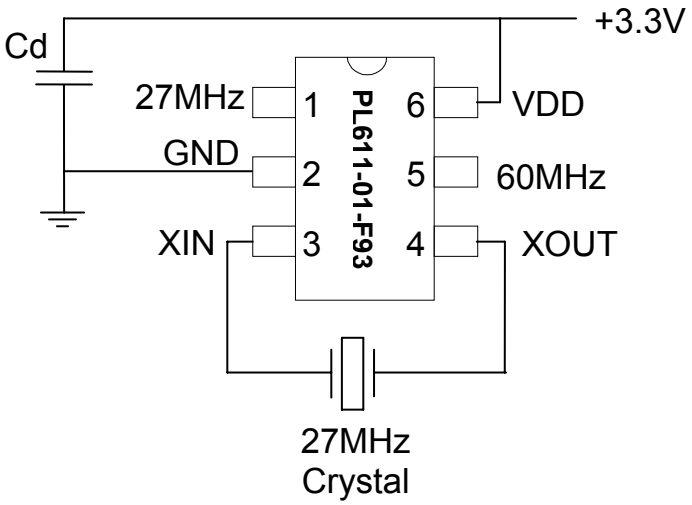
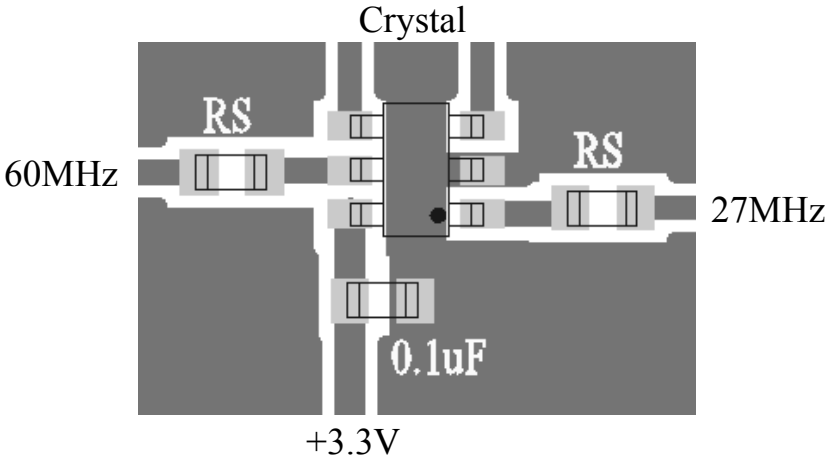
The PL611-01-F93TC is a small programmable PLL chip with one 27MHz output and one 60MHz output. The input reference is a 27MHz crystal.



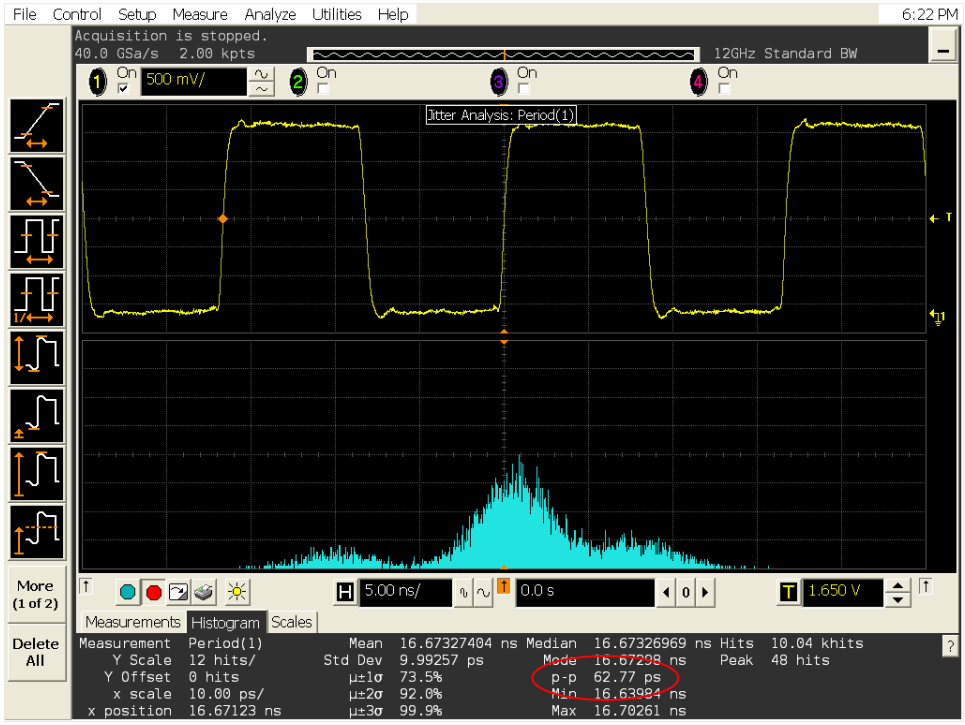
The 60MHz output is synthesized from 27MHz using a PLL circuit and the noise properties of the 60MHz output depend a lot upon the impedance of the power supply line. When the power supply impedance is not low enough, signals in the chip can cross-talk through the power lines causing larger period jitter on the 60MHz output. The power supply impedance can be minimized by placing a decoupling capacitor (Cd) right next to the PL611-01-F93TC between the VDD and GND pins.

The best location for the decoupling capacitor is next to the VDD pin. In the picture below you can see an example placement of a 0.1µF decoupling capacitor.



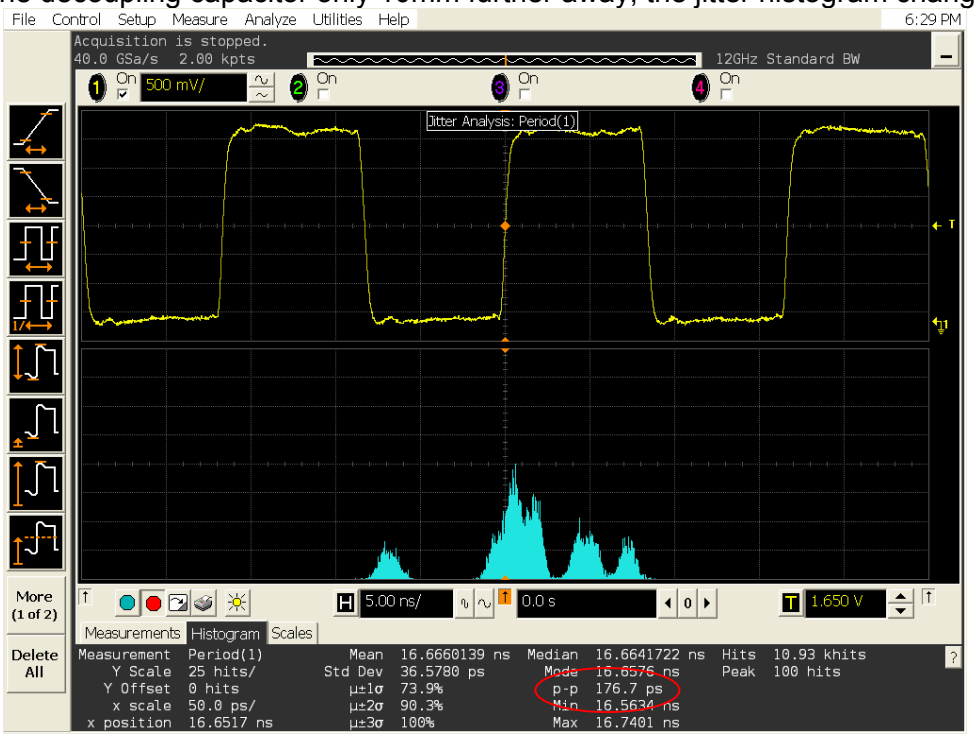
The capacitor should be roughly within 2mm of the VDD pin and within 3mm of the GND pin. The value of 0.1uF is a good compromise to deal with both the high frequency noise from the buffers and the more low frequency noise from internal PLL signals. A combination of both 0.01µF and 0.1µF is even better, where the 0.01µF capacitor is closest to the chip but measurements show that a single 0.1µF capacitor is sufficient to get the job done.

With this placement of the 0.1µF capacitor the 60MHz period jitter histogram looks like this:



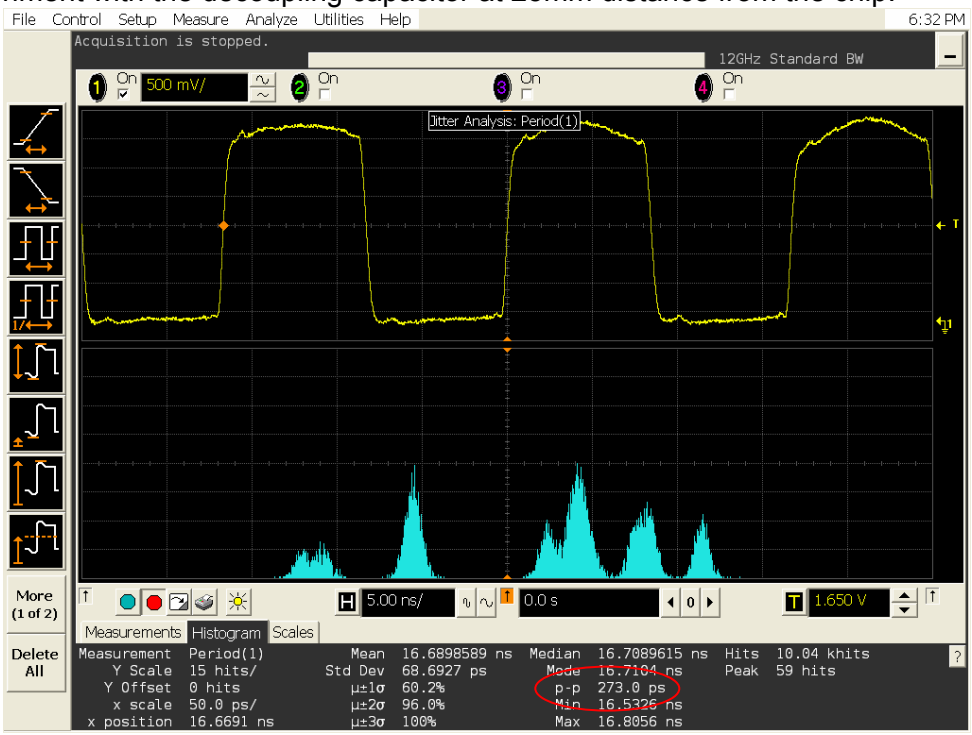
The period jitter is about 63ps PkPk for this case.

When moving the decoupling capacitor only 10mm further away, the jitter histogram changes to this:



The deterministic parts of the jitter spread it out to about 177ps PkPk.

Finally an experiment with the decoupling capacitor at 25mm distance from the chip:



Now the period jitter is as bad as 273ps PkPk.

Also observe the curved shape of the waveform high level and the shape changing from one cycle to the next. There appears to be a lot of noise on the power supply rail.