PL611 and Long Output Traces

Doc ID: PAN0507011
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Date: 1-Jul-05

To maintain signal integrity of a CMOS output waveform, output traces longer than 10mm or 0.5” should be designed as transmission lines. Two well known types are striplines and microstrips. To get the best looking waveform at the end of the trace at the target input, the beginning of the trace should be matched properly. It is not required to match the end of the trace, as long as the signal integrity is only important at the end itself. If you match just the start of the trace, the waveform may look quite bad at the start and halfway the trace but will look fine at the end. Page 3 shows four waveforms at different locations.

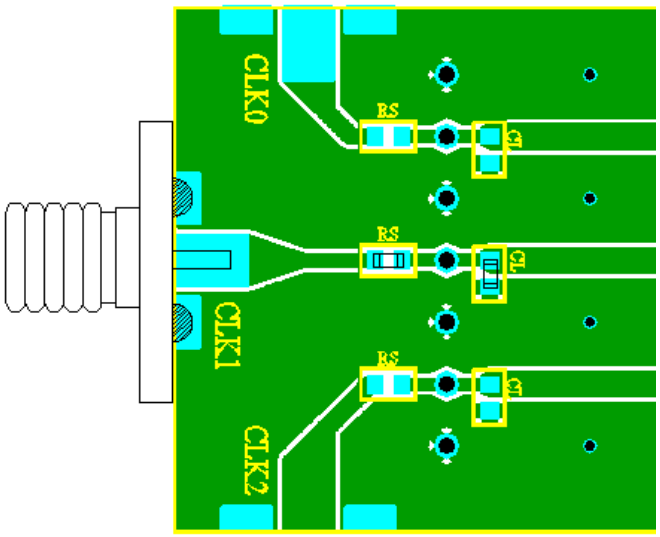
Transmission lines have a characteristic impedance. A popular choice of characteristic impedance is 50Ω. It is a good compromise. It is not advised to go much lower because this would become quite a heavy load on the CMOS output. The lower the impedance, the wider the trace needs to be, so a lower impedance may also not be practical to implement. A higher impedance will slow down rise and fall times at the target so when the frequency is high, it is not advised to go much higher than 50Ω either.

Matching is when you make the output impedance of the CMOS buffer the same as the characteristic impedance of the trace. The output impedance of the CMOS buffer usually is below 50Ω and matching is achieved by adding resistance in series, between CMOS output and start of the trace, so the total adds up to 50Ω. Our PL611 has two output configurations: “standard drive” and “high drive”. With standard drive, the output impedance is 40Ω so we need to add 10Ω in series to match with a 50Ω trace. With high drive, the output impedance is 20Ω so we need to add 30Ω in series to match with a 50Ω trace.

Design rules for striplines and microstrips are readily available on the internet. Instead of carefully designing everything ‘just right’, it is possible to determine the correct matching of CMOS buffer to (long) trace with a simple test. Our goal is a good looking waveform at the end of the trace. We can just look at the waveform and try different values for the matching resistor at the start of the trace until the waveform looks good. Test results on the next pages show waveforms with different resistor values.

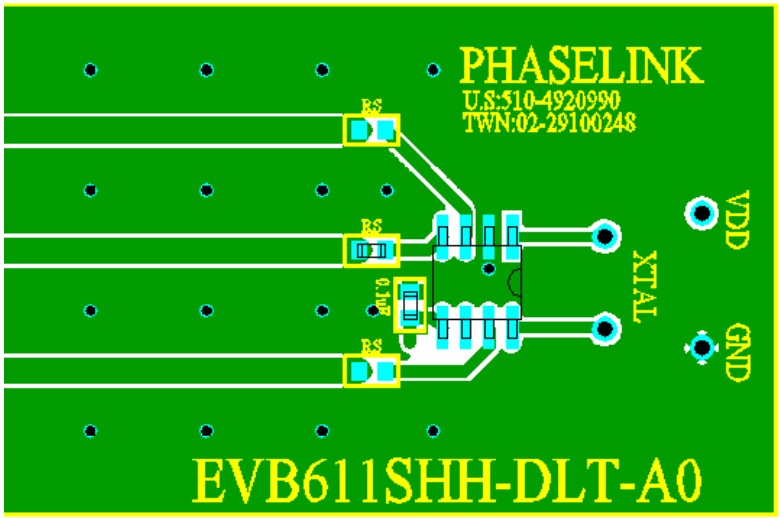
To get the best looking waveform at the end of the trace, it is important that the trace impedance is as constant as possible for the full length of the trace. In general that means that the trace width should remain constant and the ground plane under and possibly above it, should be present for the full length of the trace.

The following pages show waveform test results. The test board used has an 11” (28cm) long trace with 42Ω impedance. The end of the trace is loaded with a 15pF capacitor. There is a resistor between the CMOS output (PL611 with high drive output) and the start of the trace. The best matching is achieved with a 22Ω resistor. See below for pictures of the board. Only both ends of the board are shown because the board is very long.



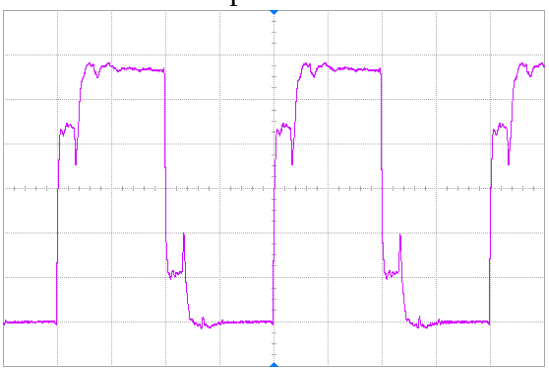
The left side of the board.

The right side of the board.

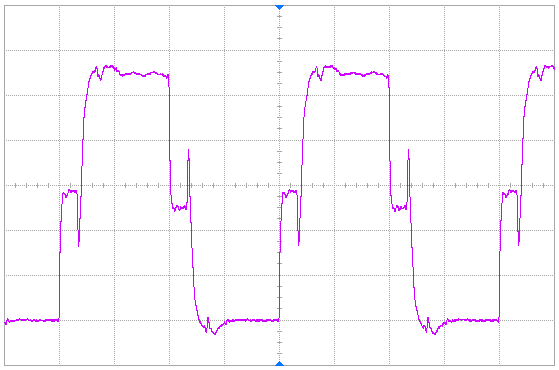


Lets first examine the waveform at different locations along a properly matched trace.

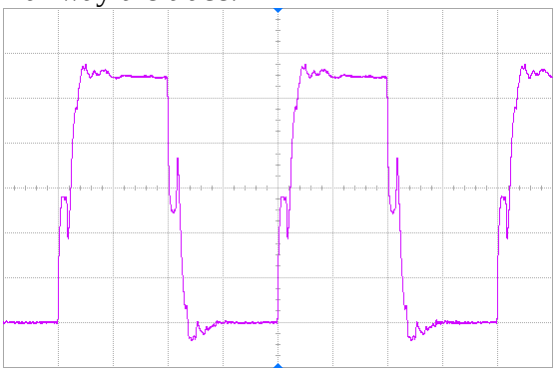
At the CMOS output:



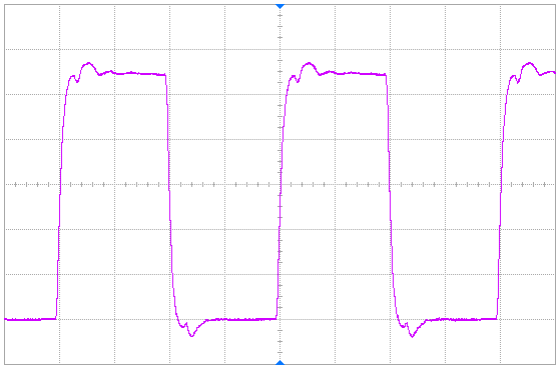
At the start of the trace:



Halfway the trace:



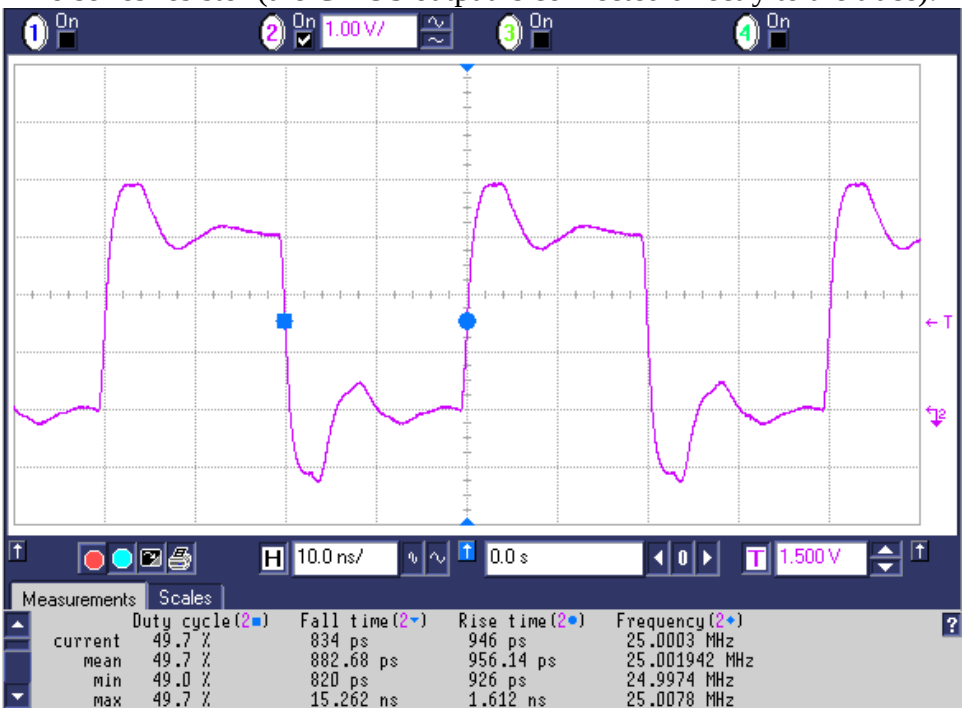
At the end of the trace:



The frequency is 25MHz. Significant reflections are present at all probed locations, except the end of the trace. So don't worry about what the waveform looks like at other locations, it is the waveform at the end of the trace that is important.
The width of the reflections depends upon the length of the trace. It is the time it takes for a pulse to travel back and forth along the trace. The speed of signals traveling through traces is about 0.67 times the speed of light or 2×10^8 m/s. So it takes 2.8ns to travel back and forth along the 28cm trace on the test board. The X-axis in above plots is 10ns/div and the width of the reflections at the start of the trace is indeed very close to this theoretical 2.8ns.

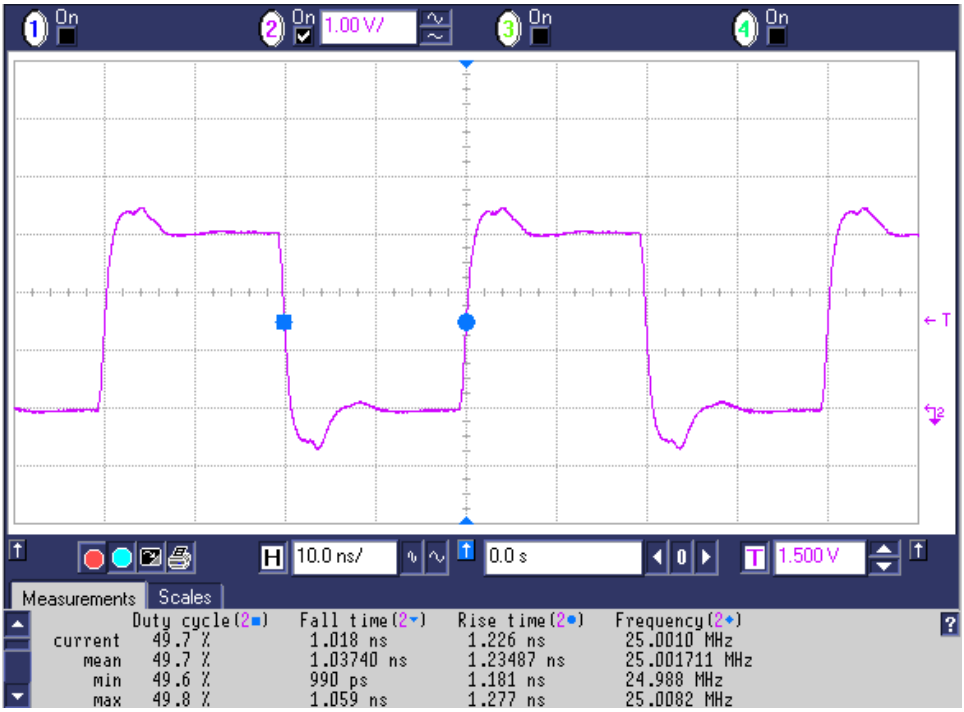
The following oscilloscope pictures show the waveform at the end of the trace, while changing the resistor at the start of the trace.

No series resistor (the CMOS output is connected directly to the trace):



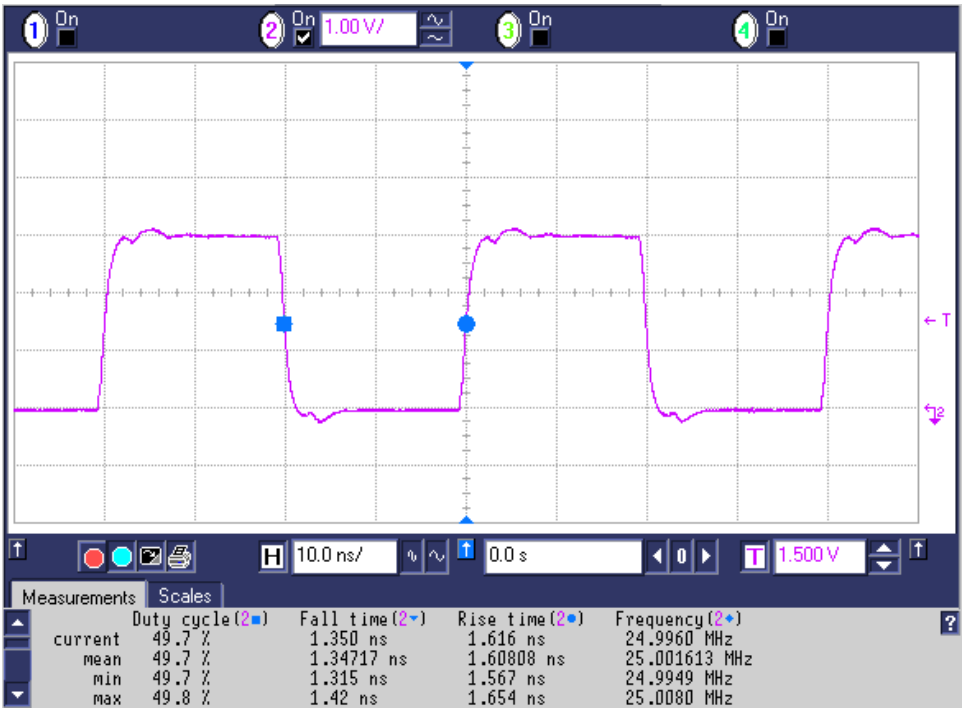
There is large ringing happening at the end of the trace.

Series resistor is 10Ω:



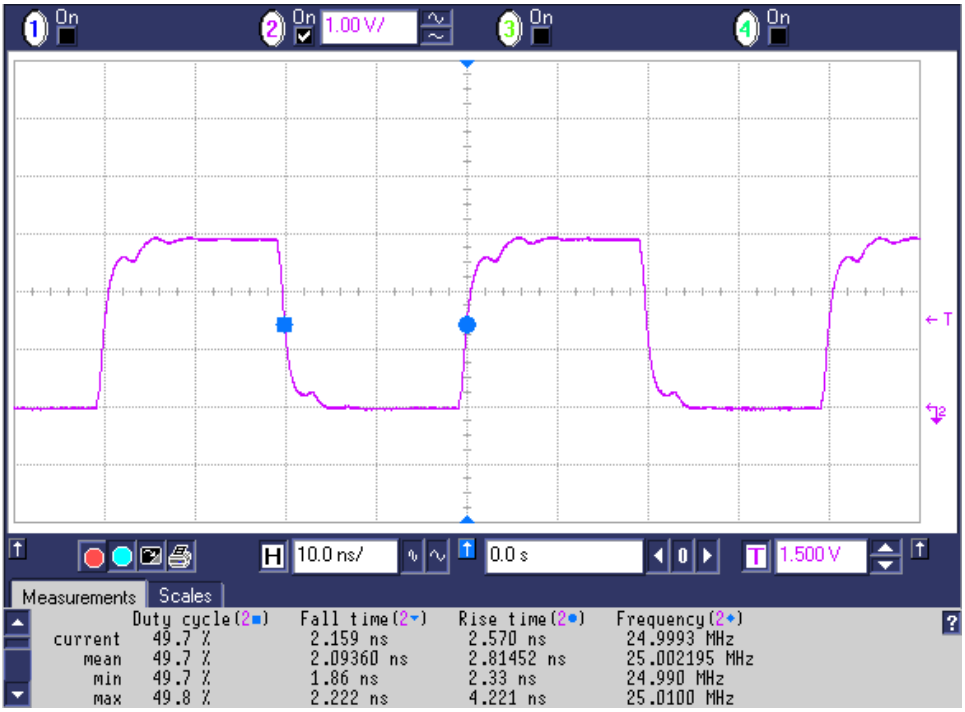
The waveform already looks better than the previous waveform.

Series resistor is 22Ω:



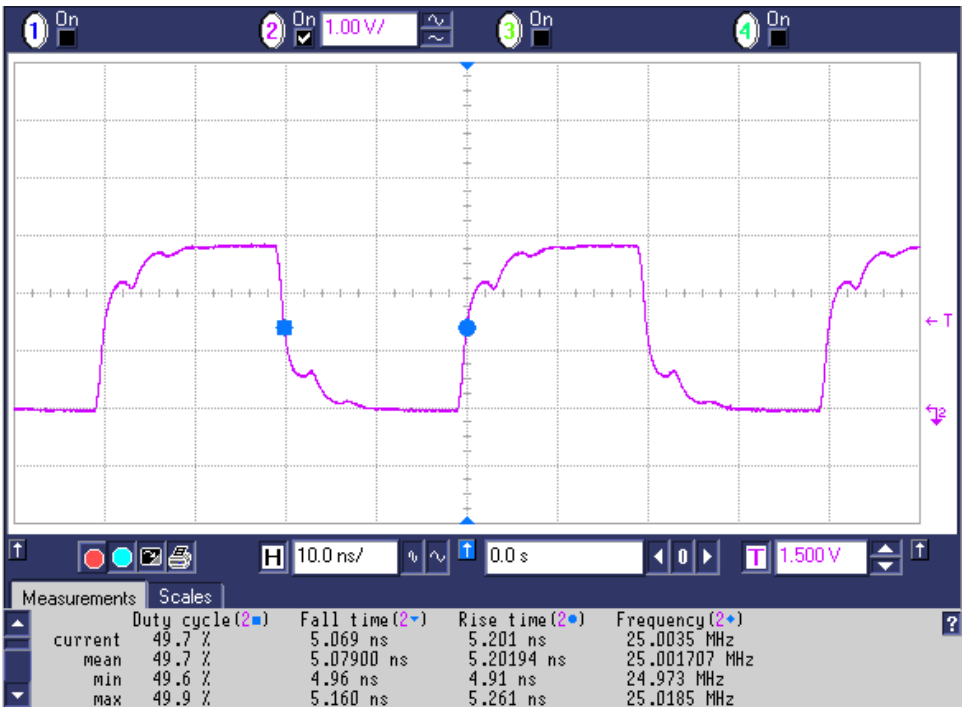
This is the best looking waveform.

Series resistor is 33Ω:



Now we are seeing the edges slow down a little bit.

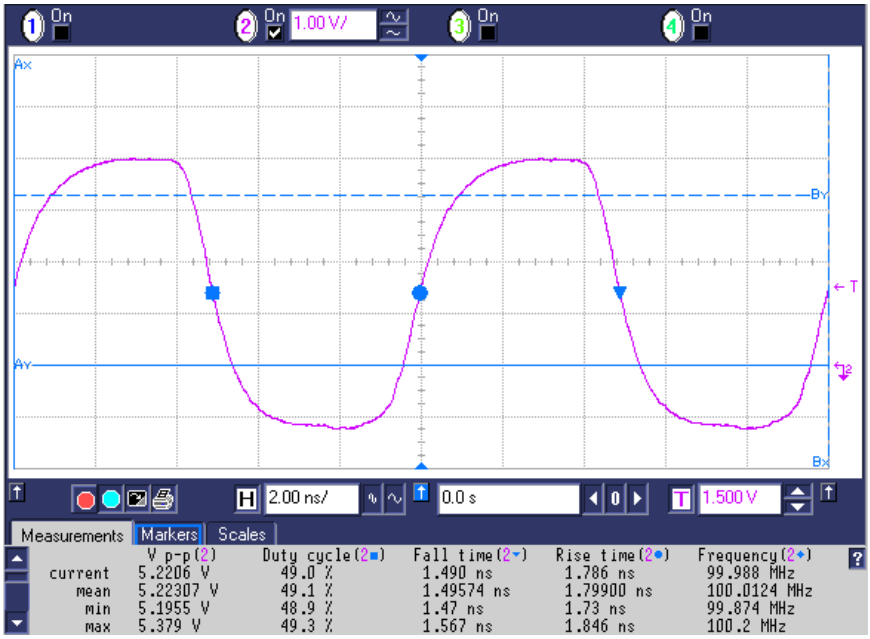
Series resistor is 51Ω:



Now the edges slow down even more so it is obvious that the value of the resistor between CMOS output and the start of the trace is getting too high. The plot with Rs = 22Ω is the best so this is the advised resistor value to use.

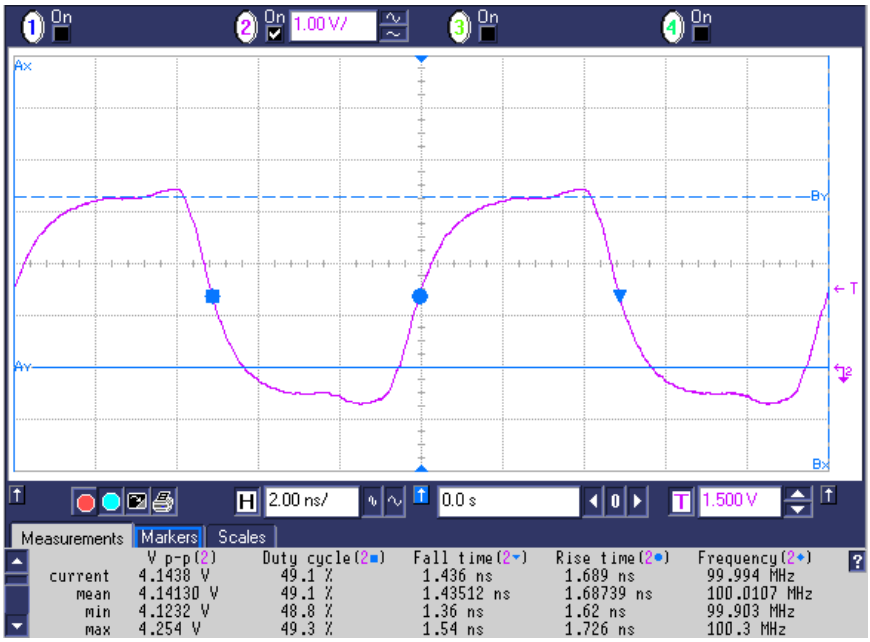
The next waveforms show how a higher frequency makes it more difficult to find the best matching.

No series resistor:



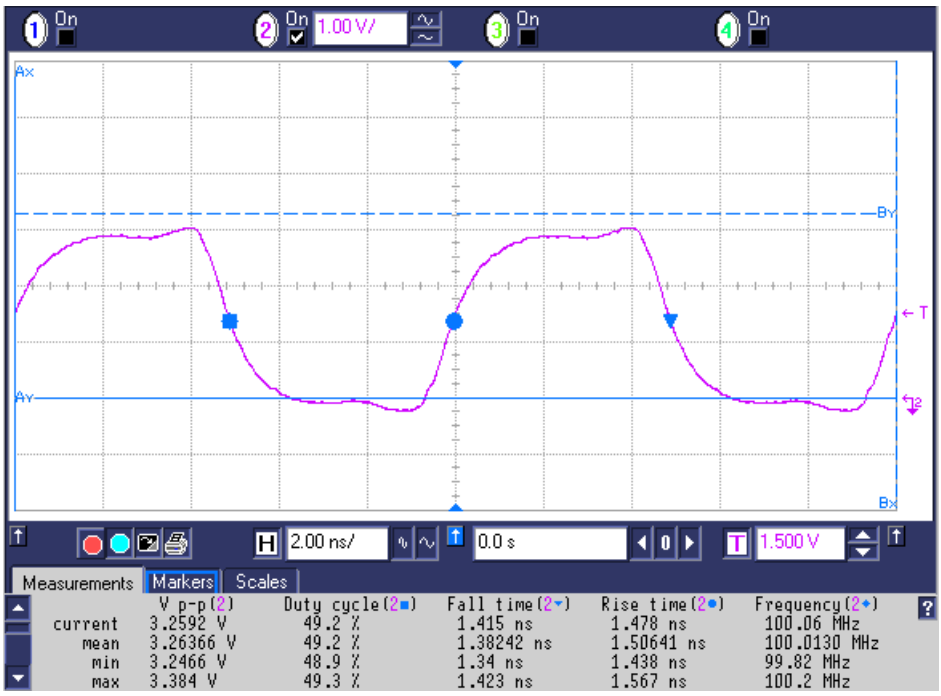
The horizontal marker lines are set at 0V and 3.3V to show the signal w.r.t. the power supply levels. The width of the waveform pulses is now approximately the same as the width of the reflection. Instead of seeing the reflection influence part of the waveform, it now influences the whole waveform. An overshoot turns into an overall larger amplitude. As you can see above, the waveform swings under 0V and over the 3.3V rail.

Series resistor is 10Ω:



This is better but still with an amplitude that is a bit high.

Series resistor is 22Ω:



Finally at 22Ω the amplitude is down to 3.3Vpp. The loading at the end of the trace is still 15pF so the rise and fall times are pretty long. If there is just one CMOS input connected to the end of the trace, then the load can be as low as 5pF and the rise and fall times will be faster.