Microchip MEMS Clocks (DSC) FAQ

1. What are the Junction to Ambient (Theta JA) and Junction to Case (Theta JC) thermal resistance for the MEMS products?

Microchip Package Name	Basic DSC Part Numbers	θJa (°C/W)	θJc (°C/W)	PCB Layers
DFN1612-4LD	**DSC6xxx**	172.6	127.0	4
DFN1612-6LD	**DSC6xxx**	172.6	127.0	4
DFN2016-4LD	**DSC6xxx**	92.4	56.4	4
DFN2016-6LD	**DSC6xxx**	92.4	56.4	4
DFN2520-4LD	**DSC10xx, DSC6xxx**	257.7	97.0	4
DFN2520-6LD	**DSC11xx, DSC12xx**	257.7	97.0	4
DFN3225-4LD	**DSC10xx, DSC6xxx**	45.0	5.5	4
DFN3225-6LD	**DSC11xx, DSC12xx**	45.0	5.5	4
DFN5032-4LD	**DSC10xx**	90.0	45.0	4
DFN5032-6LD	**DSC11xx, DSC12xx**	90.0	45.0	4
DFN7050-4LD	**DSC10xx**	113.0	30.0	4
DFN7050-6LD	**DSC11xx, DSC12xx**	103.5	30.0	4
DFN3225-14LD	**DSC2xxx**	71.0	7.5	4
DFN3225-20LD	**DSC400, DSC557**	24.1	3.0	4

2. Can a MEMS device select among different frequencies for a given output clock?

Yes, this is achieved by using some external input pins as frequency banks selectors. Let's consider the DSC2010 as an example. There are two input pins, pin 5 and pin 6 that are called FS0 and FS1. The four binary combinations of these pins allow selecting one of the four frequency banks of the device. Each frequency bank can be programmed (OTP = One Time Programmed) with a clock frequency that is independent and unrelated to the one of the other three banks.

Similarly, the DSC2110 and DSC2210 use input pin 14 (FS) to select among two frequency banks. The DSC2022 has 3 frequency select inputs, pins 5, 6 and 7 that can select one among eight

frequency banks. This concept is generic and not necessarily restricted to these parts that were picked as examples. Eight frequency banks is the maximum number for the DSC2xxx family.

3. Is it possible to change the programmed output frequency?

The output clock frequency is programmed one time (OTP) at the factory. However, frequency bank 0 (and only this specific bank) is shadowed with a non-volatile memory (RAM). It is therefore possible to temporarily change the three VCO register counters (N, f, M) that set the output frequency. Refer to the DSC2xxx Programming Guide for more details. Again, it is important to note that this is only possible for bank frequency 0, therefore the input frequency select pin(s) must be set in a way to select frequency bank 0 (typically all input pins connected to ground).

4. What is the logic level for the input frequency select pins?

The devices datasheet specify the input logic levels VIH and VIL. These levels apply to all inputs whether they are frequency select pins, output enables or standby, etc.

5. Are there MEMS devices that can generate two clock outputs from the same device?

The DSC2311 will simultaneously provide two frequencies on pins 4 and 5. The device has only one PLL, therefore the two output frequencies must have the VCO frequency as a common multiple.

The DSC400 has four output clocks and two PLLs, therefore two set of outputs can be independent and unrelated to the other set of two.

There are also other clock generators, like the DSC2xxx family, that have frequency select pins. They can provide up to 8 selectable frequencies on the clock output pin, depending on the logic levels on the frequency select pins.

6. How does the phase noise change with the carrier frequency?

As an example, let us consider a 25MHz carrier and let us assume that its phase noise plot (in the 12kHz to 20MHz bandwidth) is known. Let us also assume that one may want to know how different the plot would look like with 10MHz and 50MHz carriers.

All the frequency components in the 12kHz to 20MHz bandwidth are expressed in dBc/Hz and they scale with the different carrier frequency according to the relationship:
20[dBc/Hz]*log10(frequency/25MHz)

For frequency = 10MHz all components shift by -7.96dB/Hz

For frequency = 50MHz all components shift by +6.02dB/Hz

7. Does the supply current increase with the voltage supply and the clock frequency?

The answer is yes with both. The table below shows an example relative to the DSC1001 device.

Output Frequency	Temperature	VDD		
		1.65 V	2.5 V	3.6 V
100 MHz	-40 C	8.05	11.13	11.86
	-25 C	8.11	11.20	11.93
	15 C	8.23	11.35	12.09
	25 C	8.27	11.40	12.14
	45 C	8.36	11.51	12.26
	65 C	8.46	11.64	12.40
	72 C	8.51	11.69	12.45
	88 C	8.78	12.13	12.92
	108 C	8.96	12.35	13.16
25 MHz	-40 C	5.60	6.43	6.63
	-25 C	5.66	6.49	6.68
	15 C	5.78	6.62	6.84
	25 C	5.82	6.66	6.88
	45 C	5.91	6.75	6.98
	65 C	6.02	6.87	7.11
	72 C	6.05	6.91	7.15
	88 C	6.27	7.14	7.43
	108 C	6.50	7.52	7.82

8. In addition to bypass capacitors, do you recommend using ferrite beads on the power supply (VDD)?

We don't recommend using ferrite beads as the ferrite bead may impede the inrush current when the part starts up, and may make the part fail to initialize correctly. A low-value resistor would make a reasonable substitute for the ferrite beads.

9. Can the MEMS devices latch up?

It is possible to put the MEMS oscillator devices into latch up via the input control pin (a.k.a. Output Enable or Standby pin). If the voltage on the input control pin goes either ~0.6V above VDD or ~0.6V below GND, then latch up might be initiated. Of course, applying such voltages on the input control pin (pin 1) violates the absolute maximum ratings of the devices.

It's plausible that such voltages could be created unintentionally by the combination of a fast signal generator driving the input control pin and inductance on the trace or cable connecting the signal generator to such a pin. The key behavior produced would be voltage overshoot on the rising and/or falling edges of the signal, as seen at the input control pin. If the magnitude of this overshoot starts to approach ~0.6V, on either rising or falling edges, then that could definitely account for a latch up condition.

10. What is the difference between startup time and enable time and how are they measured?

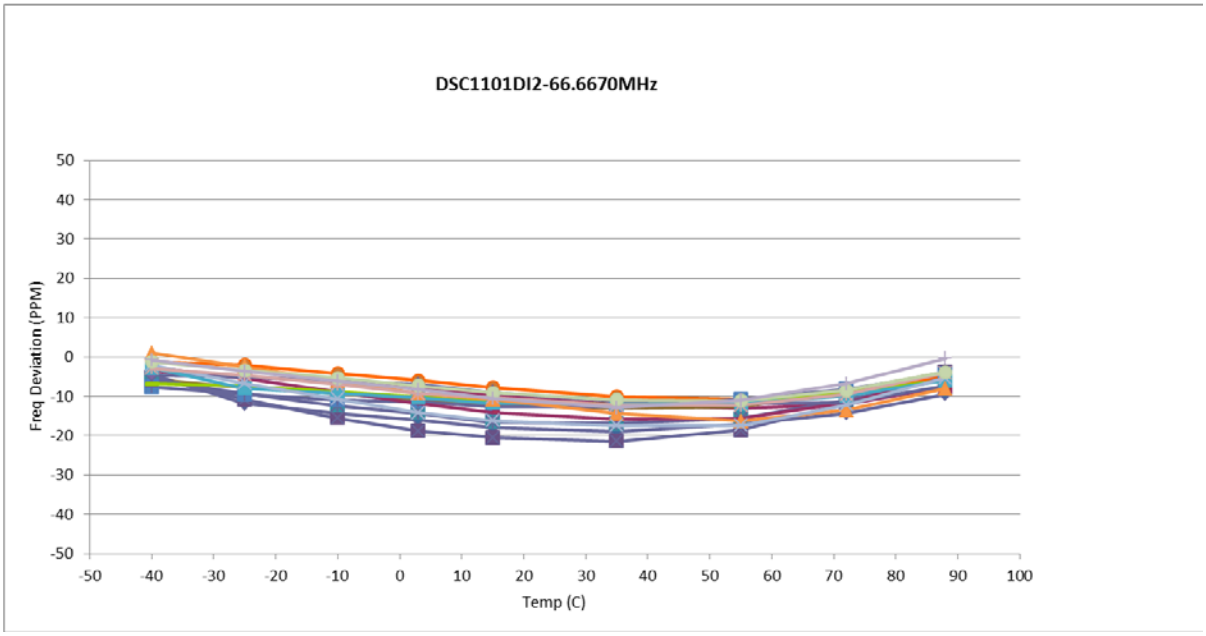
Start-up time, also called t_{SU} in the datasheet, is defined as the time from when VDD reaches 90% of its final value until the first edge on the output clock. The 90% VDD threshold is defined for cases of slow VDD ramp rates, where VDD's rise time may be significant compared to 1.5ms. There is no output clock until after the PLL has locked and the output frequency is stable.

Enable time, also called t_{EN} in the datasheet, is defined as the time from when the enable pin goes high until the first edge on the output clock. In case the rise time of the enable pin may be significant compared to 1.5ms, the VIH spec (analogous to the 90% VDD level) specifies the point on the enable pin's rising edge from which the enable time is measured.

11. What is the frequency stability behavior over the temperature range?

MEMS oscillators and clocks unlike crystals have a very stable frequency deviation over the entire temperature range. Frequency deviation in PPM generally rises significantly in crystals when the temperature rises. For MEMS it actually stays pretty flat.

The picture below shows the frequency stability for the DSC1101DI2 at 66.667MHz, as an example. This is a MEMS oscillator in a 2520 package with nominal ±25ppm frequency stability.



The frequency stability is actually independent of package and output frequency and is fairly constant over the entire temperature range.

The calibration procedure is the same for all stability grades, and the difference between frequency grades lies principally in the testing done after calibration and performance ratings that come with the part.

12. Can the soldering process affect the frequency stability?

The short answer is yes.

Datasheet specifications apply to the parts at the time of shipment. The process of soldering the MEMS DSC parts onto a PCB happens after the time of shipment and generally can introduce some modest amount of frequency shift. This solder-down frequency shift will not necessarily be constant across temperature and will, naturally, depend on the parameters of the solder down process.

The worst frequency shifts are seen when parts are hand-soldered onto the PCBs, as opposed to oven-reflowed in accordance with the datasheet's recommended reflow profile.

The frequency shift due to SMT assembly can depend on the temperature ramp rates and dwell times, amount of solder paste printed, selected solder alloy, and choice of flux paste. It is recommended that the SMT assembler measure their actual reflow profile, preferably with the thermocouple or RTD placed as close to the MEMS device as possible.

13. Can the MEMS oscillators/clocks work in high pressure environment? In particular up to 700psi and surviving at 1,700psi.

Tests have not been conducted in a way that would align with those requirements; therefore there is no guarantee that the devices will meet either the operating pressure or survival pressure requirement.

However, there is good reason to believe that the parts will not have trouble with these pressure levels. The MEMS devices are packaged using standard QFN materials and processes. During QFN molding, the pressures typically reach the range of 3-10MPa (430-1430psi), and this pressure has never been known to cause a device to fail.

The MEMS devices do have a cavity for the MEMS resonator, which is surrounded on all sides by very thick silicon walls, many times thicker than the dimensions of the cavity itself. Because of this, the resonator would theoretically deform by only Angstroms at 1700 psi.

Finally, in accordance with industry standards, all MEMS oscillators and clock devices have passed the pressure cooker (PCT) reliability testing. Also, the devices stand up to military-grade shock and vibration testing.