

Introduction

Considering that each available clock logic type (LVPECL, HCSL, CML, and LVDS) operates with a different common-mode voltage and swing level than the next (see [Table 1](#)), it is necessary to design clock logic translation between the driver side and receiver side for any given system design. This application note details how to translate one differential clock into other types of differential logics by adding attenuation resistors and bias circuits between them to attenuate the swing level and re-bias the common-mode for the input of the receiver.

Table 1. Common-Mode Voltage and Swing Levels of Different Clock Logic Types

Specification	LVPECL	LVDS	CML Terminated 50Ω to V _{CC}	HCSL
V _{CM}	V _{CC} – 1.4V	1.2V	V _{CC} – 0.2V	350mV
V _{SWING_SE}	800mV	325mV	400mV	700mV
V _{OH}	V _{CC} – 1V	1.3625V	V _{CC}	700mV
V _{OL}	V _{CC} – 1.8V	1.0375V	V _{CC} – 0.400V	0V
Reference	V _{CC}	Ground	V _{CC}	Ground

Input/Output Structure of Each Differential Clock Logic

Prior to designing the logic translation circuit, an examination of the input/output structures of each logic type – LVPECL, HCSL, CML, and LVDS – is required as each logic type features a different common-mode voltage and swing level.

Low-Voltage, Positive-Referenced, Emitter-Coupled Logic (LVPECL)

Low-voltage, positive-referenced, emitter-coupled logic (LVPECL) originates from emitter-coupled logic (ECL), adopting a positive power supply.

The LVPECL input is a current-switching differential pair with high input impedance (see [Figure 1](#)). The input common-mode voltage should be approximately V_{CC} – 1.3V for the purpose of having operating headroom, either from internal self-biasing or external biasing.

The LVPECL output consists of a differential pair amplifier which drives a pair of emitter followers (or open emitters) as illustrated in [Figure 1](#). The output emitter followers should operate in the “active” region with DC current at all times. The output pins of OUT+ and OUT– are typically connected to differential transmission lines (Z₀ = 100Ω) or a single-ended transmission line (Z₀ = 50Ω) for impedance matching. The proper termination for LVPECL output is 50Ω to V_{CC} – 2V and OUT+/OUT– will typically be V_{CC} – 1.3V, resulting in an approximate DC current flow of 14mA.

Another way to terminate LVPECL output is to apply 142Ω to GND, which provides a DC-biasing for LVPECL output and a DC current path to GND. Because the LVPECL output common-mode is at V_{CC} – 1.3V, the DC-biasing resistor can be selected by assuming a DC current of 14mA (R = V_{CC} – 1.3V / 14mA), resulting in R = 142Ω (150Ω also works) for V_{CC} – 3.3V.

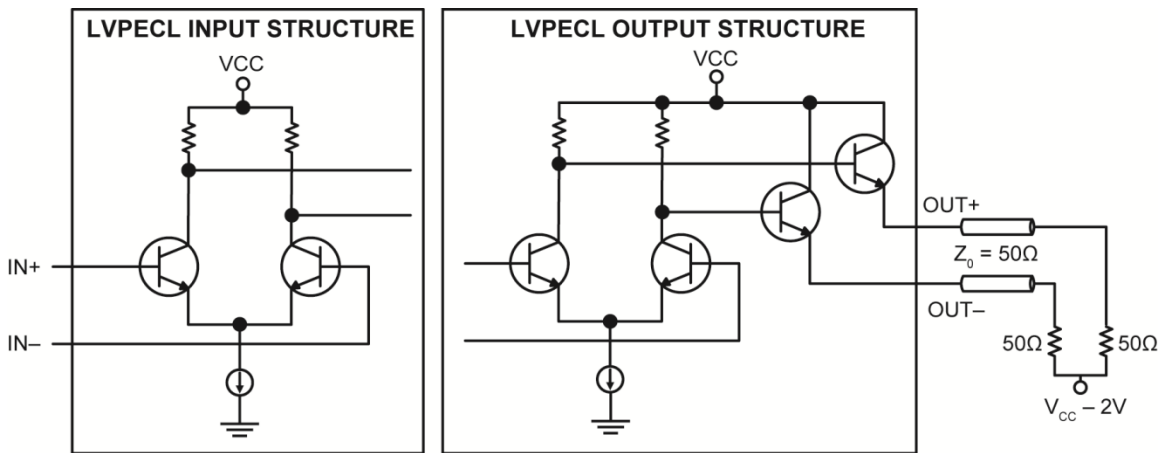


Figure 1. LVPECL Input/Output Structure

Low-Voltage Differential Signaling (LVDS)

Low-voltage differential signaling (LVDS) input requires a 100Ω termination resistor across the pins of IN+ and IN- with a common-mode voltage of approximately 1.2V (see Figure 2). If the 100Ω termination is not included on-chip, it must be included on the printed circuit board (PCB).

The LVDS output driver consists of a 3.5mA current source which is connected to differential outputs through a switching network. The output pins of OUT+ and OUT- are typically connecting to differential transmission lines ($Z_0 = 100\Omega$) or a single-ended transmission line ($Z_0 = 50\Omega$) for impedance matching – which are terminated with a 100Ω resistor across the receiver inputs – resulting in 350mV swing for LVDS logic (Figure 2).

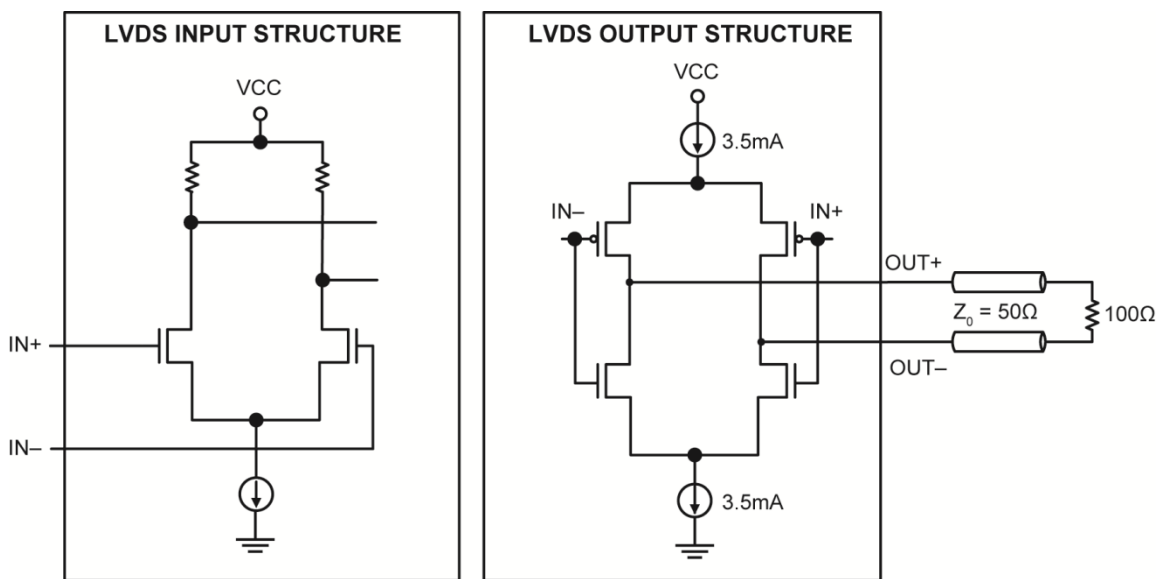


Figure 2. LVDS Input/Output Structure

Current-Mode Logic (CML)

Most current-mode logic (CML) input structures have a 50Ω resistor to V_{CC} on-chip (see Figure 3). If not, then one must be applied to VDD on both inputs of IN+ and IN- on the PCB. The input transistors are emitter followers which drive a differential-pair amplifier.

The CML output consists of a differential pair of common-emitter transistors with 50Ω collector resistors as the CML output structure illustrated in Figure 3 shows. The outputs of OUT+ and OUT- are typically connecting to differential transmission lines (Z₀ = 100Ω) or a single-ended transmission line (Z₀ = 50Ω) for impedance matching (Figure 3). The signal swing is provided by switching the current in a common-emitter differential BJT. Assuming the current source is 16mA (typical) and the CML output is loaded with a 50Ω resistor which is pull-up to V_{CC}, this will result in an output voltage swing from V_{CC} to V_{CC} - 0.4V with a common-mode voltage (V_{CC} - 0.2V).

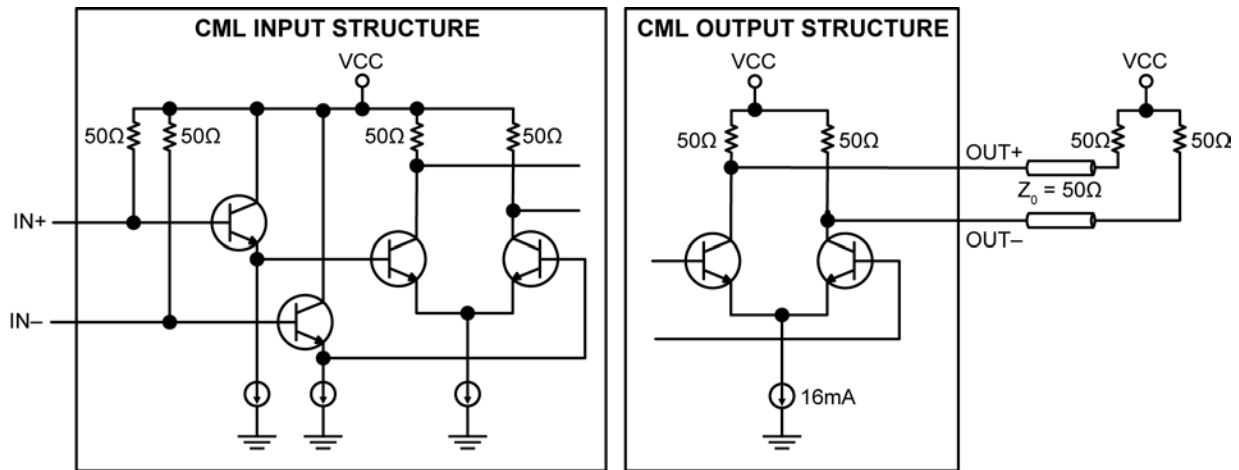


Figure 3. CML Input/Output Structure

High-Speed Current-Steering Logic

The high-speed current-steering logic (HCSL) input requires the single-ended swing of 700mV on both input pins of IN+ and IN- with a common-mode voltage of approximately 350mV (see Figure 4).

A typical HCSL driver is a differential logic with open-source outputs, where each of the output pins switches between 0 and 14mA. When one output pin is low (0), the other is high (driving 14mA). The output pins of OUT+ and OUT- are typically connecting to differential transmission lines ($Z_0 = 100\Omega$) or a single-ended transmission line ($Z_0 = 50\Omega$), which requires an external termination resistor (50Ω to GND), resulting in a 700mV swing level for HCSL input structures (Figure 4).

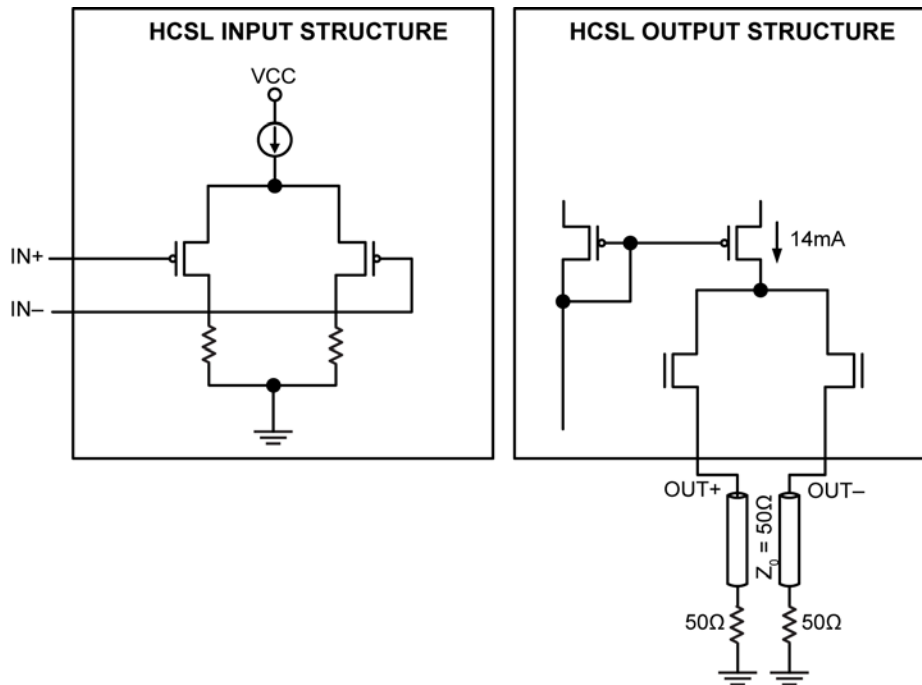


Figure 4. HCSL Input/Output Structure

LVPECL-to-CML Translation

As shown in Figure 5, placing a 150Ω resistor to GND at LVPECL driver output is essential for the open emitter to provide the DC-biasing as well as a DC current path to GND. In order to attenuate the 800mV LVPECL swing to 400mV CML swing, place a 50Ω attenuating resistor (R_A) after the 150Ω resistor to attenuate half of the LVPECL swing level. Additionally, self-biasing inside the CML receiver input must be confirmed. If the self-biasing at the input of CML is not present, a 50Ω termination resistor to VCC must be placed on the PCB for CML biasing and transmission line termination.

Micrel’s ultra-low-jitter crystal oscillators and clock generators (i.e., MX55, MX57, SM802xxx, SM803xxx, MX85xxx) can provide <0.3ps RMS phase jitter with any type of output logics, except CML logic. With the below translation circuit, it is easy to achieve CML output from LVPECL logic.

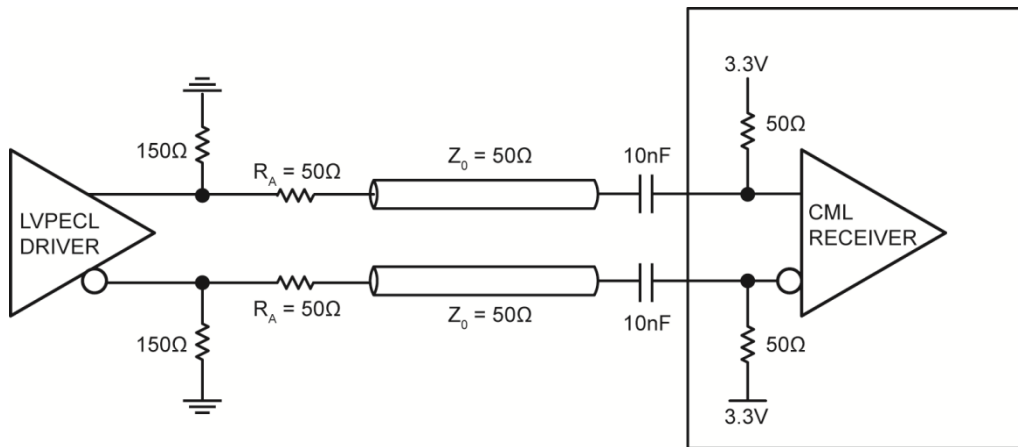


Figure 5. LVPECL-to-CML Translation

LVPECL-to-LVDS Translation

Placing a 150Ω resistor to GND at LVPECL driver output is essential for the open emitter to provide the DC-biasing as well as a DC current path to GND (Figure 6). In order to attenuate the 800mV LVPECL swing to a 325mV LVDS swing, a 70Ω attenuating resistor must be applied after the 150Ω resistor. A 10nF AC-coupled capacitor should be placed in front of the LVDS receiver to block DC level coming from the LVPECL driver. After the AC-coupled capacitor, re-biasing is required for the LVDS input and can be done by placing 8.7KΩ resistor to 3.3V and 5KΩ resistor to GND to achieve 1.2V DC level for the input common-mode of LVDS receiver. If the LVDS receiver already has integrated a 100Ω resistor across the differential input pins, the external 100Ω resistor is not required.

When Micrel’s LVPECL fan-out buffers (i.e., SY89831) have been qualified and adopted by customers, but some of the outputs require LVDS logics for the following receivers, this LVPECL-to-LVDS translation circuit is very helpful to achieve the target.

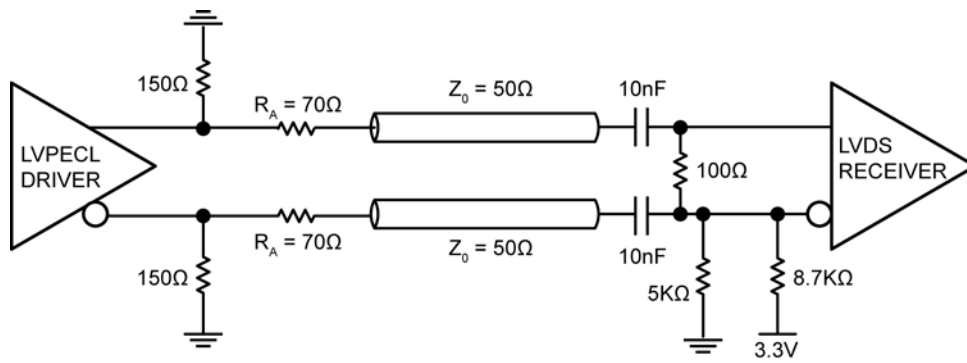


Figure 6. LVPECL-to-LVDS Translation

LVPECL-to-HCSL Translation

As shown in Figure 7, placing a 150Ω resistor to GND at LVPECL driver output is essential for the open emitter to provide the DC-biasing as well as a DC current path to GND. In order to attenuate an 800mV LVPECL swing to a 700mV HCSL swing, an attenuating resistor ($R_A = 8\Omega$) must be placed after the 150Ω resistor. A 10nF AC-coupled capacitor should be placed in front of the HCSL receiver to block DC level coming from the LVPECL driver. After the AC-coupled capacitor is placed, re-biasing is required for the HCSL input and can be done by placing 470Ω resistor to 3.3V and 56Ω resistor to GND to achieve 350mV DC level for the input common-mode of HCSL receiver.

When Micrel’s LVPECL fan-out buffers (i.e., SY89831) have been qualified and adopted by customers, but some of the outputs require HCSL logics for the following receivers, this LVPECL-to-HCSL translation circuit is very helpful to achieve the target.

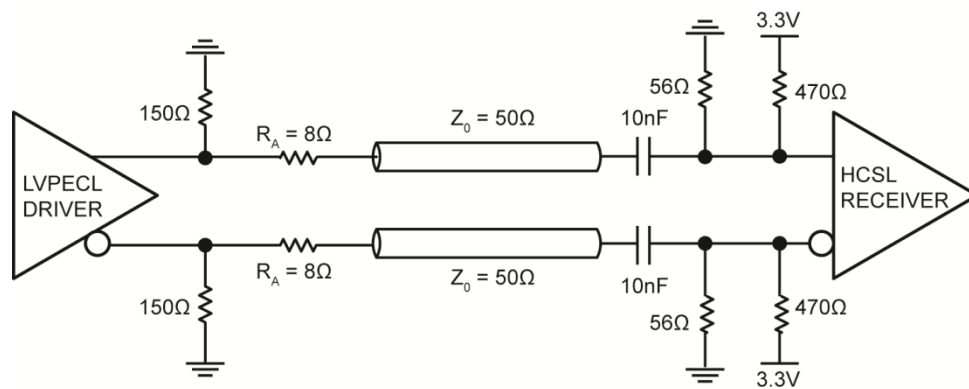


Figure 7. LVPECL-to-HCSL Translation

HCSL-to-LVDS Translation

In Figure 8, each of HCSL output pins switches between 0 and 14mA. When one output pin is low (0), the other is high (driving 14mA). The equivalent loading for HCSL driver is 48Ω parallel to 50Ω , which equates 23.11Ω . The swing level on the LVDS input is $14mA \times 23.11\Omega = 323mV$. A 10nF AC-coupled capacitor should be placed in front of the LVDS receiver to block DC level coming from the HCSL driver. After the AC-coupled capacitor is placed, re-biasing is required for the LVDS input and can be done by placing $8.7K\Omega$ resistor to 3.3V and $5K\Omega$ resistor to GND to achieve 1.2V DC level for the input common-mode of LVDS Receiver. If the LVDS receiver already has integrated a 100Ω resistor across the differential input pins, the external 100Ω resistor is not required.

When Micrel’s HCSL fan-out buffers (i.e., SY75576L, SY75578L) have been qualified and adopted by customers, but some of the outputs require LVDS logics for the following receivers, this HCSL-to-LVDS translation circuit is very helpful to achieve the target.

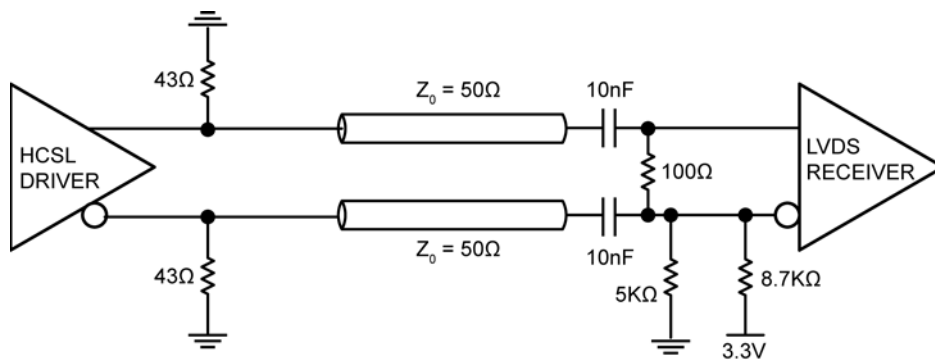


Figure 8. HCSL-to-LVDS Translation

HCSL-to-CML Translation

In Figure 9, each of HCSL output pins switches between 0 and 14mA. When one output pin is low (0), the other is high (driving 14mA). The equivalent loading for HCSL driver is 68Ω parallel to 50Ω , which equates 28.81Ω . The swing level on the CML input is $14mA \times 28.81\Omega = 403mV$. A 10nF AC-coupled capacitor should be placed in front of the CML receiver to block DC level coming from the HCSL driver. Additionally, self-biasing inside the CML receiver input must be confirmed. If the self-biasing at the input of CML is not present, a 50Ω termination resistor to VCC must be placed on the PCB for CML biasing and transmission line termination.

Micrel’s ultra-low-jitter crystal oscillators and clock generators (i.e., MX55, MX57, SM802xxx, SM803xxx, MX85xxx) can provide $<0.3ps$ RMS phase jitter with any type of output logics, except CML logic. With the below translation circuit, it is easy to achieve CML output from HCSL logic.

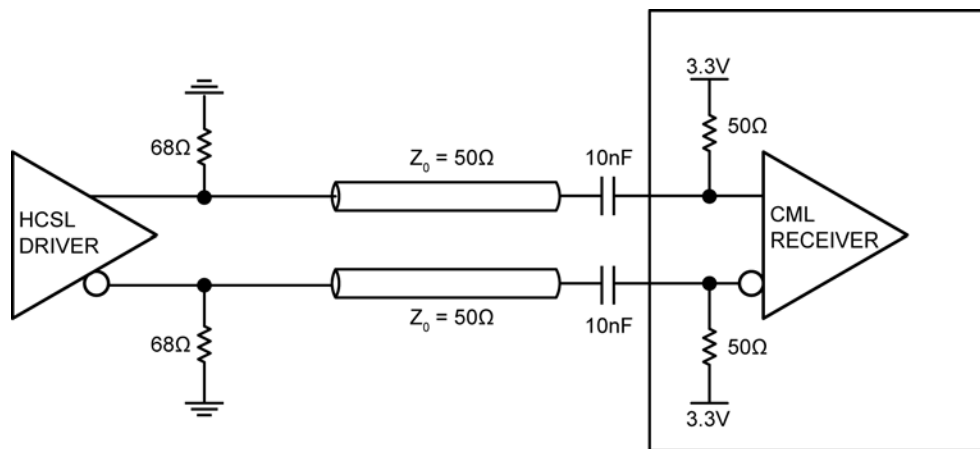


Figure 9. HCSL-to-CML Translation

LVDS-to-CML Translation

LVDS output drives a $\pm 3.5\text{mA}$ current through the termination of 100Ω resistor, resulting in a 350mV swing level in front of the CML receiver (Figure 10). Confirmation that the CML receivers are capable of receiving a 350mV swing is required because the standard swing of CML is 400mV . Additionally, self-biasing inside the CML receiver input must also be confirmed. If the self-biasing at the input of CML is not present, a 50Ω termination resistor to VCC must be placed on the PCB for CML biasing and transmission line termination.

Micrel’s ultra-low-jitter crystal oscillators and clock generators (i.e., MX55, MX57, SM802xxx, SM803xxx, MX85xxx) can provide $<0.3\text{ps}$ RMS phase jitter with any type of output logics, except CML logic. With the below translation circuit, it is easy to achieve CML output from LVDS logic.

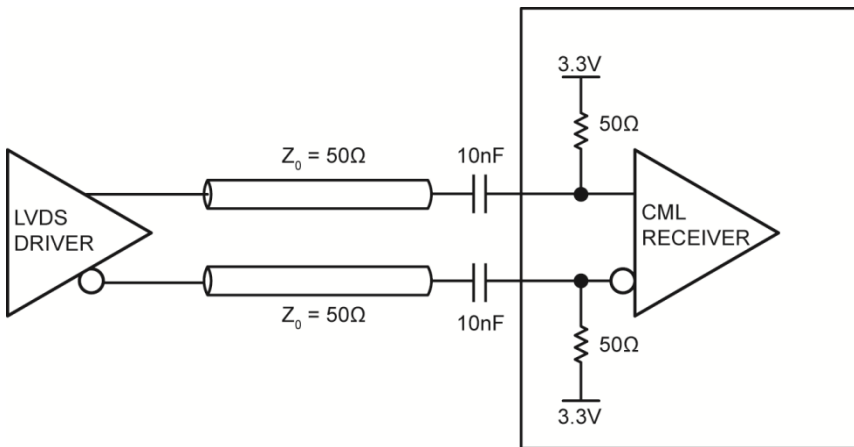


Figure 10. LVDS-to-CML Translation

Summary

This application note presents how to translate different clock logics. With the proper signal level attenuation and self-biasing circuit in front of the receiver side, a translation circuit can be easily achieved with less external components.

MICREL, INC. 2180 FORTUNE DRIVE SAN JOSE, CA 95131 USA

TEL +1 (408) 944-0800 FAX +1 (408) 474-1000 WEB <http://www.micrel.com>

Micrel makes no representations or warranties with respect to the accuracy or completeness of the information furnished in this data sheet.

This information is not intended as a warranty and Micrel does not assume responsibility for its use. Micrel reserves the right to change circuitry, specifications and descriptions at any time without notice. No license, whether express, implied, arising by estoppel or otherwise, to any intellectual property rights is granted by this document. Except as provided in Micrel's terms and conditions of sale for such products, Micrel assumes no liability whatsoever, and Micrel disclaims any express or implied warranty relating to the sale and/or use of Micrel products including liability or warranties relating to fitness for a particular purpose, merchantability, or infringement of any patent, copyright or other intellectual property right.

Micrel Products are not designed or authorized for use as components in life support appliances, devices or systems where malfunction of a product can reasonably be expected to result in personal injury. Life support devices or systems are devices or systems that (a) are intended for surgical implant into the body or (b) support or sustain life, and whose failure to perform can be reasonably expected to result in a significant injury to the user. A Purchaser's use or sale of Micrel Products for use in life support appliances, devices or systems is a Purchaser's own risk and Purchaser agrees to fully indemnify Micrel for any damages resulting from such use or sale.

© 2014 Micrel, Incorporated.

Revision History

Date	Change Description/Edits by:	Rev.
7/9/14	Initial release of new Application Note	1.0