SY898535L

Precision Differential 3.3V, Low Skew, 1:4 LVCMOS/LVTTL -to-LVPECL Fanout Buffer

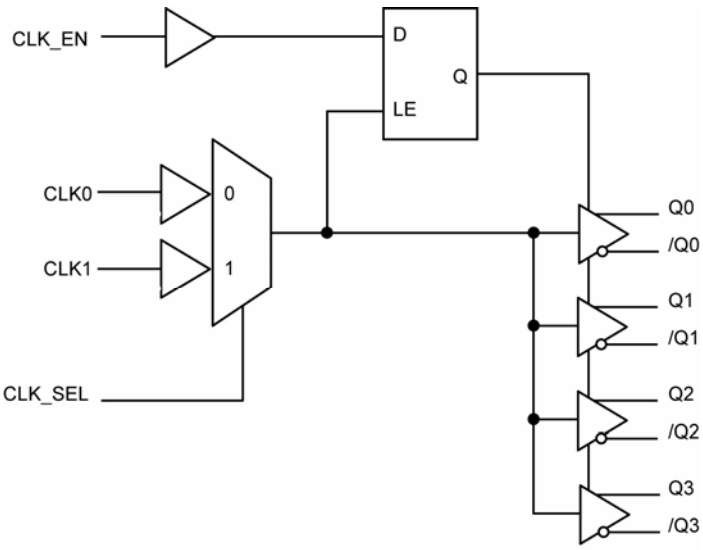
General Description

The SY898535L is a 3.3V, low skew, 1:4 LVCMOS/LVTTL-to-LVPECL fanout buffer with two selectable single ended clock inputs. The CLK0 and CLK1 accept LVCMOS or LVTTL input levels and translate them to 3.3V LVPECL levels. To eliminate runt pulses on the outputs during asynchronous assertion/de-assertion of the clock enable pin, the clock enable is synchronized with the input signal.

The SY898535L operates from a 3.3V ±5% supply and is guaranteed over the full industrial temperature range of –40°C to +85°C. The SY898535L is part of Micrel's high-speed, Precision Edge® product line.

Datasheets and support documentation can be found on Micrel's web site at: www.micrel.com.

Functional Block Diagram



Features

- Provides four differential 3.3V LVPECL copies
- Selects between single-ended CLK0 or CLK1 input
- CLK0 and CLK1 accept LVCMOS or LVTTL input levels
- Guaranteed AC performance over temperature and supply voltage:
  - 235MHz Maximum output frequency
  - <1.9ns Propagation delay (In-to-Q)
  - <30ps Output skew
  - <250ps Part-to-part skew
  - Additive phase jitter, RMS: 0.09ps (typical)
- 3.3V ±5% supply voltage
- –40°C to +85°C industrial temperature operating range
- Available in a 20-pin TSSOP package

Applications

- Gigabit Ethernet
- 10Gigabit Ethernet
- SONET/SDH
- PCI

Markets

- LAN/WAN
- Enterprise servers
- ATE
- Test and measurement

Precision Edge is a registered trademark of Micrel, Inc.

Ordering Information[1]

Part Number	Package Type	Operating Range	Package Marking
SY898535LKY	K4-20-1	Industrial	898535L with Pb-Free Bar-Line Indicator
SY898535LKYTR[2]	K4-20-1	Industrial	898535L with Pb-Free Bar-Line Indicator

Notes:

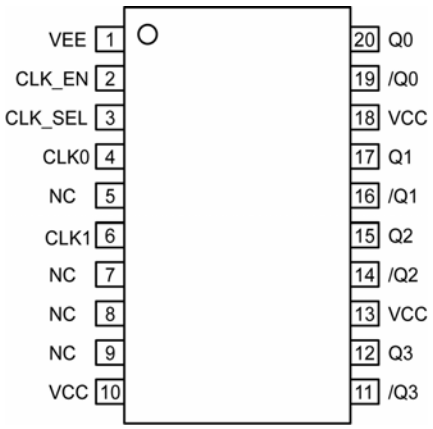
1. Contact factory for die availability. Dice are guaranteed at T_A = 25°C, DC Electricals Only.
2. Tape and Reel.

Truth Table

Inputs			Outputs	
CLK_EN	CLK_SEL	Selected Source	Q0 :Q3	/Q0:/Q3
0	0	CLK0	Disabled : LOW	Disabled : HIGH
0	1	CLK1	Disabled : LOW	Disabled : HIGH
1	0	CLK0	Enabled	Enabled
1	1	CLK1	Enabled	Enabled

hbwhelp@micrel.com or (408) 955-1690

Pin Configuration



20-Pin TSSOP (K4-20-1)

Pin Description

Pin Number	Pin Name	Pin Function
1	V_{EE}	Ground.
2	CLK_EN	Single-Ended Input: This TTL/CMOS input disables and enables the Q0-Q3 outputs. It is internally connected to a 51kΩ pull-up resistor and will default to a logic HIGH state if left open. When disabled, Q goes LOW and /Q goes HIGH. CLK_EN being synchronous, outputs will be enabled/disabled following a rising and a falling edge of the input clock. V_{TH} = is approximately 1.5V.
3	CLK_SEL	Single-Ended Input: This single-ended TTL/CMOS-compatible input selects the input to the multiplexer. If HIGH, selects CLK1 input. When LOW, it selects CLK0 input. Note that this input is internally connected to a 51kΩ pull-down resistor and will default to logic LOW state if left open. V_{TH} = is approximately 1.5V.
4	CLK0	Single-Ended Input: This LVCMOS or LVTTL signal is the input signal to the device. It is internally connected to a 51kΩ pull-down resistor and will default to a logic LOW state if left open. This input is selected when CLK_SEL is set to logic LOW.
6	CLK1	Single-Ended Input: This LVCMOS or LVTTL signal is the input signal to the device. It is internally connected to a 51kΩ pull-down resistor and will default to a logic LOW state if left open. This input is selected when CLK_SEL is set to logic HIGH.
5, 7, 8, 9	NC	Unused Pins
10, 13, 18	VCC	Positive Power Supply Pins: Bypass with 0.1µF||0.01µF low ESR capacitors as close to the V_{CC} pins as possible.
20, 19 17, 16 15, 14 12, 11	Q0, /Q0 Q1, /Q1 Q2, /Q2 Q3, /Q3	LVPECL Differential Output Pairs: Differential buffered output copies the selected input signal. The output swing is typically 800mV. Unused output pairs may be left floating with no impact on jitter. These differential LVPECL outputs are a logic function of the CLK0 and CLK1 inputs. See “Truth Table” below.

Absolute Maximum Ratings[1]

Supply Voltage (V_{CC}) ..... –0.5V to +4.6V
Input Voltage (V_{IN}) ..... –0.5V to V_{CC} +0.5V
LVPECL Output Current (I_{OUT}) .....
  Continuous 50mA
  Surge 100mA
Lead Temperature (soldering, 20 sec.) ..... +260°C
Storage Temperature (T_s) ..... –65°C to 150°C

Operating Ratings[2]

Supply Voltage (V_{CC}) ..... +3.135V to +3.465V
Ambient Temperature (T_A) ..... -40°C to +85°C
Package Thermal Resistance[3]
  TSSOP (θ_{JA})
    Still-Air ..... 73.2°C/W

Power Supply DC Electrical Characteristics[4]

V_{CC} = 3.3V ±5%; T_A = -40°C to +85°C, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{CC}	Power Supply		3.135	3.3	3.465	V
I_{EE}	Power Supply Current	No load, max V_{CC}			55	mA

LVCMOS/LVTTL DC Electrical Characteristics[4]

V_{CC} = 3.3V ±5%; T_A = -40°C to +85°C, unless otherwise stated.

Symbol	Parameter		Condition	Min	Typ	Max	Units
V_{IH}	Input High Voltage	CLK0, CLK1		2		V_{CC} + 0.3V	V
		CLK_EN, CLK_SEL		2		V_{CC} + 0.3V	V
V_{IL}	Input Low Voltage	CLK0, CLK1		-0.3		1.3	V
		CLK_EN, CLK_SEL		-0.3		0.8	V
I_{IH}	Input High Current	CLK0, CLK1, CLK_SEL	V_{IN} = V_{CC} = 3.465V			150	µA
		CLK_EN	V_{IN} = V_{CC} = 3.465V			5	µA
I_{IL}	Input Low Current	CLK0, CLK1, CLK_SEL	V_{IN} = 0V, V_{CC} = 3.465V	-5			µA
		CLK_EN	V_{IN} = 0V, V_{CC} = 3.465V	-150			µA

LVPECL DC Electrical Characteristics[4]

V_{CC} = 3.3V ±5%; T_A = -40°C to +85°C, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{OH}	Output High Voltage[5]		V_{CC} - 1.4		V_{CC} – 0.9	V
V_{OL}	Output Low Voltage[5]		V_{CC} – 2.0		V_{CC} - 1.7	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.6		1.0	V

Notes:

1. Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.
3. θ_{JA} value is determined for a 4-layer board in still air unless otherwise stated.
4. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.
5. 50Ω to V_{CC}-2V terminated outputs.

AC Electrical Characteristics[6]

V_{CC} = 3.3V ±5%; R_L = 50Ω to V_{CC}-2V; T_A = -40°C to +85°C, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
f_{MAX}	Maximum Operating Frequency				235	MHz
t_{PD}	Propagation Delay[7]	f ≤ 266MHz	1.0		1.4	ns
t_{SKEW}	Output-to-Output Skew[8]			11	30	ps
	Part-to-Part Skew[9]				250	ps
t_{JITTER}	Additive Phase Jitter[10]			0.09		ps_{RMS}
t_r, t_f	Output Rise/Fall Time	20% to 80% @ 50MHz	300		700	ps
odc	Output Duty Cycle		48	50	52	%

Notes:

6. High-frequency AC-parameters are guaranteed by design and characterization.
7. Measured from V_{CC}/2 of the input to the differential output crossing point.
8. Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the output differential cross points.
9. Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.
10. Driving only one input clock.

Timing Diagrams

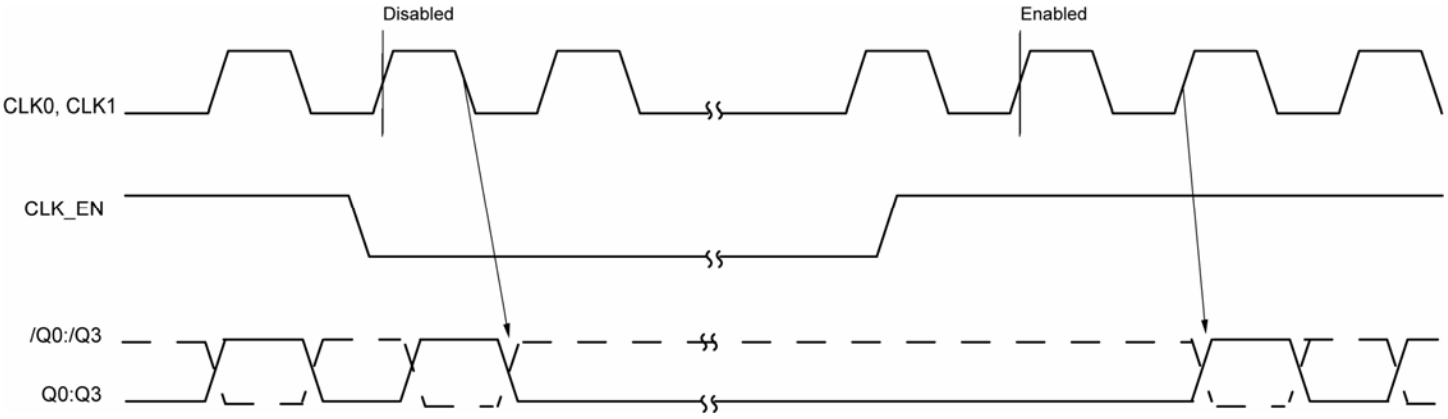


Figure 1a. CLK_EN Timing Diagram

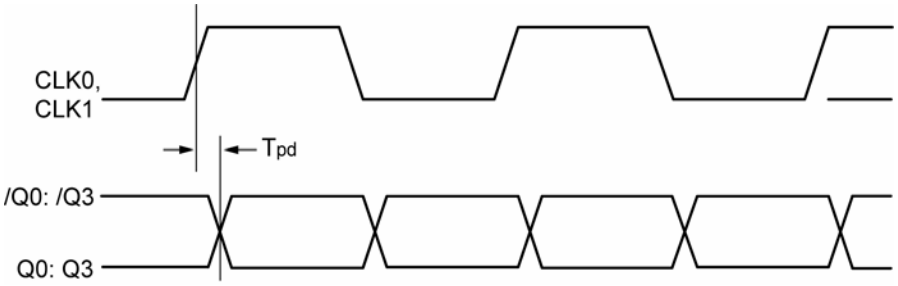


Figure 1b. Propagation Delay

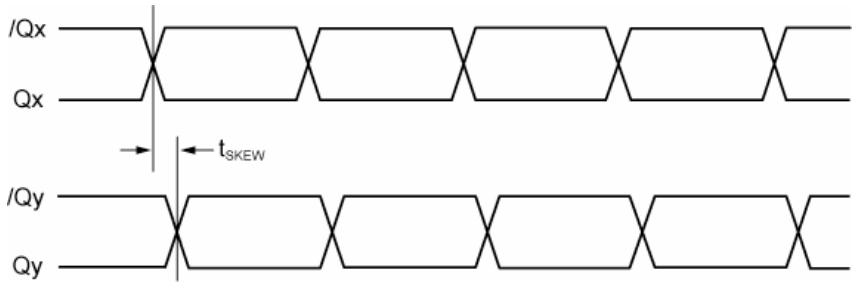
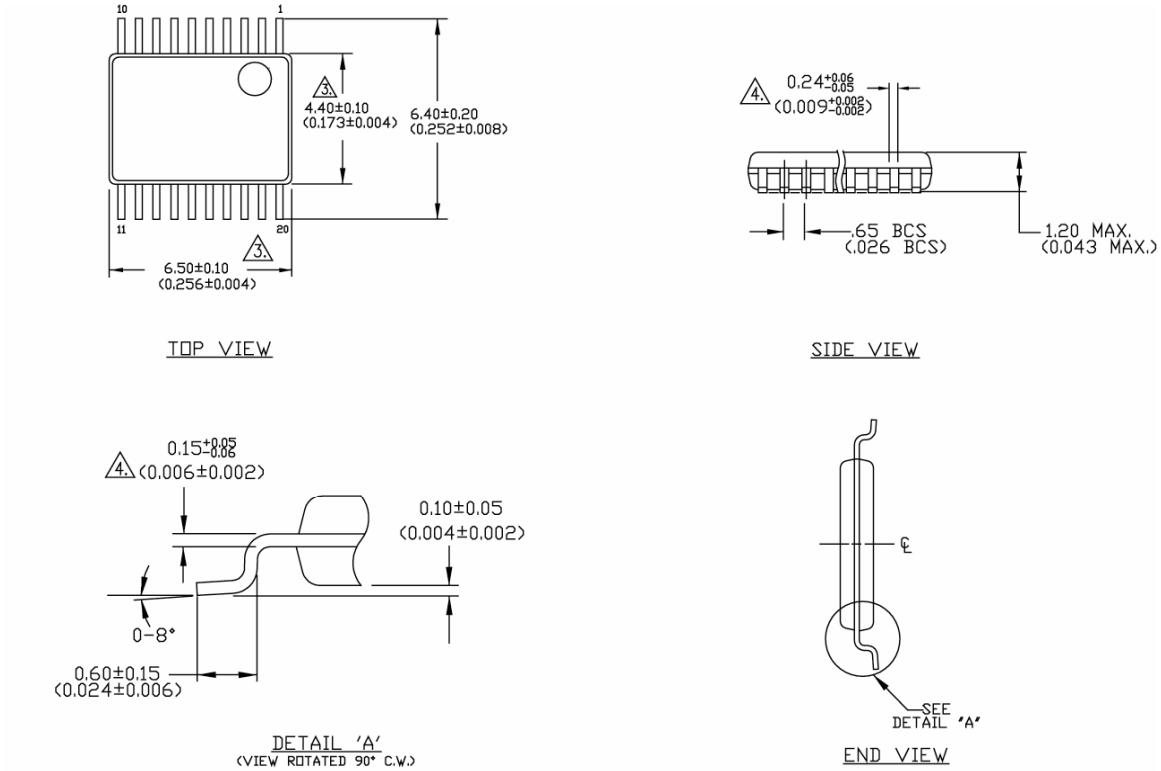


Figure 1c. Output-to-Output Skew

Package Information



NOTES:
1. DIMENSIONS ARE IN MM[INCHES].
2. CONTROLLING DIMENSION: MM.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OF 0.254[0.010] MAX.
4. THIS DIMENSION INCLUDES LEAD FINISH.

20-Pin TSSOP (K4-20-1)

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