AT24MAC402 and AT24MAC602

I²C-Compatible (2-wire) 2-Kbit Serial EEPROM with a Factory-Programmed EUI-48™ or EUI-64™ Address Plus an Embedded Unique 128-bit Serial Number

2-Kbit (256 x 8)

DATASHEET

Standard Serial EEPROM Features

- Low-voltage Operation
  - 1.7V Minimum (V_{CC} = 1.7V to 5.5V)
- Internally Organized as 256 x 8 (2K)
- I²C-compatible (2-wire) Serial Interface
- Schmitt Trigger, Filtered Inputs for Noise Suppression
- Bi-directional Data Transfer Protocol
- 400kHz (1.7V) and 1MHz (2.5V, 5.0V) Compatibility
- Write Protect Pin for Hardware Data Protection of the Entire Array
- Permanent and Reversible Software Write Protection for the First-half of the Array
  - Software Procedure to Verify Write Protect Status
- 16-byte Page Write Modes
  - Partial Page Writes Allowed
- Self-timed Write Cycle (5ms max)
- High-reliability
  - Endurance: 1,000,000 Write Cycles
  - Data Retention: 100 Years
- Green Package Options (PB/Halide-free/RoHS Compliant)
  - 8-lead JEDEC SOIC, 8-lead TSSOP, 8-pad UDFN, and 5-lead SOT23
- Die Sale Options: Wafer Form and Tape and Reel

Enhanced Features in the MAC Serial EEPROM Family

- Factory-programmed EUI-48 or EUI-64 Compatible Address
  - Permanently Locked, Read-only Value
  - Stored in a Separate Memory Area
  - Guaranteed Unique EUI Address
- Custom Programming Services Available
  - Manage and Program Customer's IEEE Assigned OUI
- Unique Factory-programmed 128-bit Serial Number
  - Unique for all Atmel® AT24CS, AT93CS, and AT25S Series Serial EEPROMs
  - Permanently Locked, Read-only Value
  - Stored in a Separate Memory Area

1. Description

The Atmel AT24MAC402 and AT24MAC602 provides 2048 bits of Serial Electrically-Erasable Programmable Read-Only Memory (EEPROM) organized as 256 words of eight bits each and is accessed via an I^2C-compatible (2-wire) serial interface. In addition, AT24MAC402/602 incorporates an easy and inexpensive method to obtain a globally unique MAC or EUI address (EUI-48 or EUI-64). AT24MAC402 is an EUI-48 compatible device that contains a 48-bit EUI address, and AT24MAC602 is an EUI-64 compatible device that contains a 64-bit EUI address.

The EUI-48 and EUI-64 addresses can be assigned as the actual physical address of a system hardware device or node or it can be assigned to a software instance. These addresses are factory programmed by Atmel and permanently write protected in an extended memory block located outside of the standard 2-Kbit bit memory array.

In addition, the AT24MAC402/602 provides the value added feature of a factory-programmed, guaranteed unique 128-bit serial number located in the extended memory block (same area as the EUI address values). The serial number is Atmel factory-programmed and permanently write protected. This 128-bit serial number is compatible with all AT24CS, AT93CS, and AT25S family serial numbers, therefore, providing guaranteed unique serial numbers for any application that is also using Atmel Serial EEPROMs.

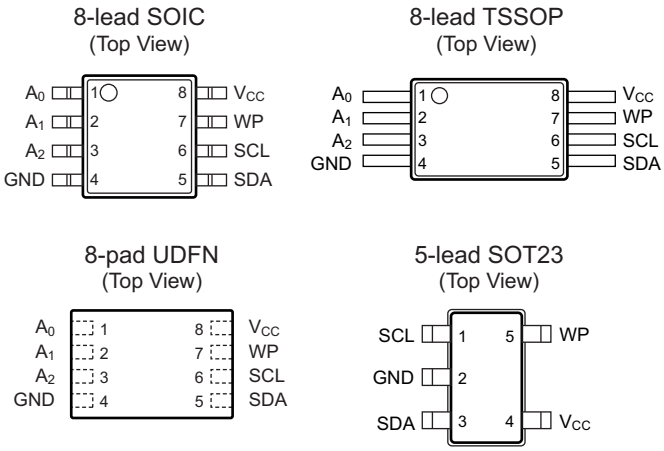
The first-half of the AT24MAC402/602 incorporates a permanent and a reversible software write protection feature while a hardware write protect feature for the entire array is available via an external pin. The permanent software write protection is enabled by sending a special command to the device. This protection cannot be reversed once executed. However, the reversible software write protection can be reversed by sending and executing a special command. The hardware write protection is controlled by the WP pin state and can be used to protect the entire array regardless of whether or not the software write protection has been enabled. The software and hardware write protection features allow the user the flexibility to protect no portion of the memory, the first-half of the memory, or the entire memory array depending on the specific needs of the application.

The device is optimized for use in many industrial and commercial applications where low-power and low-voltage operations are essential. The AT24MAC402/602 is available in space saving 8-lead JEDEC SOIC, 8-lead TSSOP, 8-pad UDFN, and 5-lead SOT23 packages. Both devices operate across a wide supply voltage range from 1.7V to 5.5V V_{CC}.

2. Pin Configurations and Pinouts

Figure 1. Pin Configurations

Pin Name	Function
A_0 - A_2	Address Inputs
SDA	Serial Data
SCL	Serial Clock Input
WP	Write Protect
GND	Ground
V_{CC}	Power Supply



Notes:
1. For use of the 5-lead SOT23, the software A2, A1, and A0 bits in the device address word must be set to zero to properly communicate with the device since the A_2, A_1, and A_0 pins are not bonded out. Some functionality is not possible due to these pins not being available. See "Write Protection" on page 15 for more details.
2. Drawings are not to scale.

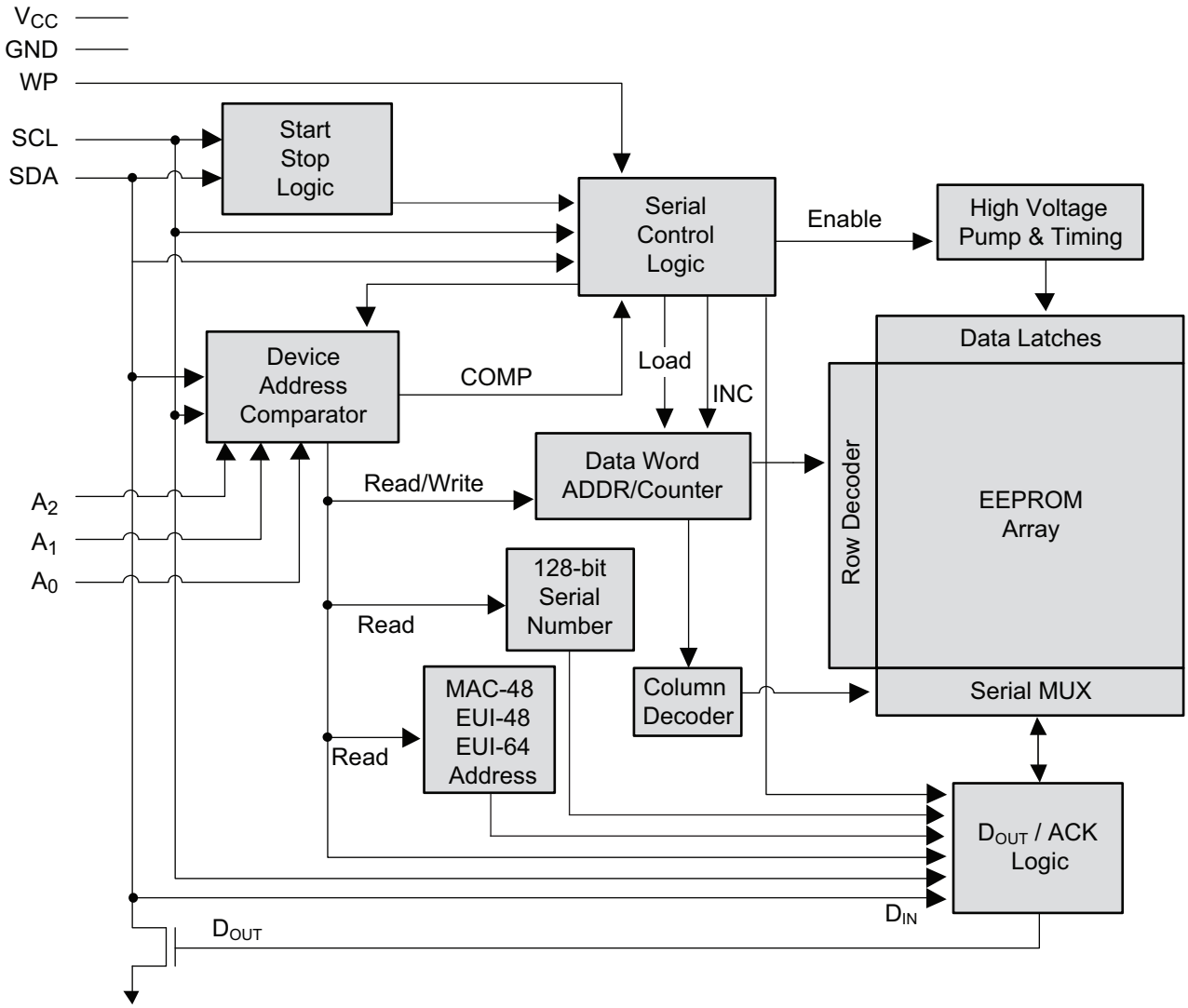
3. Absolute Maximum Ratings*

Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on any pin with respect to ground	-1.0V to +7.0V
Maximum Operating Voltage	6.25V
DC Output Current	5.0mA

*Notice: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

4. Block Diagram

Figure 4-1. Block Diagram



5. Pin Description

Serial Clock (SCL): The SCL input is used to positive edge clock data into each EEPROM device and negative edge clock data out of each device.

Serial Data (SDA): The SDA pin is bidirectional for serial data transfer. This pin is open-drain driven and may be wire-ORed with any number of other open-drain or open collector devices.

Device Addresses (A_0, A_1, A_2): The A_0, A_1, and A_2 pins are device address inputs that are hard wired for the AT24MAC402/602. As many as eight 2K devices may be addressed on a single bus system. Device addressing is discussed in detail in Section 9., “Device Addressing” on page 13.

Write Protect (WP): The AT24MAC402/602 has a Write Protect pin that provides hardware data protection. When the Write Protect pin is connected to ground (GND), normal Read/Write operations to the full array are possible. When the Write Protect pin is connected to V_{CC}, all write operations to the memory are inhibited, but read operations are still possible. However, due to capacitive coupling that may appear during customer applications, Atmel recommends always connecting the WP pins to a known state. When using a pull-up resistor, Atmel recommends using 10kΩ or less. The write protection operation is summarized in Table 5-1 below.

5.1 Write Protection Modes

Table 5-1. Write Protection Modes

WP Pin Status	Permanent Write Protect Register	Reversible Write Protect Register	Part of the Array Write Protected
V_{CC}	—	—	Full Array (2K)
GND or Floating	Not Programmed	Not Programmed	Normal Read/Write
GND or Floating	Programmed	—	First-half of Array
GND or Floating	—	Programmed	First-half of Array

6. Electrical Characteristics

6.1 Pin Capacitance

Table 6-1. Pin Capacitance[1]

Symbol	Test Condition	Max	Units	Conditions
$C_{I/O}$	Input/Output Capacitance (SDA)	8	pF	$V_{I/O}$ = 0V
C_{IN}	Input Capacitance (A_0, A_1, A_2, SCL)	6	pF	V_{IN} = 0V

Note: 1. This parameter is characterized and is not 100% tested.

6.2 DC Characteristics

Table 6-2. DC Characteristics

Applicable over recommended operating range from: T_{AI} = -40°C to +85°C, V_{CC} = 1.7V to 5.5V (unless otherwise noted).

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
V_{CC}	Supply Voltage		1.7		5.5	V
I_{CC1}	Supply Current V_{CC} = 5.0V	Read at 400kHz		0.4	1.0	mA
I_{CC2}	Supply Current V_{CC} = 5.0V	Write at 400kHz		2.0	3.0	mA
I_{SB1}	Standby Current V_{CC} = 1.7V	V_{IN} = V_{CC} or V_{SS}			1.0	µA
I_{SB2}	Standby Current V_{CC} = 2.5V	V_{IN} = V_{CC} or V_{SS}			2.0	µA
I_{SB3}	Standby Current V_{CC} = 5.5V	V_{IN} = V_{CC} or V_{SS}, A_0 = V_{SS}			6.0	µA
I_{LI}	Input Leakage Current	V_{IN} = V_{CC} or V_{SS}		0.10	3.0	µA
I_{LO}	Output Leakage Current	V_{OUT} = V_{CC} or V_{SS}		0.05	3.0	µA
V_{IL}	Input Low Level[1]		-0.6		V_{CC} x 0.3	V
V_{IH}	Input High Level[1]		V_{CC} x 0.7		V_{CC} + 0.5	V
V_{OL1}	Output Low Level V_{CC} = 1.7V	I_{OL} = 0.15mA			0.2	V
V_{OL2}	Output Low Level V_{CC} = 3.0V	I_{OL} = 2.1mA			0.4	V

Note: 1. V_{IL} min and V_{IH} max are reference only and are not tested.

6.3 AC Characteristics

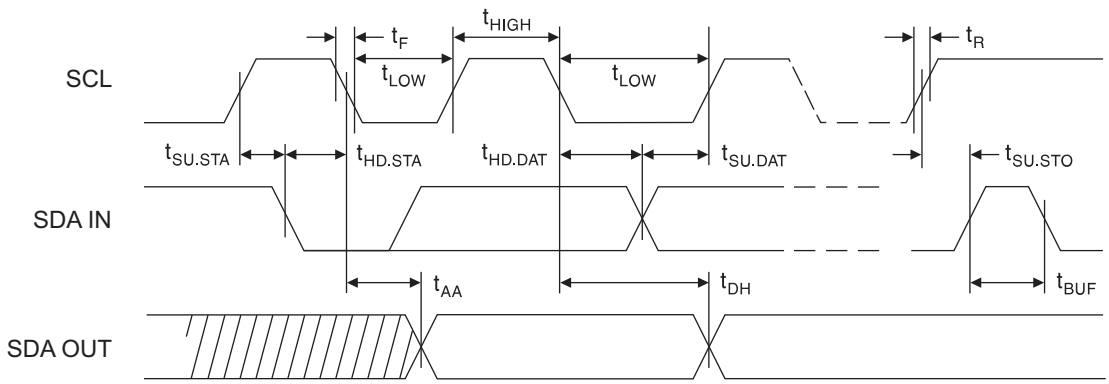
Table 6-3. AC Characteristics

Symbol	Parameter	1.7V		2.5V, 5.0V		Units
		Min	Max	Min	Max	
f_{SCL}	Clock Frequency, SCL		400		1000	kHz
t_{LOW}	Clock Pulse Width Low	1.2		0.4		µs
t_{HIGH}	Clock Pulse Width High	0.6		0.4		µs
t_I	Noise Suppression Time(1)		100		50	ns
t_{AA}	Clock Low to Data Out Valid	0.1	0.9	0.05	0.55	µs
t_{BUF}	Time the bus must be free before a new transmission can start.(1)	1.3		0.5		µs
$t_{HD.STA}$	Start Hold Time	0.6		0.25		µs
$t_{SU.STA}$	Start Set-up Time	0.6		0.25		µs
$t_{HD.DAT}$	Data In Hold Time	0		0		µs
$t_{SU.DAT}$	Data In Set-up Time	100		100		ns
t_R	Inputs Rise Time(1)		0.3		0.3	µs
t_F	Inputs Fall Time(1)		300		100	ns
$t_{SU.STO}$	Stop Set-up Time	0.6		0.25		µs
t_{DH}	Data Out Hold Time	50		50		ns
t_{WR}	Write Cycle Time		5		5	ms
Endurance(1)	25°C, Page Mode, 3.3V	1,000,000				Write cycles

Note: 1. This parameter is characterized and is not 100% tested.

Figure 6-1. Bus Timing

SCL Serial Clock, SDA: Serial Data I/O

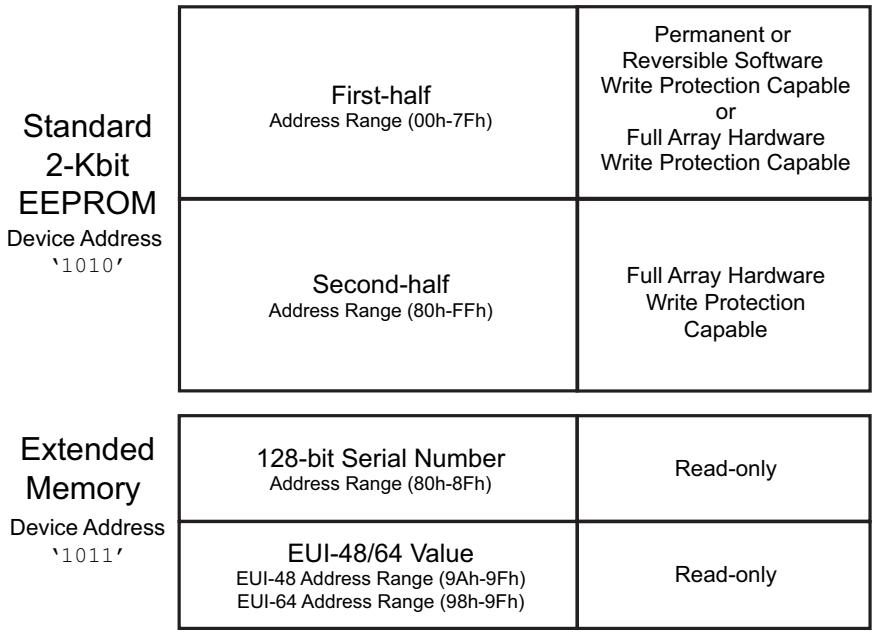


7. Memory Organization

AT24MAC402/602, 2K Serial EEPROM: The 2-Kbit memory array is internally organized as 16 pages of 16 bytes of EEPROM each. Random word addressing requires a 8-bit data word address.

EUI Address and Serial Number: The 48-bit EUI address in the AT24MAC402 and the 64-bit EUI address in the AT24MAC602 are located in the extended memory block. In addition, the serial number data is also located in the extended memory block as shown below in Figure 7-1. These EUI-48 or EUI-64 addresses are stored in a dedicated read-only EEPROM memory block located outside the standard 2K memory array as shown below. This means the full standard 2-Kbit EEPROM array is available for use as opposed to solutions where only half of the EEPROM memory array is available for application usage.

Figure 7-1. Memory Organization



The EUI-48 and EUI-64 address fields contain either six or eight bytes respectively. The first three bytes of the EUI read-only address field are called the Organizationally Unique Identifier (OUI) and the IEEE Registration Authority has assigned FCC23Dh as the Atmel, OUI.

Following the OUI, the remaining bytes are called the Extension Identifier and will be either three bytes or five bytes depending on if it is an EUI-48 address (AT24MAC402) or EUI-64 address (AT24MAC602). Atmel generates this unique 24-bit/40-bit data value along with the OUI to guarantee a globally unique EUI address value and programs it at the factory before permanently locking the extended memory region.

7.1 EUI-48 Support

The EUI-48 address is stored in the last six bytes of the AT24MAC402's extended memory block as shown in Table 7-1. For information on the protocol to read the EUI-48 value, see Section 9., "Device Addressing" on page 13 and Section 12., "Read Operations" on page 19.

Table 7-1. 48-Bit EUI Address Memory Map Example

	48-Bit EUI					
Description	**24-Bit OUI**			**24-Bit Extension Identifier**		
Memory Address	9Ah	9Bh	9Ch	9Dh	9Eh	9Fh
EUI Data Value	FCh	C2h	3Dh	Byte 1	Byte 2	Byte 3

Using an EUI-48 Value in an EUI-64 Application: An EUI-64 compatible value can be generated from the EUI-48 value contained in the AT24MAC402 by concatenating the 24-bit OUI, an FFFEh data value, and the 24-bit Extension Identifier. This is commonly referred to as an Encapsulated EUI-48 value. However, Atmel recommends using the AT24MAC602 which contains a true EUI-64 value so that post read processing is not required by the application.

7.2 EUI-64 Support

For applications that utilize an EUI-64 standard, the EUI-64 address is stored in the last eight bytes of the AT24MAC602's extended memory block. Similar to EUI-48, the EUI-64 standard consists of the same three byte OUI coupled with a five byte extension identifier (Table 7-2). Atmel generates this unique 40-bit data value coupled with the OUI to guarantee a globally unique 64-bit EUI value and requires no additional data manipulation like other solutions where the application must manually insert a two byte FFFEh value in between the OUI and Extension Identifier. For information on how to read the EUI read protocol, see See Section 9., "Device Addressing" on page 13 and "Read Operations" on page 19.

Table 7-2. 64-Bit EUI Address Memory Map Example

	64-Bit EUI							
Description	**24-Bit OUI**			**40-Bit Extension Identifier**				
Memory Address	98h	99h	9Ah	9Bh	9Ch	9Dh	9Eh	9Fh
EUI Data Value	FCh	C2h	3Dh	Byte 1(1)	Byte 2(1)	Byte 3	Byte 4	Byte 5

Note: 1. The data values FFFEh and FFFFh are prohibited beginning from the 40-bit Extension Identifier in Byte 1 and Byte 2. These values are reserved for denoting an encapsulated MAC-48 or EUI-48 value for use in an EUI-64 environment.

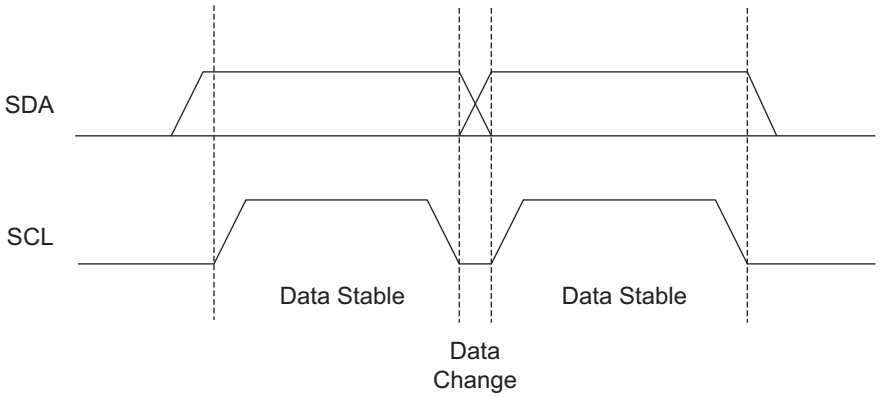
7.3 Non-Atmel OUI Programming Option

For customers with their own IEEE-assigned OUI or Company ID, Atmel offers the time saving option to manage and deliver custom AT24MAC402/602 devices with their EUI-48/64 values uniquely pre-programmed at delivery. Contact your local Atmel Sales Office for additional information.

8. Device Operation

Clock and Data Transitions: The SDA pin is normally pulled high with an external component such as a pull-up resistor. Data on the SDA pin may change only during SCL low time periods. Data changes during SCL high periods will indicate a Start or Stop condition as defined below.

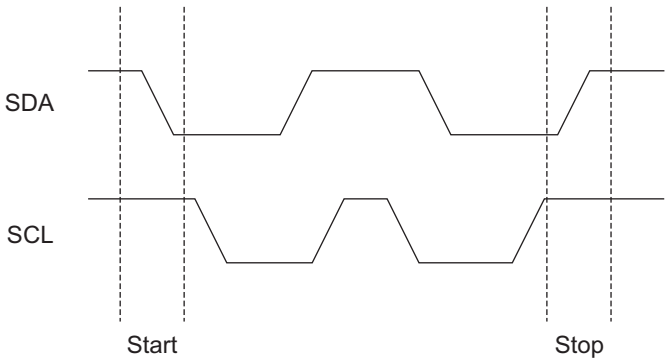
Figure 8-1. Data Validity



Start Condition: A high-to-low transition of SDA with SCL high is a Start condition which must precede any other command.

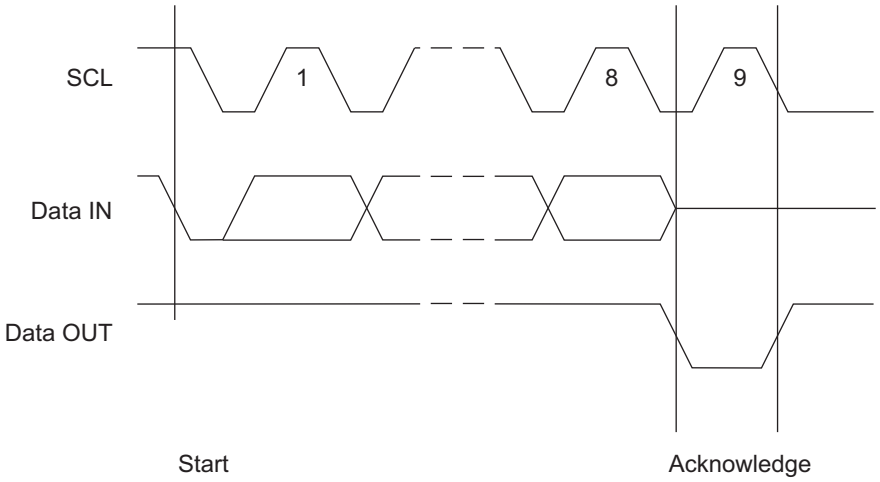
Stop Condition: A low-to-high transition of SDA with SCL high is a Stop condition. After a read sequence, the stop command will place the EEPROM in a standby power mode.

Figure 8-2. Start and Stop Condition



Acknowledge: All addresses and data words are serially transmitted to and from the EEPROM in 8-bit words. The EEPROM sends a zero to acknowledge that it has received each word. This happens during the ninth clock cycle.

Figure 8-3. Output Acknowledge



Standby Mode: The AT24MAC402/602 features a low-power standby mode which is enabled upon

- Power-up or
- After the receipt of the Stop condition and the completion of any internal operations.

2-Wire Software Reset: After an interruption in protocol, power loss or system reset, any 2-wire part can be reset by following these steps:

1. Create a Start condition (if possible).
2. Clock nine cycles.
3. Create another Start condition followed by Stop condition as shown below.

The device should be ready for the next communication after above steps have been completed. In the event that the device is still non-responsive or remains active on the SDA bus, a power cycle must be used to reset the device.

Figure 8-4. Software Reset

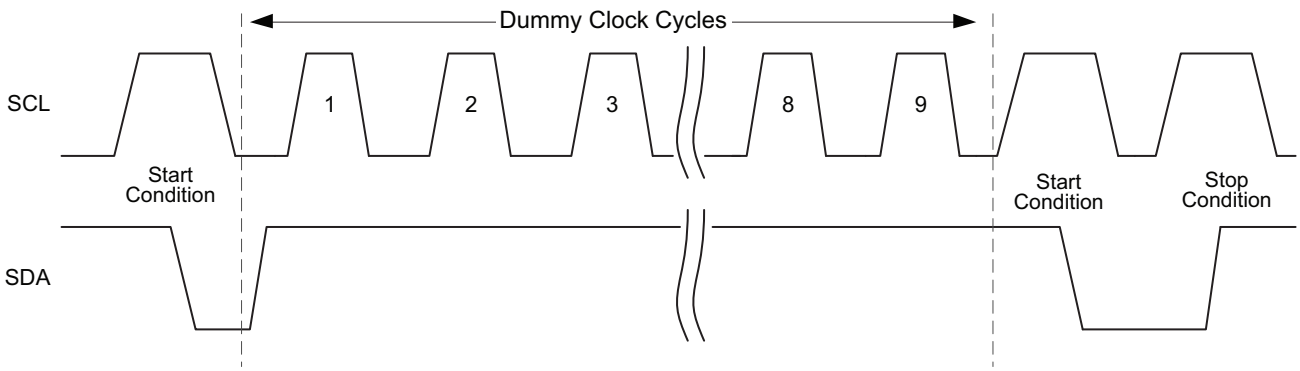
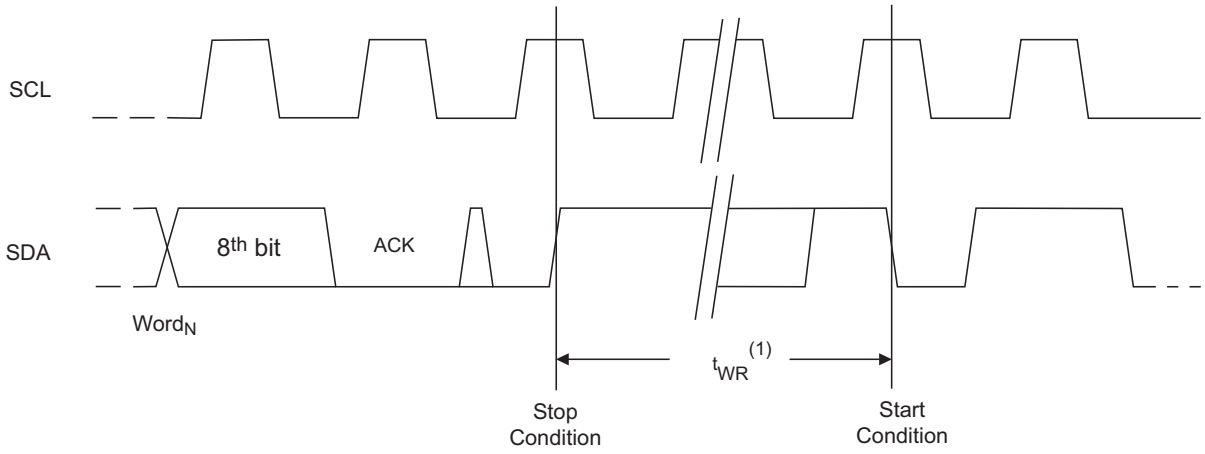


Figure 8-5. Write Cycle Timing

SCL Serial Clock, SDA: Serial Data I/O



Note: 1. The write cycle time t_{WR} is the time from a valid Stop condition of a write sequence to the end of the internal clear/write cycle.

9. Device Addressing

Standard EEPROM Access: The 2K EEPROM requires an 8-bit device address word following a start condition to enable the chip for a read or write operation (see Figure 10-1 on page 14).

The device address word consists of a mandatory one-zero sequence for the first four most-significant bits '1010' (Ah) for normal read and write operations and '0110' (6h) for writing to the Software Write Protect Register.

The next three bits in the protocol sequence are the A2, A1, and A0 device address bits. These three bits must match their corresponding hard-wired input pins A_2, A_1, and A_0 in order for the part to acknowledge.

The eighth bit of the device address is the read/write operation select bit. A read operation is initiated if this bit is high, and a write operation is initiated if this bit is low. Upon a compare of the device address, the EEPROM will output a zero. If a compare is not made, the device will return to a standby state. The device will not acknowledge if the Write Protect Register has been programmed and the control code is '0110' (6h).

Serial Number Access: The AT24MAC402/602 incorporates an extended memory block containing a factory-programmed 128-bit serial number. Access to this memory location is obtained by beginning the device address word with a '1011' (Bh) sequence. The behavior of the next three bits (A2, A1, and A0) remain the same as during a standard memory addressing sequence.

The eighth bit of the device address needs to be set to a one to read the serial number. A zero in this bit position, other than during a dummy write sequence to set the address pointer, will result in a unknown condition and behavior. Writing or altering the 128-bit serial number is not possible as it is permanently write protected. Further specific protocol is needed to address the serial number feature of the part. For more details on accessing this special feature, See Section 12., “Read Operations” on page 19.

EUI Address Access: The AT24MAC402/602 utilizes an extended memory block containing a factory-programmed read-only EUI-48 or EUI-64 address respectively. Access to this memory block is obtained by beginning the device address word with a '1011' (Bh) sequence. The behavior of the next three bits (A2, A1, and A0) remain the same as during a standard memory addressing sequence.

The eighth bit of the device address needs to be set to a one to read the EUI address. A zero in this bit position, other than during a dummy write sequence to set the address pointer, will result in a unknown condition and behavior. Attempting to write or alter the EUI address is not possible as it is permanently write protected. Further specific protocol is needed to address this feature of the part. For more details on accessing this special feature, see Section 12., “Read Operations”.

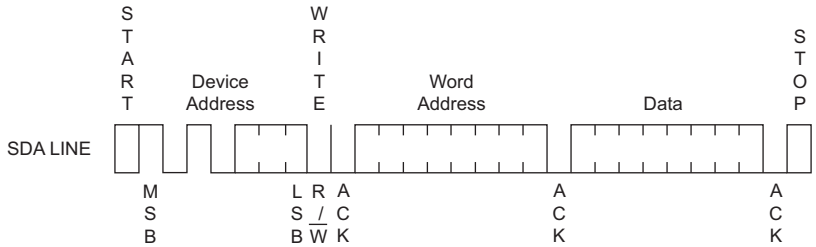
Table 9-1. Device Address

Access Area	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EEPROM	1	0	1	0	A_2	A_1	A_0	R/$\overline{W}$
EUI or Serial Number Read	1	0	1	1	A_2	A_1	A_0	1

10. Write Operations

Byte Write: A Byte Write operation requires an 8-bit data word address following the device address word and acknowledgment. Upon receipt of this address, the EEPROM will again acknowledge or respond with a zero and then clock in the first 8-bit data word. Following receipt of the 8-bit data word, the EEPROM will output a zero and the addressing device, such as a microcontroller, must terminate the write sequence with a Stop condition. At this time, the EEPROM enters an internally-timed write cycle, t_{WR}, to the nonvolatile memory. All inputs are disabled during this write cycle and the EEPROM will not respond until the write is complete. The device will acknowledge a write command, but not write the data if the software or hardware write protection has been enabled. The write cycle time must be observed even when the write protection is enabled.

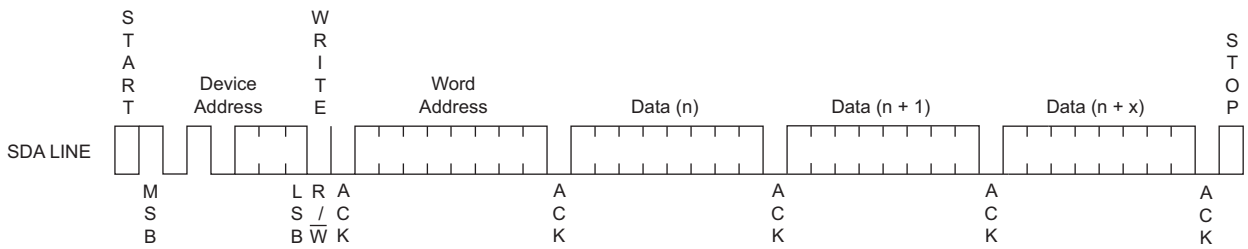
Figure 10-1. Byte Write



Page Write: The AT24MAC402/602 is capable of a 16-byte Page Write. A Page Write is initiated by the same method as a Byte Write, but the microcontroller does not send a Stop condition after the first data word is clocked in. Instead, after the EEPROM acknowledges receipt of the first data word, the microcontroller can transmit up to fifteen more data words. The EEPROM will respond with a zero after each data word received. The microcontroller must terminate the page write sequence with a Stop condition.

The lower four data word address bits are internally incremented following the receipt of each data word. The higher data word address bits are not incremented, retaining the memory page row location. When the internally generated word address reaches the page boundary, the next byte is placed at the beginning of the same page. If more than sixteen data words are transmitted to the EEPROM, the data word address will roll-over and previous data will be overwritten. The address roll-over during write is from the last byte of the current page to the first byte of the same page. The device will acknowledge a write command, but will not write the data if the software or hardware write protection has been enabled. The write cycle time must be observed even when the write protection is enabled.

Figure 10-2. Page Write



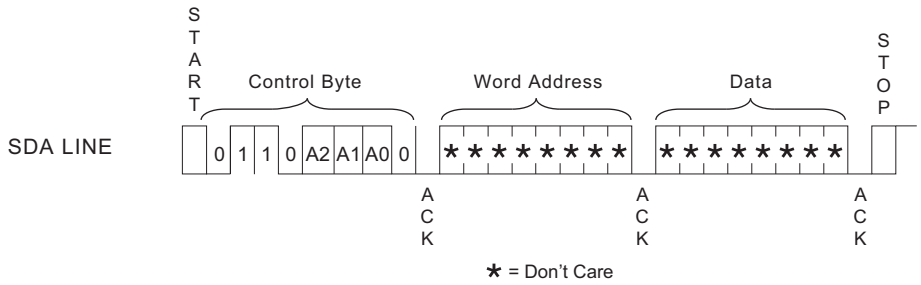
Acknowledge Polling: Once the internally-timed write cycle has started and the EEPROM inputs are disabled, acknowledge polling can be initiated. This involves sending a Start condition followed by the device address word. The read/write bit is representative of the operation desired. Only if the internal write cycle has completed will the EEPROM respond with a zero allowing the read or write sequence to continue.

11. Write Protection

Once enabled, the Software Write Protection write protects only the first-half of the array (00h - 7Fh) while the hardware write protection, via the WP pin, is used to protect the entire array (see Table 11-2 on page 16).

Permanent Software Write Protection (PSWP): The Permanent Software Write Protection is enabled by sending a command to the device, similar to a normal write command, which programs the Permanent Write Protect Register. This must be done with the WP pin low. The Write Protect Register is programmed by sending a write command with the device address of '0110' (6h) instead of '1010' (Ah) with the address and data bit(s) being don't cares. The write cycle time must be observed. Once the permanent software write protection has been enabled, the device will no longer acknowledge the '0110' (6h) control byte and cannot be reversed even if the device is powered down. The Permanent Software Write Protection can only be invoked on a SOT23 packaged device with the A2, A1, and A0 bits set to zero.

Figure 11-1. Setting Permanent Write Protect Register (PSWP)



Reversible Software Write Protection (RSWP): The Reversible Software Write Protection is enabled by sending a command to the device, similar to a normal write command, which programs the Reversible Write Protect Register. This must be done with the WP pin low. The Reversible Write Protect Register is programmed by sending a write command '01100010' (62h) with pins A_2 and A_1 tied to ground or not connected and the A_0 pin connected to V_{HV} (see Figure 11-2 and Table 11-1 on page 16). The Reversible Write Protection Register or Write Protection can be reversed by sending a command '01100110' (66h) with the A_2 pin tied to ground or no connect, the A_1 pin tied to V_{CC} and the A_0 pin tied to V_{HV} (see Figure 11-3 on page 16 and Table 11-1 on page 16). Due to the unavailability of the A_2, A_1, and A_0 pins, the Reversible Software Write Protection function is not available on the SOT23 package.

Figure 11-2. Setting Reversible Write Protect Register (RSWP)

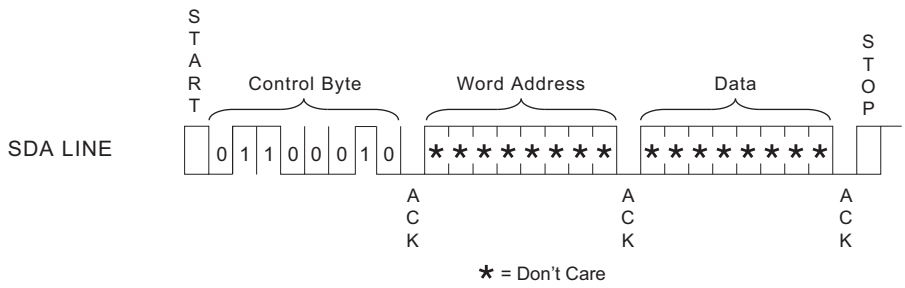


Figure 11-3. Clearing Reversible Write Protect Register (RSWP)

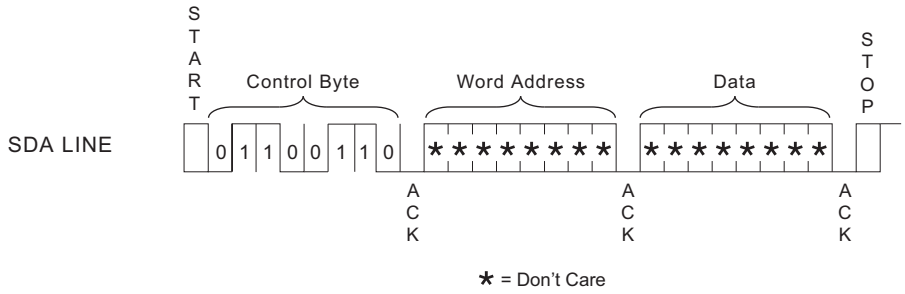


Table 11-1. V_{HV}

	Min	Max	Units
V_{HV}	7	10	V

Note: $V_{HV} - V_{CC} > 4.8V$

Hardware Write Protection: The WP pin can be connected to V_{CC}, GND, or left floating. Connecting the WP pin to V_{CC} will write protect the entire array regardless of whether or not the Software Write Protection has been enabled or invoked (see Table 11-3 on page 17 and Table 11-4 on page 18). The Software Write Protection Register cannot be programmed when the WP pin is connected to V_{CC}. If the WP pin is connected to GND or left floating, the write protection mode is determined by the status of the Software Write Protect Register.

Table 11-2. Write Protection

	Pin			Preamble							R/$\overline{W}$
Command	A_2	A_1	A_0	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Set PSWP	A_2	A_1	A_0	0	1	1	0	A_2	A_1	A_0	0
Set RSWP	0	0	V_{HV}	0	1	1	0	0	0	1	0
Clear RSWP	0	V_{CC}	V_{HV}	0	1	1	0	0	1	1	0

Table 11-3. WP Connected to GND or Floating

WP Connected to GND or Floating					
Command	R/$\overline{W}$ Bit	Permanent Write Protect Register PSWP	Reversible Write Protect Register RSWP	Response from Device	Action from Device
1010	R	X	X	ACK	Read Array.
1010	W	Programmed	X	ACK	Can write to second-half (80h - FFh) only.
1010	W	X	Programmed	ACK	Can write to second-half (80h - FFh) only.
1010	W	Not Programmed	Not Programmed	ACK	Can write to full array.
Read PSWP	R	Programmed	X	No ACK	STOP – Indicates Permanent Write Protect Register is programmed.
Read PSWP	R	Not Programmed	X	ACK	Data read out is undefined. Indicates PSWP Register is not programmed.
Set PSWP	W	Programmed	X	No ACK	STOP – Indicates Permanent Write Protect Register is programmed.
Set PSWP	W	Not Programmed	X	ACK	Program Permanent Write Protect Register (irreversible).
Read RSWP	R	X	Programmed	No ACK	STOP – Indicates Reversible Write Protect Register is programmed.
Read RSWP	R	X	Not Programmed	ACK	Data read out is undefined. Indicates RSWP Register is not programmed.
Set RSWP	W	X	Programmed	No ACK	STOP – Indicates Reversible Write Protect Register is programmed.
Set RSWP	W	X	Not Programmed	ACK	Program Reversible Write Protect Register (reversible).
Clear RSWP	W	Programmed	X	No ACK	STOP – Indicates Permanent Write Protect Register is programmed.
Clear RSWP	W	Not Programmed	X	ACK	Clear (unprogram) Reversible Write Protect Register (reversible).

Table 11-4. WP Connected to V_{CC}

WP Connected to V_{CC}					
Command	R/$\overline{W}$ Bit	Permanent Write Protect Register PSWP	Reversible Write Protect Register RSWP	Response from Device	Action from Device
1010	R	X	X	ACK	Read array.
1010	W	X	X	ACK	Device is write protected.
Read PSWP	R	Programmed	X	No ACK	STOP – Indicates pErmanent Write Protect Register is programmed.
Read PSWP	R	Not Programmed	X	ACK	Data read out is undefined. Indicates PSWP Register is not programmed.
Set PSWP	W	Programmed	X	No ACK	STOP – Indicates Permanent Write Protect Register is programmed.
Set PSWP	W	Not Programmed	X	ACK	Cannot program write protect registers.
Read RSWP	R	X	Programmed	No ACK	STOP – Indicates Reversible Write Protect Register is programmed.
Read RSWP	R	X	Not Programmed	ACK	Data read out is undefined. Indicates RSWP Register is not programmed.
Set RSWP	W	X	Programmed	No ACK	STOP – Indicates Reversible Write Protect Register is programmed.
Set RSWP	W	X	Not Programmed	ACK	Cannot program write protect registers.
Clear RSWP	W	Programmed	X	No ACK	STOP – Indicates Permanent Write Protect Register is programmed.
Clear RSWP	W	Not Programmed	X	ACK	Cannot write to Write Protect Registers.

12. Read Operations

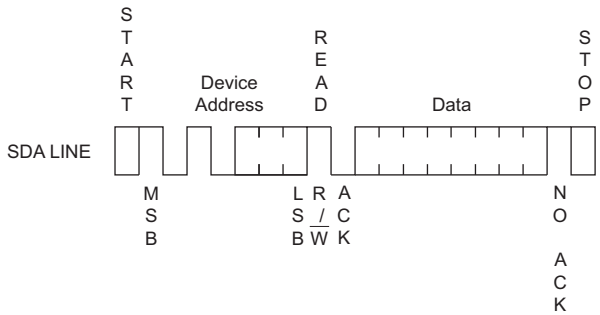
Read operations are initiated the same way as write operations with the exception that the read/write select bit in the device address word is set to one. There are three types of read operations:

- Current Address Read
- Random Address Read
- Sequential Read

Current Address Read: The internal data word address counter maintains the last address accessed during the last read or write operation, incremented by one. This address stays valid between operations as long as V_{CC} to the chip is maintained. The address roll-over during read is from the last byte of the last memory page to the first byte of the first page.

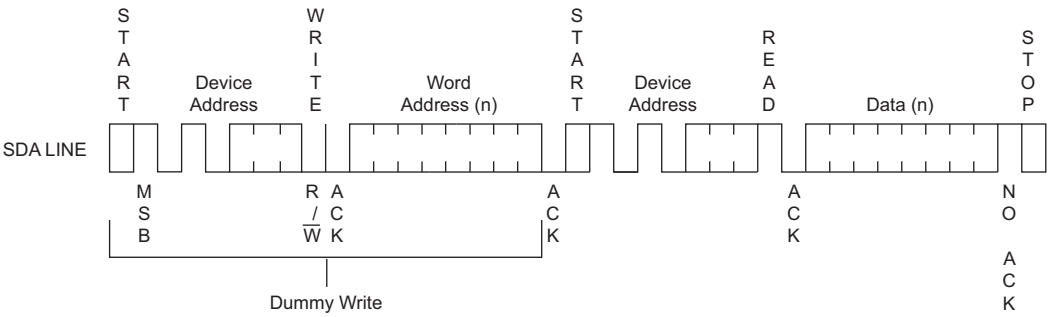
Once the device address with the read/write select bit set to one is clocked in and acknowledged by the EEPROM, the current address data word is serially clocked out. To end the command, the microcontroller does not respond with a zero but does generate a Stop condition in the subsequent clock cycle.

Figure 12-1. Current Address Read



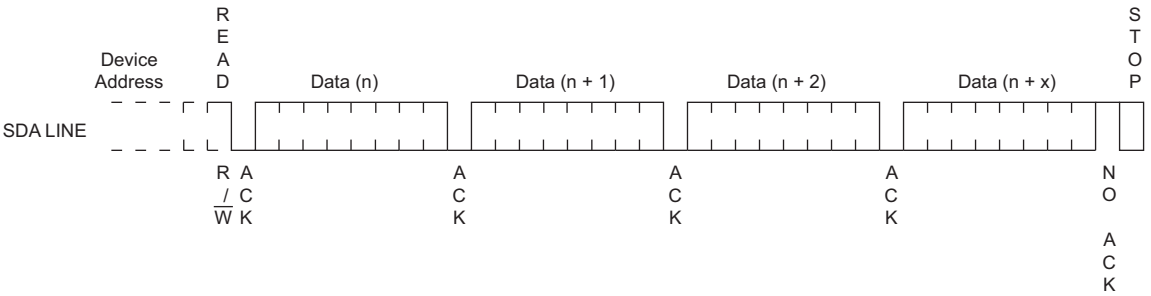
Random Read: A Random Read requires a dummy byte write sequence to load in the data word address. Once the device address word and data word address are clocked in and acknowledged by the EEPROM, the microcontroller must generate another Start condition. The microcontroller now initiates a current address read by sending a device address with the read/write select bit high. The EEPROM acknowledges the device address and serially clocks out the data word. To end the random read sequence, the microcontroller does not respond with a zero but does generate a Stop condition in the subsequent clock cycle.

Figure 12-2. Random Read



Sequential Read: Sequential reads are initiated by either a current address read or a random address read. After the microcontroller receives a data word, it responds with an acknowledge. As long as the Serial EEPROM receives an acknowledge, it will continue to increment the data word address and serially clock out sequential data words. When the memory address limit is reached, the data word address will “roll over” and the sequential read will continue. The sequential read operation is terminated when the microcontroller does not respond with a zero but does generate a following Stop condition in the subsequent clock cycle.

Figure 12-3. Sequential Read



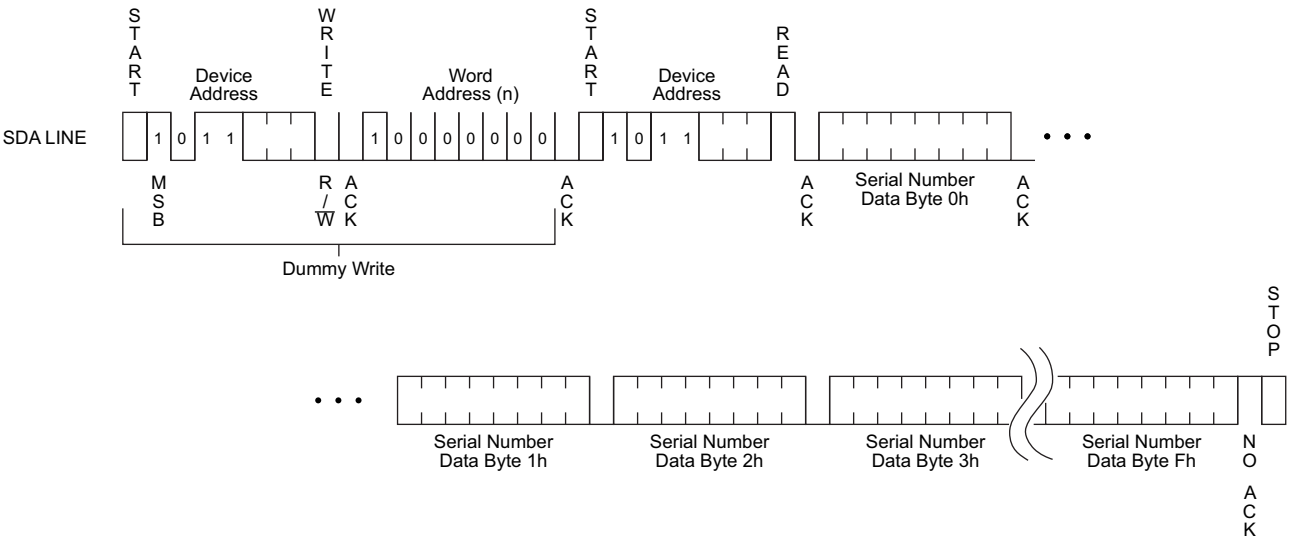
Serial Number Read: Reading the serial number is similar to the sequential read sequence but requires use of a different device address value as shown in Figure 12-4, followed by a dummy write, and the use of a specific word address.

Note: The entire 128-bit value must be read from the starting address of the serial number block to guarantee a unique number.

Since the address pointer of the device is shared between the regular EEPROM array and the serial number block, a dummy write sequence, as part of a Random Read or Sequential Read protocol, should be performed to ensure the address pointer is set to zero. A Current Address Read of the serial number block is supported but if the previous operation was to the EEPROM array, the address pointer will retain the last location accessed, incremented by one. Reading the serial number from a location other than the first address of the block will not result in a unique serial number.

Additionally, the most-significant four bits of the word address must be `'1000'` (8h). Thus, if the application desires to read the pre-programmed serial number, then the corresponding word address input would be 80h. If a word address other than 80h is used, then the device will output undefined data.

Figure 12-4. Serial Number Read



EUI Address Read: Reading the EUI address is very similar to the Serial Number read sequence with the exceptions of the starting word address and the amount of data bytes clocked out (see Figure 12-5 on page 21). The EUI read sequence requires use of the device address values as shown in Table 10-1 on page 14, followed by a dummy write, and the use of a specific word address from Figure 7-1 on page 9 for EUI-48 standard or Figure 7-2 on page 9 for EUI-64 standard.

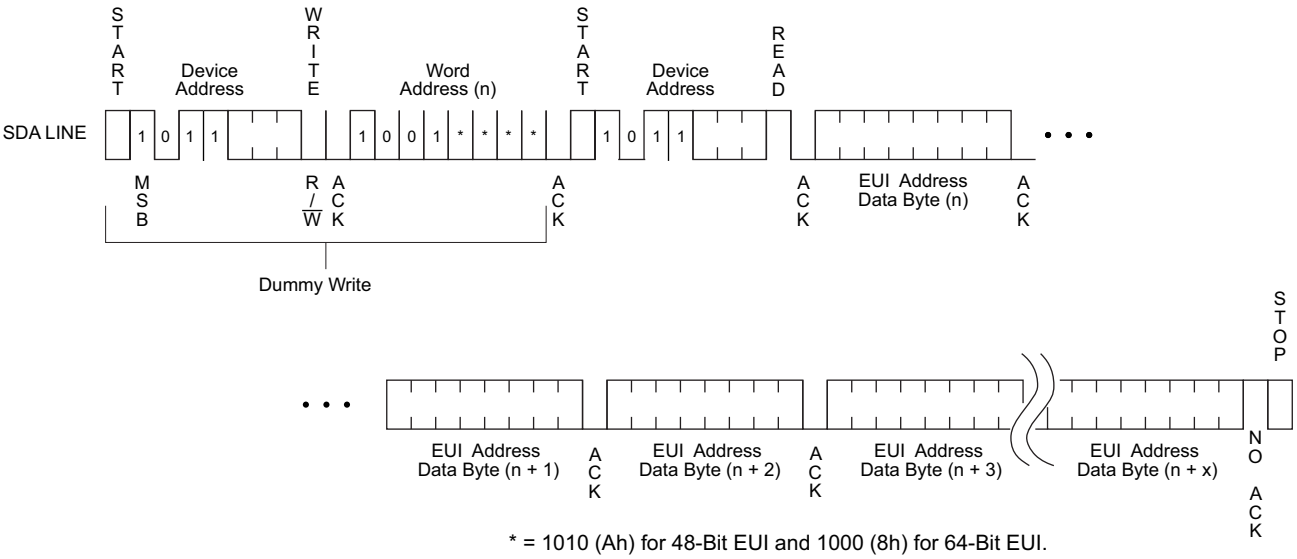
Note: The entire six byte (EUI-48) or eight byte (EUI-64) values must be read from the respective starting address of either 9Ah (for EUI-48) or 98h (for EUI-64) to guarantee a unique EUI data value.

Since the address pointer of the device is shared between the regular EEPROM array, the serial number block, and the EUI block, a dummy write sequence should be performed to ensure the address pointer is set to the correct starting EUI-48 or EUI-64 address. Random reads of the EUI block are supported, but if the previous operation was to the EEPROM array or to the serial number block, the address pointer will retain the last location accessed, incremented by one. Reading the EUI data from a location other than the correct starting EUI address of the block will not result in a unique EUI data value.

Additionally, the most-significant four bits of the word address must be `'1001'` (9h). Therefore, if the application desires to read the pre-programmed EUI value, then the corresponding word address input would be 9Ah in the AT24MAC402 and 98h for the AT24MAC602. If a word address other than 9Ah or 98h respectively is used, the device will output undefined data.

Once the EUI block of six or eight bytes of data have been clocked out of the device, the EUI read operation will end when the microcontroller does not respond with a zero or acknowledge, but then creates a Stop condition. It is important to note that the data word address will not roll-over back to the beginning of the respective EUI starting address. If the read operation continues past the last EUI data value, the data word address will roll-over back to the beginning of the extended memory block where the 128-bit serial number will begin to read out. Therefore, every EUI read sequence attempt requires a valid starting address in the dummy write sequence as shown in Figure 12-5.

Figure 12-5. EUI Address Read



Checking the Permanent Write Protect Register (PSWP) Status: Determining the status of the Permanent Write Protect Register can be accomplished by sending a similar command to the device as was used when programming the register, except the R/W bit must be set to one. If the device responds with an acknowledge, the Permanent Write Protect Register has not been programmed; otherwise, it has been programmed and the first-half of the array is permanently write protected.

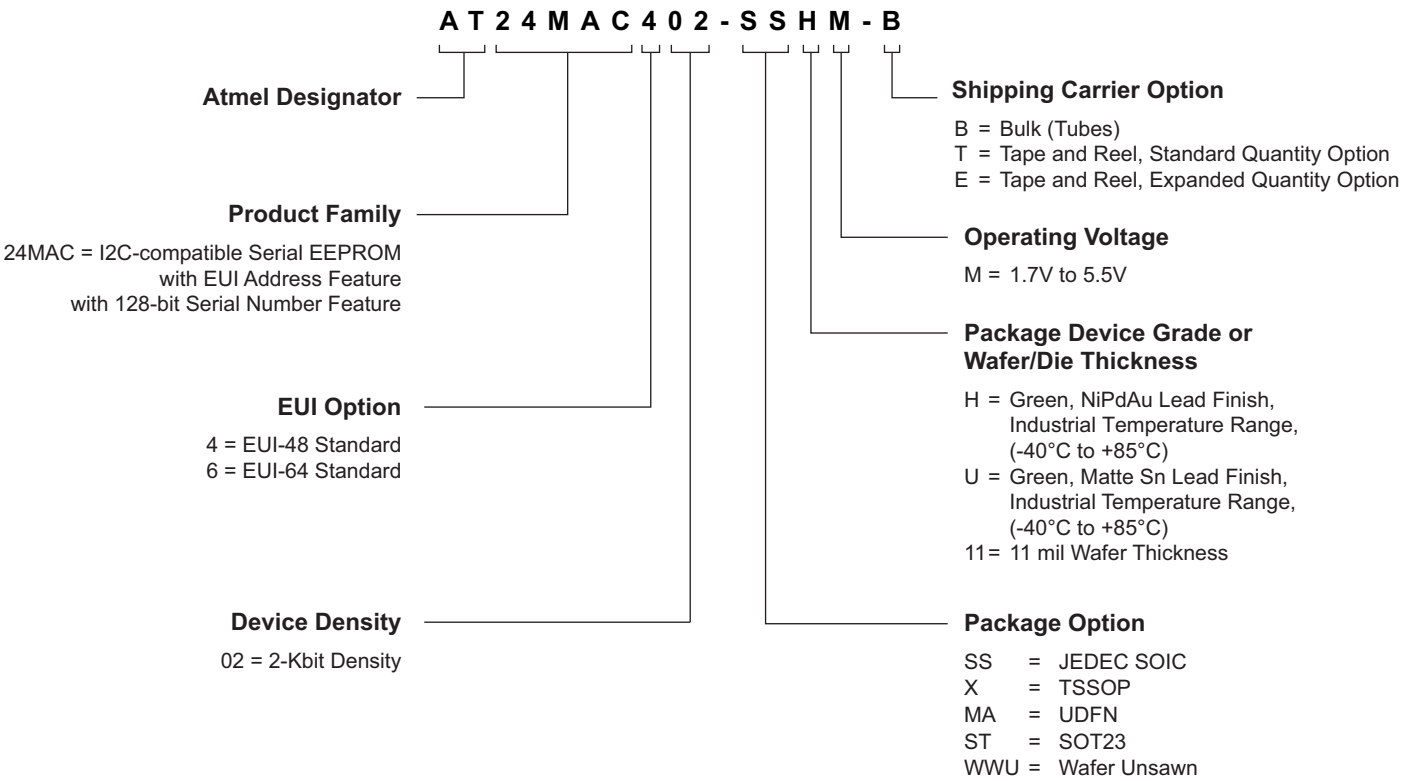
Checking the Reversible Write Protect Register (RSWP) Status: Determining the status of the Reversible Write Protect Register can be accomplished by sending a similar command to the device as was used when programming the register, except the R/W bit must be set to one. If the device returns an acknowledge, the Reversible Write Protect Register has not been programmed; otherwise, it has been programmed and the first-half of the array is write protected, but remains reversible.

Table 12-1. PSWP and RSWP Status

	Pin			Preamble							R/$\overline{W}$
Command	**A_2**	**A_1**	**A_0**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Read PSWP	A_2	A_1	A_0	0	1	1	0	A_2	A_1	A_0	1
Read RSWP	0	0	A_0	0	1	1	0	0	0	1	1

13. Ordering Information

13.1 Ordering Code Detail



13.2 AT24MAC402/602 Ordering Codes

Programming of IEEE assigned customer OUIs (non-Atmel OUIs) in conjunction with specific blocks of EUI-48 (AT24MAC402) or EUI-64 (AT24MAC602) values is available. Contact Atmel for more details.

Additional package types that are not listed may be available. Contact Atmel for more details.

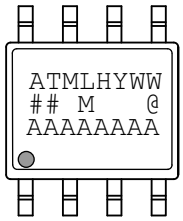
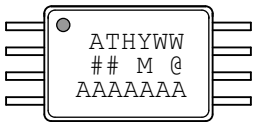
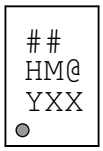
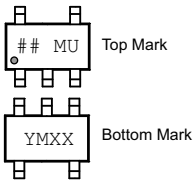
Atmel Ordering Codes	Finish	Package	Delivery Information		Operation Range
			Form	Quantity	
AT24MAC402-SSHM-B	NiPdAu (Lead-free/Halogen-free)	8S1	Bulk (Tubes)	100 per Tube	Industrial Temperature (-40°C to 85°C)
AT24MAC402-SSHM-T			Tape and Reel	4,000 per Reel	
AT24MAC402-XHM-B		8X	Bulk (Tubes)	100 per Tube	
AT24MAC402-XHM-T			Tape and Reel	5,000 per Reel	
AT24MAC402-MAHM-T		8MA2	Tape and Reel	5,000 per Reel	
AT24MAC402-MAHM-E			Tape and Reel	15,000 per Reel	
AT24MAC402-STUM-T	Matte Tin (Lead-free/Halogen-free)	5TS1	Tape and Reel	5,000 per Reel	
AT24MAC402-WWU11M(1)	N/A	Wafer Sale	Note 1		
AT24MAC602-SSHM-B	NiPdAu (Lead-free/Halogen-free)	8S1	Bulk (Tubes)	100 per Tube	Industrial Temperature (-40°C to 85°C)
AT24MAC602-SSHM-T			Tape and Reel	4,000 per Reel	
AT24MAC602-XHM-B		8X	Bulk (Tubes)	100 per Tube	
AT24MAC602-XHM-T			Tape and Reel	5,000 per Reel	
AT24MAC602-MAHM-T		8MA2	Tape and Reel	5,000 per Reel	
AT24MAC602-MAHM-E			Tape and Reel	15,000 per Reel	
AT24MAC602-STUM-T	Matte Tin (Lead-free/Halogen-free)	5TS1	Tape and Reel	5,000 per Reel	
AT24MAC602-WWU11M(1)	N/A	Wafer Sale	Note 1		

Note: 1. For wafer sales, please contact Atmel Sales.

Package Type	
8S1	8-lead, 0.150" wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
8X	8-lead, 0.170" wide, Thin Shrink Small Outline Package (TSSOP)
8MA2	8-pad, 2.00mm x 3.00mm body, 0.50mm pitch, Ultra Thin Dual No Lead (UDFN)
5TS1	5-lead, 2.90mm x 1.60mm body, Plastic Thin Shrink Small Outline (SOT23)

14. Part Markings

AT24MAC402 and AT24MAC602: Package Marking Information

8-lead SOIC	8-lead TSSOP
	
8-lead UDFN	**5-lead SOT-23**
2.0 x 3.0 mm Body 	

Note 1: ● designates pin 1

Note 2: Package drawings are not to scale

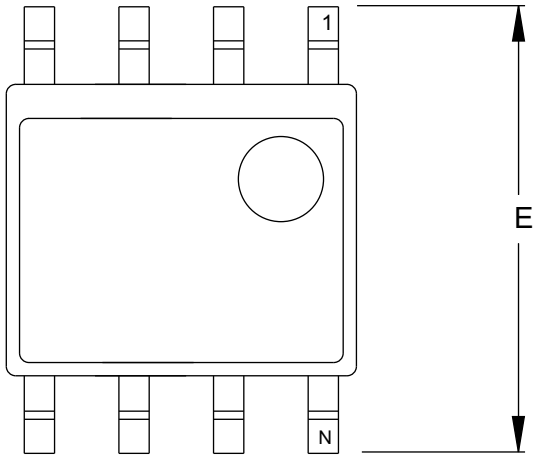
Catalog Number Truncation			
AT24MAC402		Truncation Code ##: P4	
AT24MAC602		Truncation Code ##: P6	
Date Codes			**Voltages**
Y = Year	M = Month	WW = Work Week of Assembly	M: 1.7V min
2: 2012 6: 2016	A: January	02: Week 2	
3: 2013 7: 2017	B: February	04: Week 4	
4: 2014 8: 2018	...	...	
5: 2015 9: 2019	L: December	52: Week 52	
Country of Assembly	**Lot Number**		**Grade/Lead Finish Material**
@ = Country of Assembly	AAA...A = Atmel Wafer Lot Number		H: Industrial/NiPdAu U: Industrial/Matte Tin
Trace Code			**Atmel Truncation**
XX = Trace Code (Atmel Lot Numbers Correspond to Code) Example: AA, AB.... YZ, ZZ			AT: Atmel ATM: Atmel ATML: Atmel

4/3/12

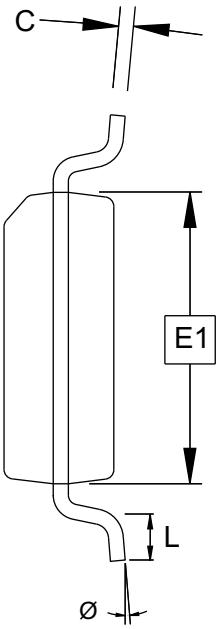
Atmel Package Mark Contact: DL-CSO-Assy_eng@atmel.com	TITLE	DRAWING NO.	REV.
	24MAC402-602SM, AT24MAC402 and AT24MAC602 Package Marking Information	24MAC402-602CSM	C

15. Packaging Information

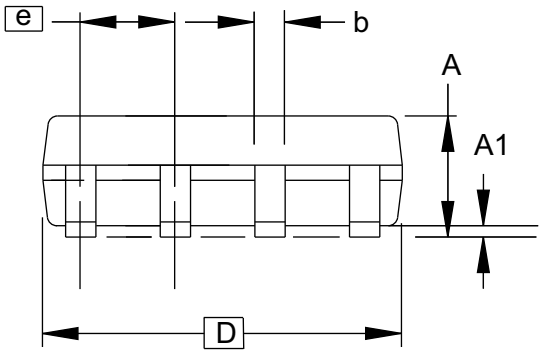
15.1 8S1 — 8-lead JEDEC SOIC



TOP VIEW



END VIEW



SIDE VIEW

Notes: This drawing is for general information only.
Refer to JEDEC Drawing MS-012, Variation AA
for proper dimensions, tolerances, datums, etc.

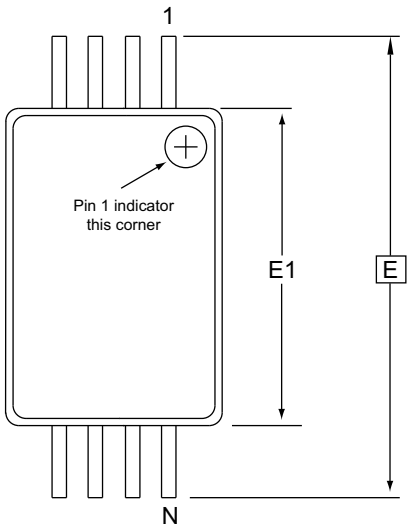
COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	1.35	–	1.75	
A1	0.10	–	0.25	
b	0.31	–	0.51	
C	0.17	–	0.25	
D	4.80	–	5.05	
E1	3.81	–	3.99	
E	5.79	–	6.20	
e	1.27 BSC			
L	0.40	–	1.27	
Ø	0°	–	8°	

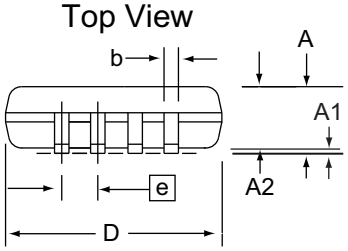
6/22/11

Atmel Package Drawing Contact: packagedrawings@atmel.com	TITLE 8S1, 8-lead (0.150” Wide Body), Plastic Gull Wing Small Outline (JEDEC SOIC)	GPC SWB	DRAWING NO. 8S1	REV. G

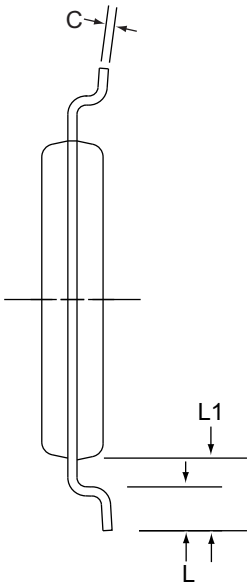
15.2 8X — 8-lead TSSOP



Top View



Side View



End View

Notes:
1. This drawing is for general information only. Refer to JEDEC Drawing MO-153, Variation AA, for proper dimensions, tolerances, datums, etc.
2. Dimension D does not include mold Flash, protrusions or gate burrs. Mold Flash, protrusions and gate burrs shall not exceed 0.15mm (0.006in) per side.
3. Dimension E1 does not include inter-lead Flash or protrusions. Inter-lead Flash and protrusions shall not exceed 0.25mm (0.010in) per side.
4. Dimension b does not include Dambar protrusion. Allowable Dambar protrusion shall be 0.08mm total in excess of the b dimension at maximum material condition. Dambar cannot be located on the lower radius of the foot. Minimum space between protrusion and adjacent lead is 0.07mm.
5. Dimension D and E1 to be determined at Datum Plane H.

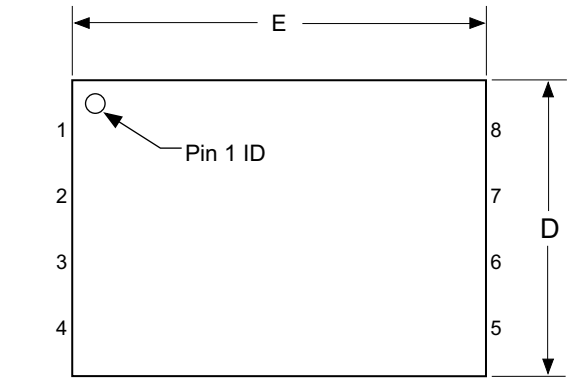
COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	-	-	1.20	
A1	0.05	-	0.15	
A2	0.80	1.00	1.05	
D	2.90	3.00	3.10	2, 5
E		6.40 BSC		
E1	4.30	4.40	4.50	3, 5
b	0.19	0.25	0.30	4
e		0.65 BSC		
L	0.45	0.60	0.75	
L1		1.00 REF		
C	0.09	-	0.20	

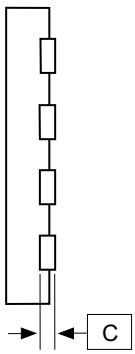
2/27/14

Atmel Package Drawing Contact: packagedrawings@atmel.com	TITLE 8X, 8-lead 4.4mm Body, Plastic Thin Shrink Small Outline Package (TSSOP)	GPC TNR	DRAWING NO. 8X	REV. E

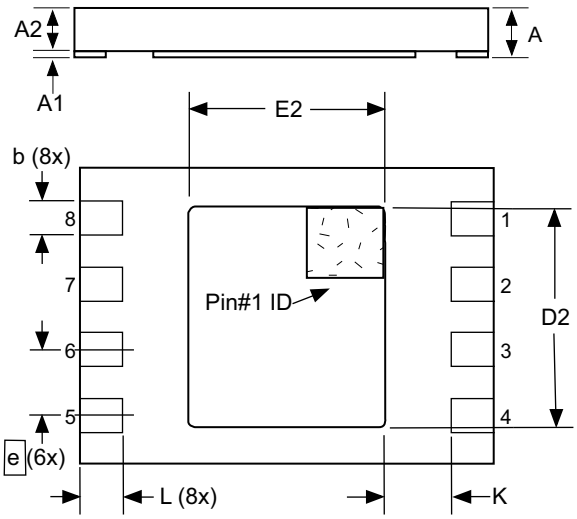
15.3 8MA2 — 8-pad UDFN



TOP VIEW



SIDE VIEW



BOTTOM VIEW

Notes:
1. This drawing is for general information only. Refer to Drawing MO-229, for proper dimensions, tolerances, datums, etc.
2. The Pin #1 ID is a laser-marked feature on Top View.
3. Dimensions b applies to metallized terminal and is measured between 0.15 mm and 0.30 mm from the terminal tip. If the terminal has the optional radius on the other end of the terminal, the dimension should not be measured in that radius area.
4. The Pin #1 ID on the Bottom View is an orientation feature on the thermal pad.

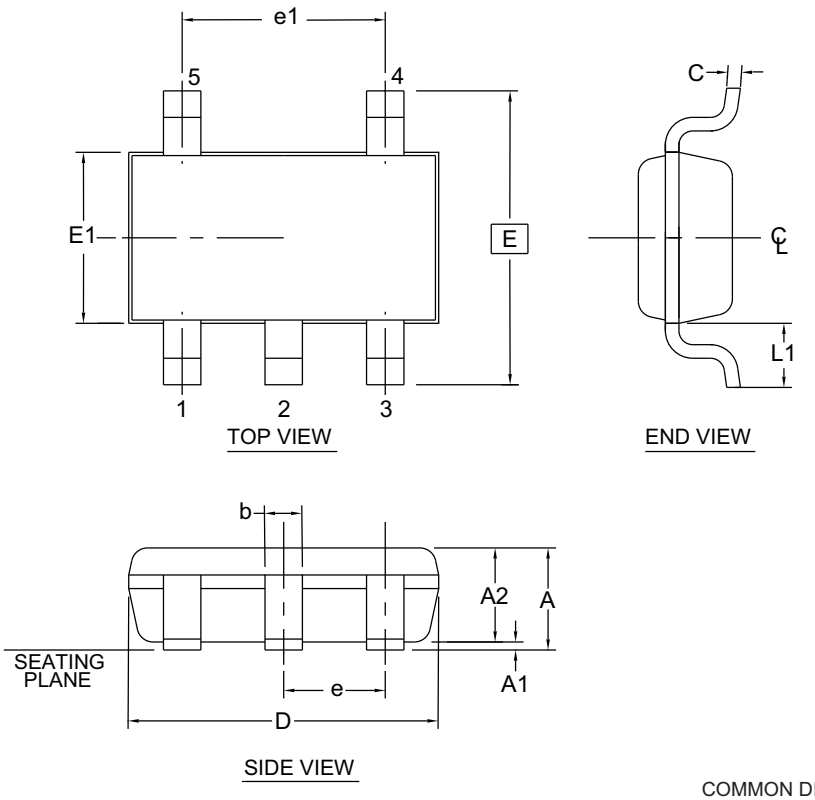
COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	0.50	0.55	0.60	
A1	0.0	0.02	0.05	
A2	-	-	0.55	
D	1.90	2.00	2.10	
D2	1.40	1.50	1.60	
E	2.90	3.00	3.10	
E2	1.20	1.30	1.40	
b	0.18	0.25	0.30	3
C	1.52 REF			
L	0.30	0.35	0.40	
e	0.50 BSC			
K	0.20	-	-	

11/26/14

Atmel Package Drawing Contact: packagedrawings@atmel.com	**TITLE** 8MA2, 8-pad 2 x 3 x 0.6mm Body, Thermally Enhanced Plastic Ultra Thin Dual Flat No-Lead Package (UDFN)	**GPC** YNZ	**DRAWING NO.** 8MA2	**REV.** G

15.4 5TS1 — 5-lead SOT23



1. Dimension D does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 mm per end. Dimension E1 does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.15 mm per side.
2. The package top may be smaller than the package bottom. Dimensions D and E1 are determined at the outermost extremes of the plastic body exclusive of mold flash, tie bar burrs, gate burrs and interlead flash, but including any mismatch between the top and bottom of the plastic body.
3. These dimensions apply to the flat section of the lead between 0.08 mm and 0.15 mm from the lead tip.
4. Dimension "b" does not include dambar protrusion. Allowable dambar protrusion shall be 0.08 mm total in excess of the "b" dimension at maximum material condition. The dambar cannot be located on the lower radius of the foot. Minimum space between protrusion and an adjacent lead shall not be less than 0.07 mm.

This drawing is for general information only. Refer to JEDEC Drawing MO-193, Variation AB for additional information.

COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	-	-	1.00	
A1	0.00	-	0.10	
A2	0.70	0.90	1.00	
c	0.08	-	0.20	3
D	2.90 BSC			1,2
E	2.80 BSC			1,2
E1	1.60 BSC			1,2
L1	0.60 REF			
e	0.95 BSC			
e1	1.90 BSC			
b	0.30	-	0.50	3,4

5/31/12

Atmel Package Drawing Contact: packagedrawings@atmel.com	TITLE 5TS1, 5-lead 1.60mm Body, Plastic Thin Shrink Small Outline Package (Shrink SOT)	GPC TSZ	DRAWING NO. 5TS1	REV. D

16. Revision History

Doc. Rev.	Date	Description
8808E	01/2015	Add the UDFN Expanded Quantity Option and the ordering information section and reorganize sections. Update the 8MA2 package outline drawing.
8808D	08/2014	Add bulk SOIC and TSSOP ordering codes. Update ordering code table, 8X and 8MA2 package drawings, and the disclaimer page. Correct pinouts from bottom to top view and reorganization figures. No changes to functional specification.
8807C	07/2013	Update status from preliminary to release. Update footers and disclaimer page.
8807B	09/2012	Update ordering information.
8807A	06/2012	Initial document release.





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