MICROCHIP

Analog and Interface Guide – Volume 1

A Compilation of Technical Articles and Design Notes

Contents

An Intuitive Approach To Mixed Signal Layout

Miscellaneous

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The Art of Laying Out Two Layer Boards

In this highly competitive, battery-powered marketplace, cost objective usually dictates that a designer uses two layer boards in the design. Although the multi-layer board (4-, 6- and 8-layers) allows the designer to build cleaner solutions in terms of size, noise and performance, financial pressures force the engineer to rethink his layout strategies with the two-layer board in mind. In this article we will discuss the use or misuse of auto routing, the concept of current return paths with and without ground planes, and recommendations for component placement where two layer boards are concerned.

Pay Now Or Pay Later With The Auto Router And Analog Circuits

It is tempting to use the auto router when designing a printed circuit board (PCB). More often than not, a purely digital board, (especially if the signals are relatively slow, and the circuit density is low) will work just fine. But as you try to lay out analog, mixed signal or high-speed circuits with the auto routing tool that is available with your layout software there may be some issues. The probability of creating serious circuit performance problems is very real.

For instance, the auto routed top layer of a two-layer board is shown in Figure 1. The bottom layer of this board is in Figure 2, and the circuit diagram for these layout layers is in Figure 3a and Figure 3b. For the layout of this mixed-signal circuit, the devices were manually placed on the board with careful thought to separating the digital and analog devices.

With this layout there are several areas of concern, but the most troubling issue is the grounding strategy. If the ground traces are followed on the top layer, every device is connected through traces on that layer. A second ground connection for every device uses the bottom layer with vias at the far right-hand side of the board. The immediate red flag that one should see when examining this layout strategy would be the existence of several ground loops. Additionally, the ground return paths on the bottom side are interrupted with horizontal signal lines. The saving grace with this grounding scheme is that the analog devices (MCP3202, 12-bit A/D converter and MCP4125, 2.5V voltage reference) are at the far right hand side of the board. This placement ensures that digital ground signals do not pass under these analog chips.

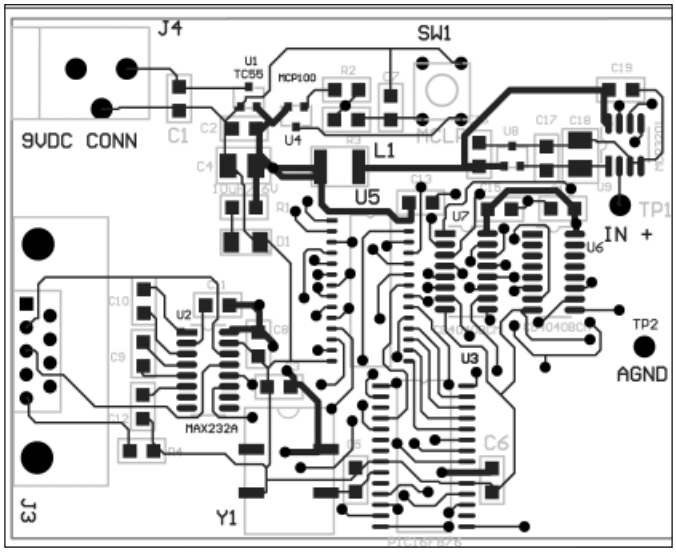


Figure 1: *Top layer of an auto-routed layout of circuit diagram shown in Figure 3.*

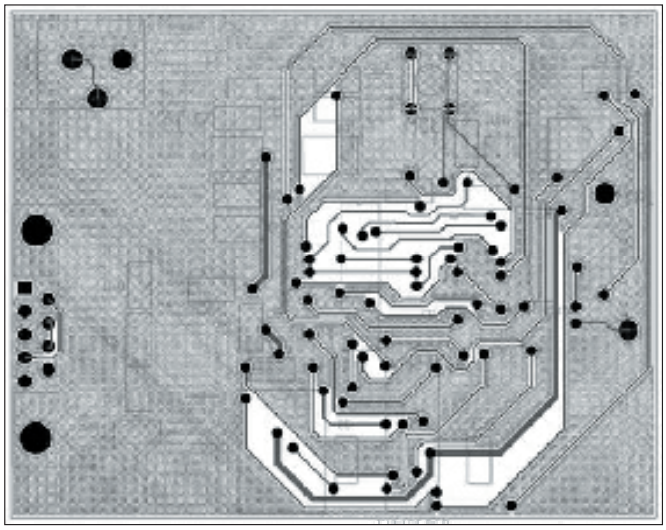


Figure 2: *Bottom layer of an auto-routed layout of circuit diagram shown in Figure 3.*

An Intuitive Approach to Mixed Signal Layout – Part 1

The manual layout of the circuit shown, in Figure 3a and Figure 3b, is given in Figure 4 and Figure 5. With this manual layout, a few general guidelines are followed to ensure positive results. These guidelines are:

1. Use the ground plane as a current return path as much as possible.
2. Separate the analog ground plane from the digital ground plane with a break.
3. If interruptions from signal traces are required on the ground-plane side, make them vertical to reduce the interference with the ground current return paths.
4. Place analog circuitry at the far end of the board and digital circuitry closest to the power connects. This reduces the effects of di/dt from digital switching.

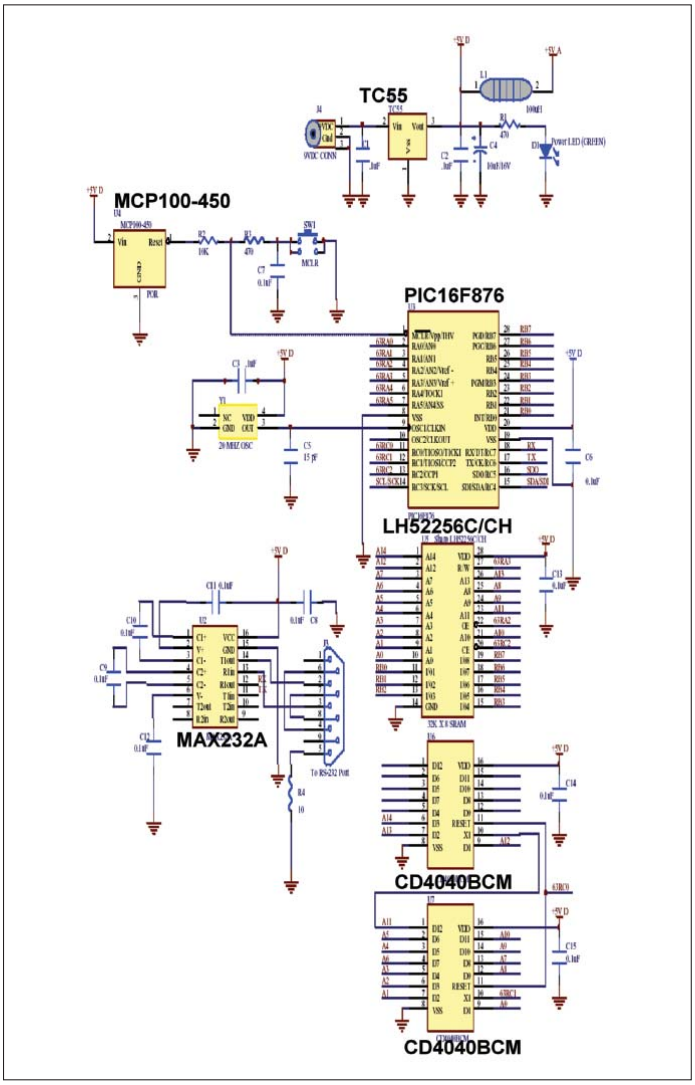


Figure 3a: *Circuit diagram for layouts in Figures 1, 2, 4 and 5. This is the circuit diagram from Microchip's MXDEV® evaluation board for the 10- and 12-bit ADCs (MCP300X and MCP320X).*

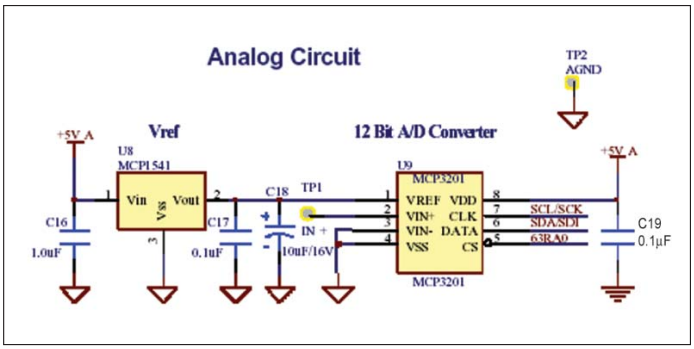


Figure 3b: *Analog section of circuit diagram for layouts in Figures 1, 2, 4 and 5. This is the circuit diagram from Microchip's MXDEV® evaluation board for the 10- and 12-bit ADCs (MCP300X and MCP320X).*

Note that with both of these two layer boards there is a ground plane on the bottom. This is only done so that an engineer working on the board can quickly see the layout when trouble shooting. This strategy is typically found with a manufacturer's demo and evaluation boards. But more typically, the ground plane is on the top of board, thereby reducing electromagnetic interference (EMI).

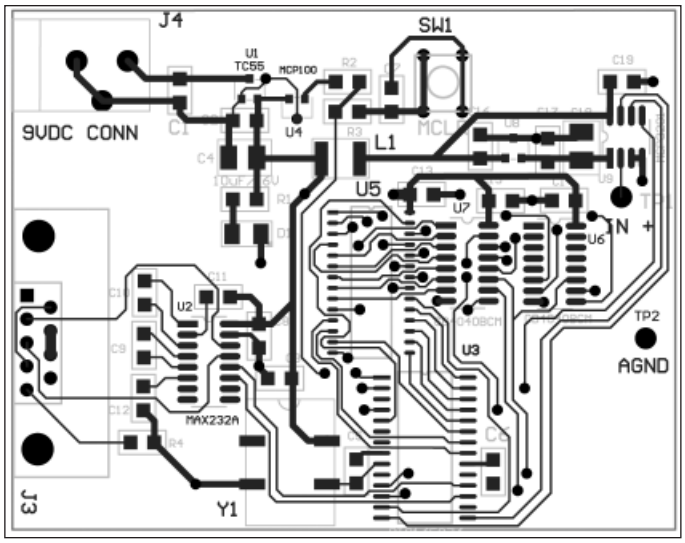


Figure 4: *Top layer of a manual routed layout of circuit diagram shown in Figure 3.*

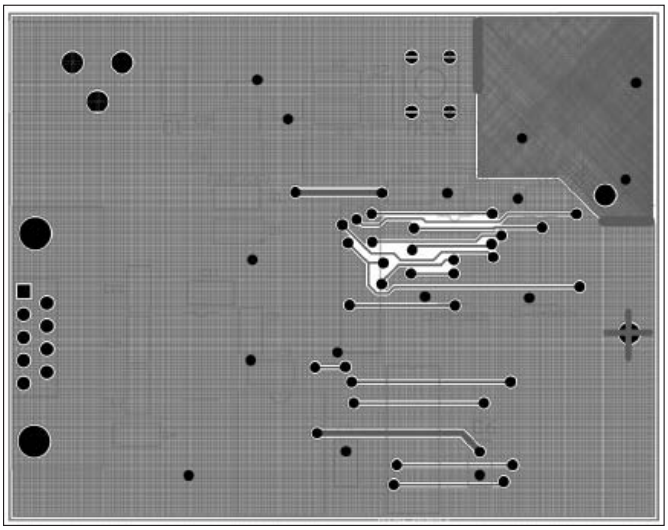


Figure 5: *Bottom layer of a manual routed layout of circuit diagram shown in Figure 3.*

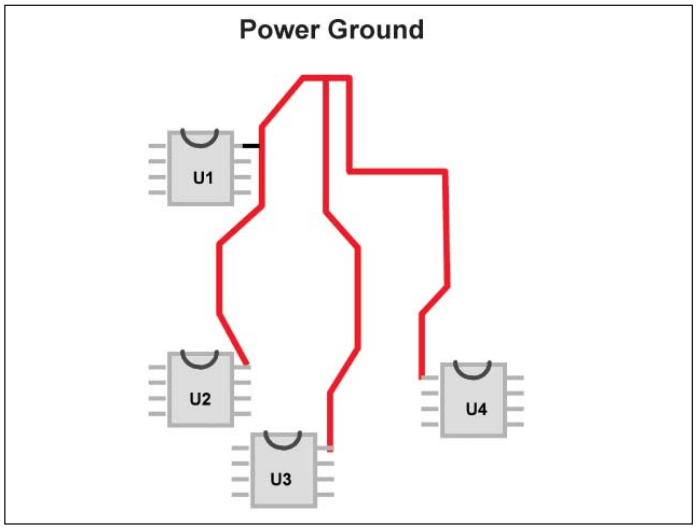


Figure 6: *If a ground plane is not feasible, current return paths can be handled with a "star" layout strategy.*

Current Return Paths With Or Without A Ground Plane

The fundamental issues that should be considered when dealing with current return paths are:

1. If traces are used, they should be as wide as possible. In the event that you are considering using traces for your ground connects on your PCB, they should be designed to be as wide as possible. This is a good rule of thumb, but also understand that the thinnest width in your ground trace will be the effective width of the trace from that point to the end, where the "end" is defined as the point furthest from the power connection.
2. Ground loops should be avoided.
3. If no ground plane is available, star connection strategies should be used.

A graphical example of a star connection strategy is shown in Figure 6.

With this type of approach, the ground currents return to the power connection independently. You will note that in Figure 6 all of the devices do not have their own return path. With U1 and U2, the return path is shared. This can be done if guidelines 4 and 5 are used.

4. Digital currents should not pass across analog devices.

   During switching, digital currents in the return path are fairly large, but only briefly. This phenomenon occurs due to the effective inductance and resistance of the ground. With the inductance portion of the ground plane or trace, the governing formula is V = Ldi/dt, where V is the resulting voltage, L is the inductance of the ground plane or trace, di is the change in current from the digital device and dt is the time span considered for the event. To calculate the effects of the resistance portion of the ground plane, changes in the voltage simply change because of V = RI, again where V is the resulting voltage, R is the ground plane or trace resistance and I is the current change caused by the digital device. These changes in the voltage of the ground plane or trace across the analog device will change the relationship between ground and the signal in the signal chain.

5. High-speed current should not pass across lower speed devices.

   Ground-return signals of high-speed circuits have a similar effect on changes to the ground plane. Again the more important formulas that determine the effects of this interference are V = Ldi/dt for the ground plane or trace inductance and V = RI for the ground plane or trace resistance. And as with digital currents, high-speed circuits that ground activity on the ground plane or that trace across the analog device change the relationship between ground and the signal in the signal chain.

6. Regardless of the technique used, the ground return paths must be designed to have a minimum resistance and inductance.
7. If a ground plane is used, breaks in plane can improve or degrade circuit performance. Use with care.

A clean way of separating analog and digital ground planes is shown in Figure 7.

In Figure 7, the precision analog is closer to the connector, however it is isolated from the activity in the digital network as well as the switching currents from the power supply circuit. This is a very effective way of keeping the ground return paths separated. This technique was also used in the layout previously discussed in Figure 4 and 5.

Conclusion

At every layout-related presentation that I give in a seminar setting, the question always asked in one form or another is, "What if management tells me I can't have two layers or a ground plane, and I still need to reduce noise in the circuit? How do I design my circuit to work around the need for a ground plane?" Typically, I instruct the person asking the question to inform their management that a ground plane is simply required if they want reliable circuit performance. The primary reason for using ground planes is lower ground impedance. They also provide a degree of EMI reduction.

But, if you are unable to win that battle because of cost constraints, this article offers some suggestions such as star networks and current return paths which if used properly will give a little relief with the circuit noise.

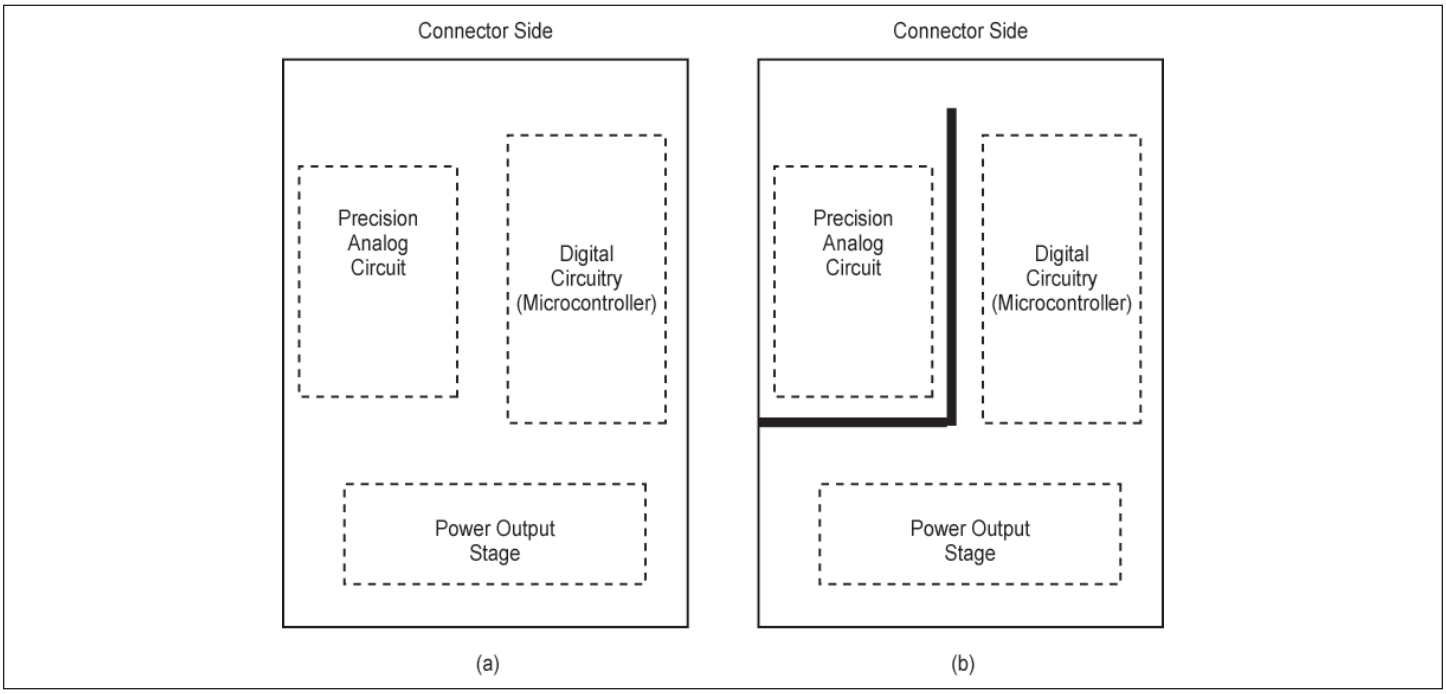


Figure 7: *Sometimes a continuous ground plane is less effective than if the ground plane was separated. In this Figure (a) shows a less desirable grounding layout strategy than is shown in (b).*

Could It Be Possible That Analog Layout Differs From Digital Layout Techniques?

The increasing percentage of digital designers and digital layout experts in the engineering population reflects the directions that our industry is headed. Although the emphasis on digital design is providing significant advances in electronics end products, there is still and will always be a portion of circuit design that interfaces with the analog or real world. There is some similarity in layout strategies between these two domains, but the differences can make an easy circuit layout design less than optimum when trying to achieve good results. In this article, we will discuss the fundamental similarities and differences between analog and digital layout with respect to bypass capacitors, power supply and ground layout, voltage errors, and electromagnetic interference (EMI) due to PCB layout.

The Similarities Of Analog And Digital Layout Practices

Bypass Or Decoupling Capacitors

In terms of layout, analog devices and digital devices all require these types of capacitors. In both cases, these devices require a capacitor as close to the power supply pin(s) with a common value for this capacitor of 0.1 micro-farads (µF). A second class of capacitor in the system is required at the power supply source. The value of this capacitor is usually about 10 µF.

The position of these capacitors is shown in Figure 1. The values of these capacitors can vary by being ten times higher or lower, but they are both required to have short leads and be as close to the devices (in the case with the 0.1 µF capacitor) or power supply source (in the case with the 10 µF capacitor) as possible.

Bypass or decoupling capacitors and their placement on the board are just common sense for both types of designs, but interesting enough, for different reasons. In the analog layout design, bypass capacitors generally serve the purpose of redirecting high frequency signals on the power supply that would otherwise enter into the sensitive analog chip through the power supply pin. Generally speaking, these high frequency signals occur at frequencies beyond the analog device's capability to reject those signals. The possible consequences of not using a bypass capacitor in your analog circuit results in the addition of undue noise to the signal path and worse yet, oscillation.

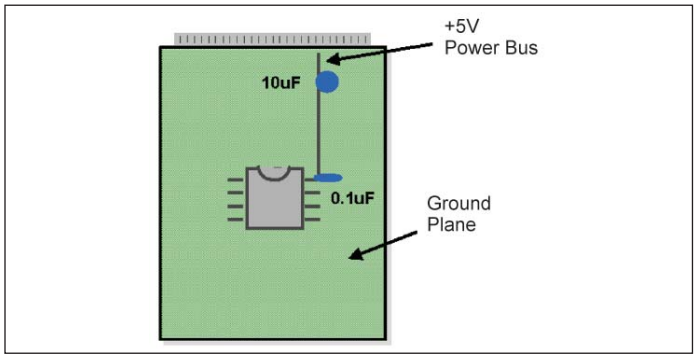


Figure 1: *In analog and digital PCB design, the bypass or decouple capacitors (1 µF) should be positioned as close to the device as possible. The power supply decoupling capacitor (10 µF) should be positioned where the power bus enters the board. In all cases, these capacitors should have short leads.*

For digital devices, such as controllers and processors, decoupling capacitors are required, but for a different reason. One of the functions of these capacitors serves as a "mini" charge reservoir. Frequently in digital circuits, a great deal of current is required to execute the transitions of the changing gate states. Because of the switching transient currents that occur on the chip and throughout the circuit board, having additional charge "on call" is advantageous. The consequence of not having enough charge locally to execute this switching action could result in a significant change in the power supply voltage. When the voltage change is too large, it will cause the digital signal level to go into the indeterminate state, more than likely resulting in erroneous operation of the state machines in the digital device. The switching current passing through the circuit board traces would cause this change in voltage. The circuit board traces have parasitic inductance, and the change in voltage results can be calculated using the formula:

$V = LdI/dt$

Where: V = voltage change
L = board trace inductance
dI = change in current through the trace
dt = the time it takes for the current to change

So for multiple reasons, it is a good idea to bypass (or decouple) the power supply at the power supply and at the power supply pin of active devices.

The Power And Ground Should Be Routed Together

When power and ground traces are well matched with respect to location, the opportunities for EMI is lessened. If power and ground are not matched, system loops are designed into the layout and the possibility of seeing "noisy" results without explanation is possible. An example of a PCB designed with the power and ground traces not matched is shown in Figure 2.

The loop area that is designed into this board is 697cm^2. The opportunity for induced voltages in the loop because of radiated noise off the board and in the board is decreased dramatically using the approach shown in Figure 3.

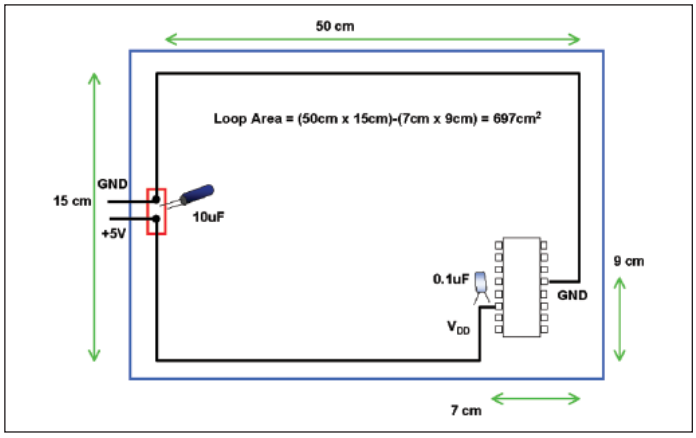


Figure 2: *The power and ground traces are laid out using different routes to the device on this board. This mismatch opens the opportunity for EMI into the electronics of this board.*

An Intuitive Approach to Mixed Signal Layout – Part 2

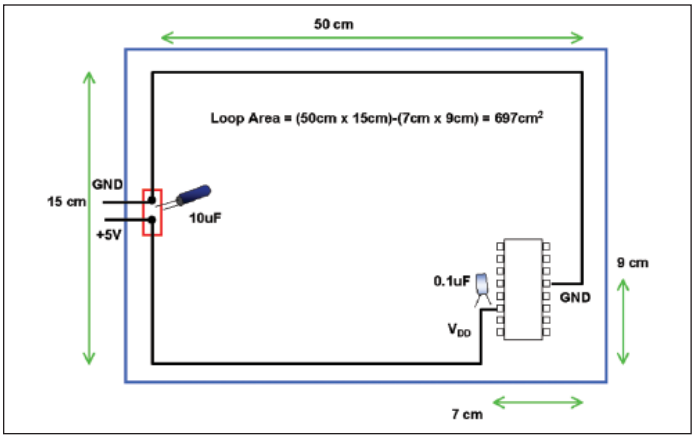


Figure 3: *In this one layer board, the power trace and ground trace are laid next to each other on their way to the device on this board. This board is better matched than that shown in Figure 2. The opportunity for EMI into the electronics of this board is lessened by 679/12.8 or ~54x.*

Where The Domains Differ

Ground Planes Can Be A Problem

The fundamentals of circuit board layout apply to analog circuits as well as digital circuits. One fundamental rule of thumb is to use uninterrupted ground planes. This common practice reduces the effects of dI/dt (change in current with time) in digital circuits, which changes the potential of ground and noise being injected into the analog circuits. But when comparing digital and analog circuits, the layout techniques are essentially the same with one exception. The added precaution that should be taken with analog circuits is to keep the digital signal lines and return paths in the ground plane as far away from the analog circuitry as possible. This can be done by connecting the analog ground plane separately to the system ground connect or having the analog circuitry at the farthest side of the board, i.e., at the end of the line. This is done in order to maintain signal paths that have a minimal amount of interference from external sources. The opposite is not true for digital circuitry. The digital circuitry can tolerate a great deal of noise on the ground plane before problems start to appear.

Location of Components

In every PCB design, the noisy and quiet portions of the circuit should be separated as mentioned above. Generally speaking, the digital circuitry is "rich" with noise and in turn less sensitive to this type of noise (because of the larger voltage noise margins). In contrast the voltage noise margins of the analog circuitry are much smaller. Of the two domains, the analog domain is most sensitive to switching noise. In the layout of a mixed signal system, the two domains should be separated. This is graphically shown in Figure 4.

Parasitics Designed Into The PCB

There are two fundamental parasitic components that can easily be designed into the PCB that might create problems; a capacitor and an inductor. A capacitor is designed into a board simply by placing two traces close to each other. This can be done by placing the two traces, one on top of the other with two layers or by placing them beside each other on the same layer, as shown in Figure 5. In both trace configurations, changes in voltage with time (dV/dt) on one trace could generate a current on a second trace. If the second trace is high impedance, the current that is created by the e-field of this event will convert into a voltage.

Fast voltage transients are most typically found on the digital side of the mixed signal design. If the traces that have these fast voltage transients are in close proximity of high impedance analog traces, this type of error will be very disruptive with analog circuitry accuracy. Analog circuitry has two strikes against it in this environment. The noise margins are much lower than digital and it is not unusual to have high impedance traces.

This type of phenomena can be easily minimized using one of two techniques. The most commonly used technique is to change the dimensions between the traces as the capacitor equation suggests. The most effect dimension to change is the distance between the two offending traces. It should be noted that the variable, "d", is in the denominator of the capacitor equation. As "d" is increased, the capacitance will decrease. Another variable that can be changed is the length of the two traces. In this case, if the length ("L") is reduced the capacitance between the two traces will also be reduced.

Another technique used is the lay a ground trace between the two offending traces. Not only is the ground trace low impedance, but an additional trace like this will break up the e-fields that are causing the disturbance shown in Figure 5.

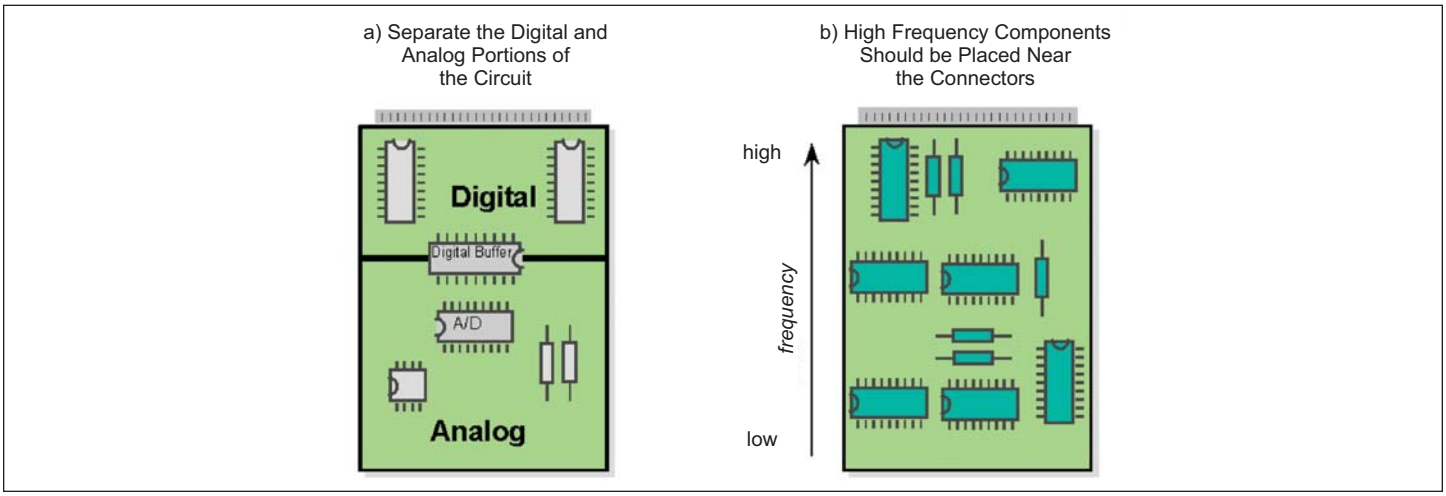


Figure 4: *If possible, (a) the digital and analog portion of circuits should be separated in order to separate the digital switching activity from the analog circuitry. Additionally, (b) the high frequency should be separated from the low frequency where possible, keeping the higher frequency components closer to the board connector.*

An Intuitive Approach to Mixed Signal Layout – Part 2

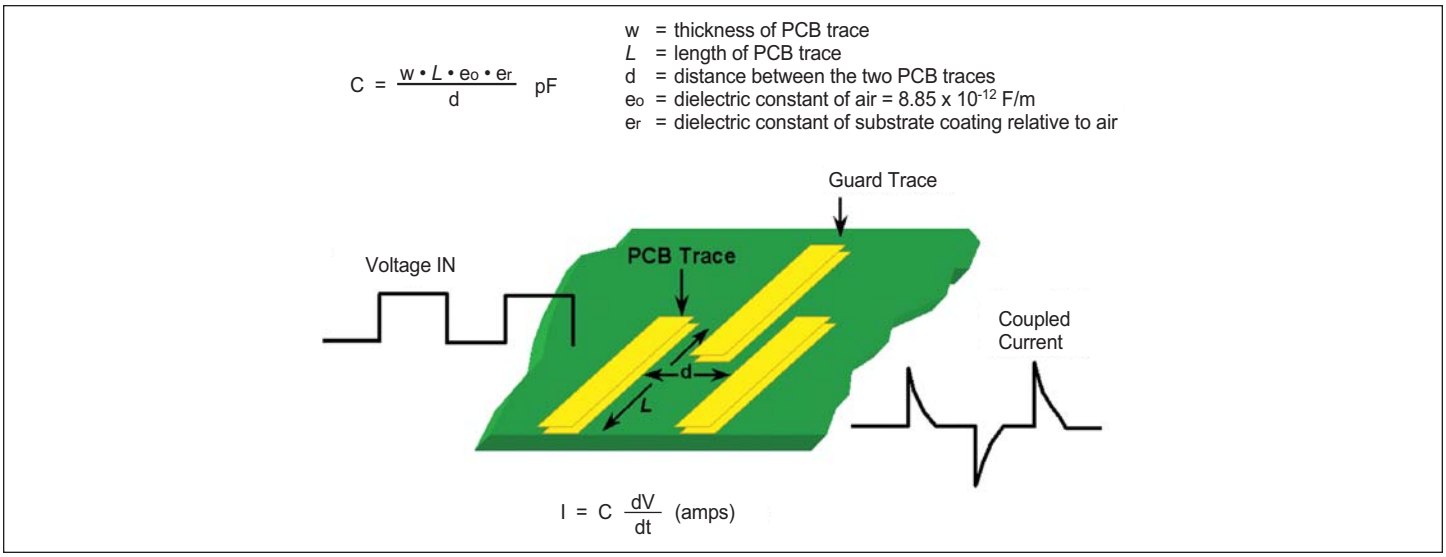


Figure 5: *Capacitors can easily be fabricated into a PCB by laying out two traces in close proximity. With this type of capacitor, fast voltage changes on one trace can initiate a current signal in the other trace.*

The way that an inductor is designed into a board is similar to the construction of a capacitor. Again this is done by placing two traces, one on top of the other with two layers or by placing them beside each other on the same layer, as shown in Figure 6. In both trace configurations, changes in current with time (dI/dt) on one trace could generate a voltage in the same trace due to the inductance on that trace and initiate a proportional current on the second trace due to the mutual inductance. If the voltage change is high enough on the primary trace, the disturbance can reduce the voltage margin of the digital circuitry enough to cause errors. This phenomena is not necessary reserved for digital circuits, but more common in that environment because of the larger, seemingly instantaneous switching currents.

To eliminate potential noise for EMI sources it is best to separate quiet analog lines versus noisy I/O ports. Try to implement low impedance power and ground networks, minimize inductance in conductors for digital circuits and minimize capacitive coupling in analog circuits.

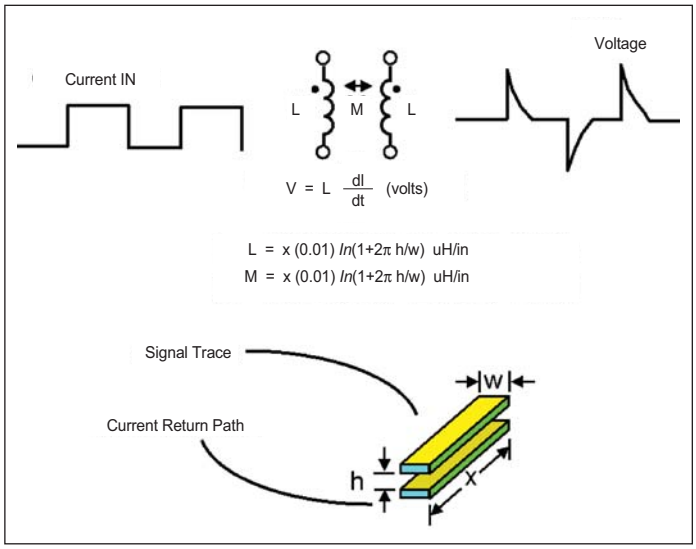


Figure 6: *If little attention is paid to the placement of traces, line inductance and mutual inductance can be created with the traces in a PCB. This kind of parasitic element is most detrimental to the circuit operation where digital switching circuits reside.*

Conclusion

When the domains meet, careful layout is critical if a designer intends to have a successful final PCB implementation. Layout strategies usually are presented as rules of thumb because it is difficult to test the success of your final product in a lab environment. So, generally speaking, although there are some similarity in layout strategies between the digital and analog domain, the differences should be recognized and worked with. In this article we briefly talked about bypass capacitors, power supply and ground layout, voltage errors and EMI because of PCB layout.

For more information refer to:

[1] Henry W. Ott, Noise Reduction Techniques in Electronic Systems, 2nd ed., Wiley, 1998

[2] Ralph Morrison, Noise and Other Interfering Signals, Wiley and Sons, 1992

Where The Board And Component Parasitics Can Do the Most Damage

The major classes of parasitics generated by the PC board layout come in the form of resistors, capacitors and inductors. For instance, PCB resistors are formed as a result of traces from component to component. Unintentional capacitors can be built into the board with traces, soldering pads and parallel traces. Circumstances that surround where inductors are built come in the form of loop inductance, mutual inductance and vias. All of these parasitics stand a chance of interfering with the effectiveness of your circuit as you transition from the circuit diagram to the actual PCB. This article quantifies the most troublesome class of board parasitics, the board capacitor, and gives an example of where the effects on circuit performance can be clearly seen.

Feeling the Pain of Those Unnecessary Capacitors

In Part 2 of this series we discussed how capacitors could inadvertently be built into your board. To quickly review this concept, most layout capacitors are built by placing two parallel traces close together. The value of this type of capacitor can be calculated using the formulas shown in Figure 1 (note that this figure is the same as Figure 5 in Part 2 of this series).

This type of capacitor can cause problems in mixed signal circuits where sensitive, high impedance analog traces are in close proximity to digital traces. For example, the circuit in Figure 2 has the potential to have this type of problem.

To quickly explain the circuit operation in Figure 2, a 16-bit DAC is built using three 8-bit digital potentiometers and three CMOS operational amplifiers. To the left side of this figure, two digital potentiometers (U3a and U3b) span across V_{DD} to ground with the wiper output connected to the non-inverting input of two amplifiers (U4a and U4b). The digital potentiometers, U2 and U3 are programmed using an SPI™ interface between the microcontroller, U1. In this configuration, each digital potentiometer is configured to operate as an 8-bit multiplying DAC. If V_{DD} is equal to 5V, the LSB size of these DACs is equal to 19.61 mV.

The wipers of each of these two digital potentiometers are connected to the non-inverting inputs of two buffer configured operational amplifiers. In this configuration, the inputs to the amplifiers are high impedance, which isolates the digital potentiometers from the rest of the circuit. These two amplifiers are also configured so that the output swing restrictions on the amplifiers in the second stage are not violated.

To have this circuit perform as a 16-bit DAC (U2a), a third digital potentiometer spans across the output of these two amplifiers, U4a and U4b. The programmed setting of U3a and U3b sets the voltage across the digital potentiometer. Again, if V_{DD} is 5V it is possible to program the output of U3a and U3b 19.61 mV apart. With this size of voltage across the third 8-bit digital potentiometer, R3, the LSB size of this circuit from left to right is 76.3 mV. The critical device specifications that will give optimum performance with this circuit are given in Table 1.

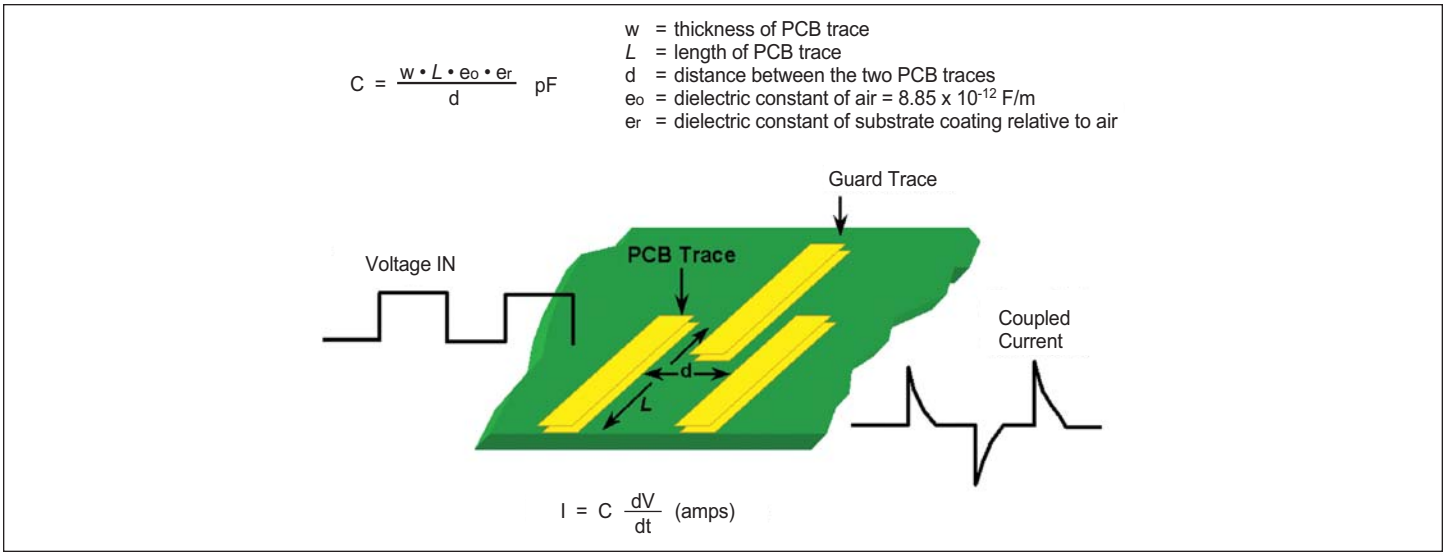


Figure 1: *Capacitors can easily be fabricated into a PCB by laying out two traces in close proximity. With this type of capacitor, fast voltage changes on one trace can initiate a current signal in the other trace. (Also found in Part 2, Could It Be Possible That Analog Layout Differs From Digital Layout Techniques, Figure 5.)*

An Intuitive Approach to Mixed Signal Layout – Part 3

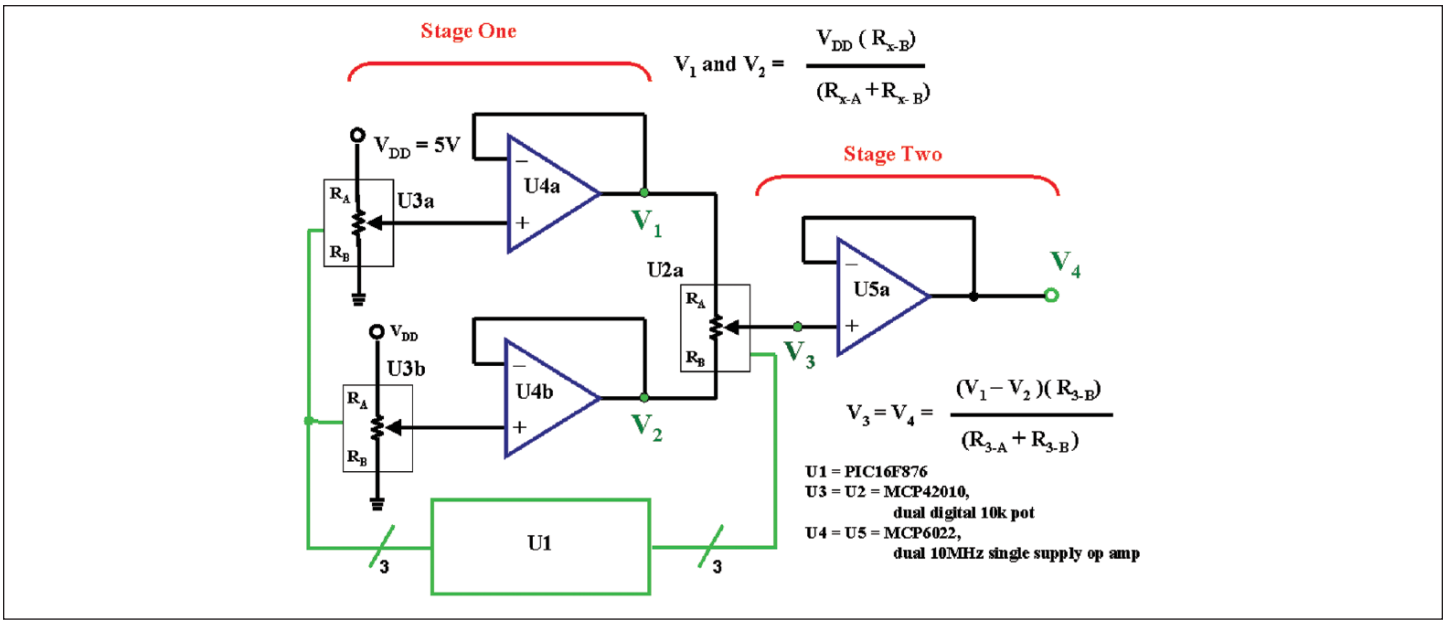


Figure 2: A 16-bit DAC can be built using three 8-bit digital potentiometers and three amplifiers to provide 65,536 different output voltages. If V_{DD} is 5V in this system the resolution or LSB size of this DAC is 76.3 mV.

This circuit can be used in two basic modes of operation. The first mode would be if you wanted a programmable, adjustable, DC reference. In this mode the digital portion of the circuit is only used occasionally and certainly not during normal operation. The second mode would be if you used the circuit as an arbitrary wave generator. In this mode, the digital portion of the circuit is an intimate part of the circuit operation. In this mode, the risk of capacitive coupling may occur.

The first pass layout of the circuit in Figure 2 is shown in Figure 3. This circuit was quickly designed in our lab without attention to detail. The consequences of placing digital traces next to high impedance analog lines were overlooked in the layout review. This speaks strongly to doing it right the first time, but to our benefit this article will illustrate how to identify the problem and make significant improvements.

Device	Specification		Purpose
Digital Potentiometers (MCP42010)	Number of bits	8-bits	Determines the overall LSB size and resolution of the circuit.
	Nominal resistance (resistive element)	10 kΩ (typ)	The lower this resistance is the lower the noise contribution will be to the overall circuit. The trade off is that the current consumption of the circuit is high with these lower resistances.
	DNL	± 1 LSB (max)	Good Differential Non-Linearity is needed to insure no missing codes occur in this circuit which allows for a possible 16-bit operation.
	Voltage Noise Density (for half of the resistive element)	9 nV / √Hz @ 1 kHz (typ)	If the noise contribution of these devices is too high it will take away from the ability to get 16-bit noise free performance. Selecting lower resistive elements can reduce the digital potentiometer noise.
Operational Amplifiers (MCP6022)	Input Bias Current, IB	1 pA @ 25°C (max)	Higher IB will cause a DC error across the potentiometer. CMOS amplifiers were chosen for this circuit for that reason.
	Input Offset Voltage	500 mV (max)	A difference in amplifier offset error between A1 and A2 could compromise the DNL of the overall system.
	Voltage Noise Density	8.7 nV / √Hz @10 kHz (typ)	If the noise contribution of these devices is too high it will take away from the ability to get 16-bit accurate performance. Selecting lower noise amplifiers can reduce amplifier noise.

Table 1: From the long list of specifications that each of the devices has, there are a handful of key specifications that make this circuit more successful when it is used to provide DC reference voltages or arbitrary wave forms.

An Intuitive Approach to Mixed Signal Layout – Part 3

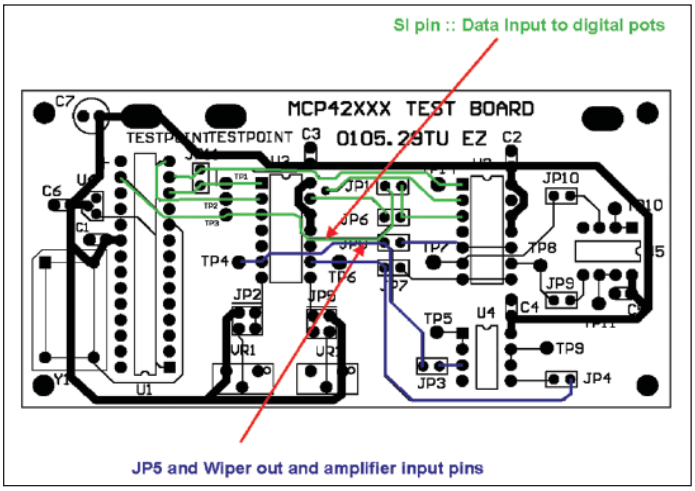


Figure 3: *This is the first attempt at the layout for the circuit in Figure 2. In this figure it can quickly be seen that a critical high impedance analog line is very close to a digital trace. This configuration produces inconsistent noise on the analog line because the data input code on that particular digital trace changes, dependent on the programming requirements for the digital potentiometer.*

Taking a look at the color-coding in this layout it is obvious where a potential problem is. The analog trace (blue) that is pointed out goes from the wiper of U3a to the high impedance amplifier input of U4a. The digital trace (green) that is pointed out carries the digital word that programs the digital potentiometer settings.

On the bench, it is found that the digital signal on the green trace is coupled into the sensitive blue trace. This is illustrated in the scope photo below (Figure 4).

The digital signal that is programming the digital potentiometers in the system has transmitted from trace to trace onto an analog line that is being held at a DC voltage. This noise propagates through the analog portion of the circuit all the way out to the third digital potentiometer (U5a). The third digital potentiometer is toggling between two output states.

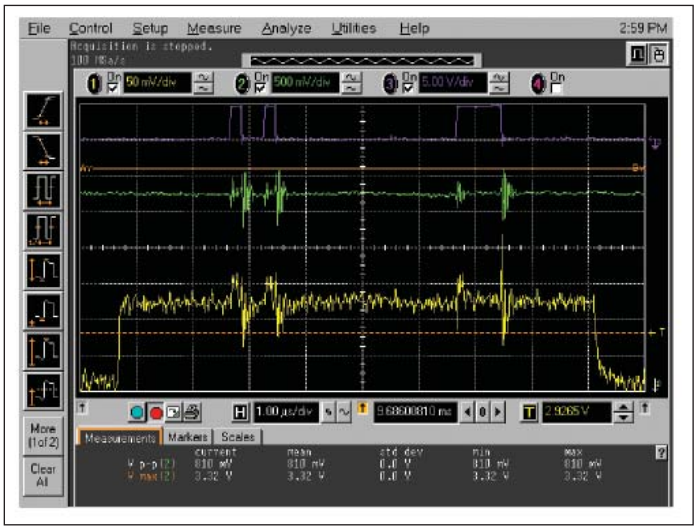


Figure 4: *In this scope photo, the top trace was taken at JP1 (digital word to the digital potentiometers), the second trace on JP5 (noise on the adjacent analog trace) and the bottom yellow trace is taken at -TP10 (noise at the output of the 16-bit DAC).*

What is the solution to this problem? Basically we separated the traces. Figure 5 shows an improved layout solution.

The results of the layout change are shown in Figure 6. With the analog and digital traces carefully kept apart, this circuit becomes a very clean 16-bit DAC. A single code transition of the third digital potentiometer 76.29 mV is shown with the green trace. You may notice that the oscilloscope scale is 80 mV/div and that the amplitude of this code change is shown to be approximately 80 mV. In the lab, we were forced by the equipment to gain the output of the 16-bit DAC by 1000x.

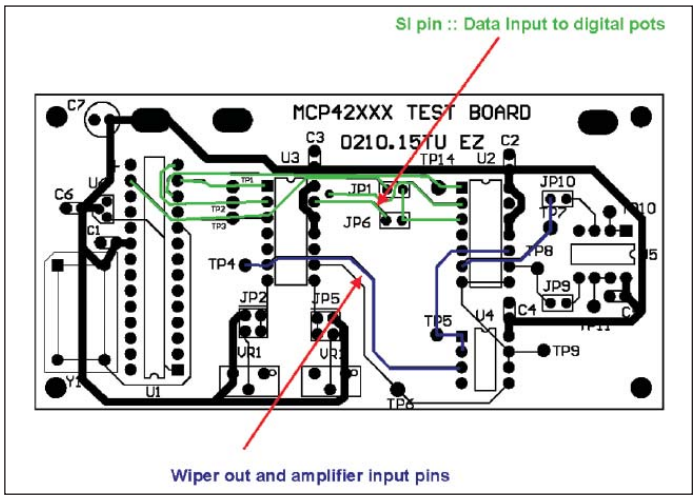


Figure 5: *With this new layout the analog lines have been separated from the digital lines. This distance has essentially eliminated the digital noise that was causing interference in the previous layout.*

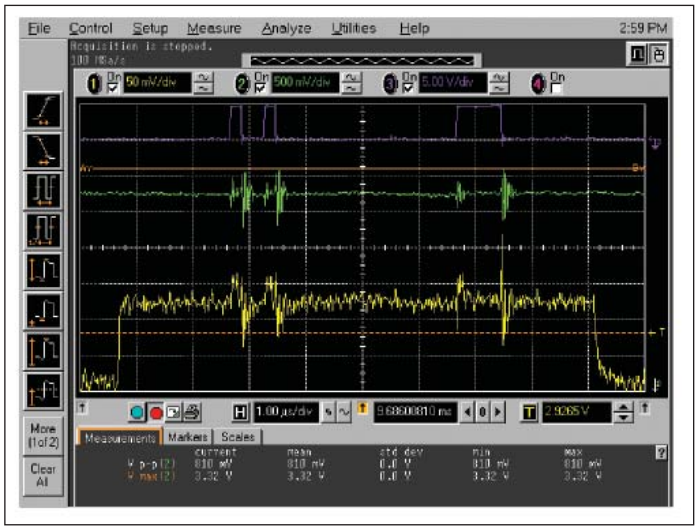


Figure 6: *The 16-bit DAC in this new layout is showing a single code transition with no digital noise from the communication to the digital potentiometers.*

Conclusion

Once again, when the digital and analog domains meet, careful layout is critical if you intend to have a successful final PCB implementation. In particular, active digital traces close to high impedance analog traces will cause serious coupling noise that can only be avoided with distance between traces.

Layout Techniques To Use As The ADC Accuracy and Resolution Increase

Initially, analog-to-digital (A/D) converters rose from an analog paradigm where a large percentage of the physical silicon was analog. As the progression of new design topologies evolves, this paradigm shifted to where slower speed A/D converters were predominately digital. Even with this on-chip shift from analog to digital, the PCB layout practices have not changed. Now as always, when the layout designer is working with mixed signal circuits, key layout knowledge is still needed in order to implement an effective layout. This article will look at the PCB layout strategies required for A/D converters using successive approximation register (SAR) and Sigma-Delta topologies.

SAR Converter Layout

SAR A/D converters can be found with 8-bit, 10-bit, 12-bit, 16-bit and sometimes 18-bit resolution. Originally, the process and architecture for these converters was bipolar with R-2R ladders. But recently these devices have migrated to a CMOS process with a capacitive charge distribution topology. Needless to say, the system layout strategy for these converters has not changed with this migration. The basic approach to layout is consistent except for higher resolution devices. These devices require more attention to the prevention digital feedback from the serial or parallel output interface of the converter.

The SAR converter is predominately analog in terms of circuitry and the amount of real estate dedicated to the different domains on the chip. In Figure 1, a block diagram of a 12-bit CMOS SAR converter is shown.

Within this block diagram the Sample/Hold, comparator, most of the digital-to-convert (DAC) and 12-bit SAR are analog. The remaining portions of the circuit are digital. As a consequence, most of the power and current needed for this converter is used for the internal analog circuitry. There is very little digital currents coming from the device with the exception of the small amount of switching that occurs in the DAC and at the digital interface.

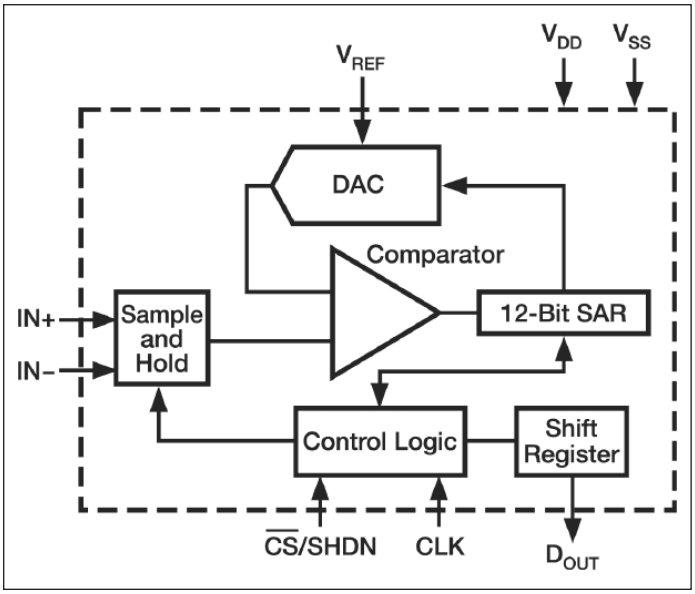


Figure 1: *A block diagram of a 12-bit CMOS SAR A/D converter. This converter uses a charge distribution across a capacitive array.*

These types of converters can have several pins for the ground and power connections. The pin names are often misleading in that the analog and digital connections can be differentiated with the pin label. These labels are not meant to describe the system connections to the PCB, but rather they identify how the digital and analog currents come off the chip. Knowing this information and understanding that the primary real estate consumed on the chip is analog, it makes sense to connect the power and ground pins on the same planes, e.g., analog planes.

For instance, the pinout for a representative sample of 10-bit and 12-bit converters are shown in Figure 2.

With these devices, the ground is usually directed off the chip with two pins: AGND and DGND. The power is taken for a single pin. When implementing the PCB layout using these chips, the AGND and DGND should be connected to the analog ground plane. The analog and digital power pins should also be connected to the analog power plane or at least connected to the analog power train with proper by-pass capacitors as close to each pin as possible. The only reason that these devices would have only one ground pin and one positive supply pin, as with the MCP3201, is due to package pin limitations. However, separate grounds enhance the probability of getting good and repeatable accuracy from the converter.

With all of the converters, the power supply strategy should be to connect all grounds, positive supply and negative supply pins to the analog plane. In addition, the 'COM' pin or 'IN' pin associated with the input signal should be connected as close to the signal ground as possible.

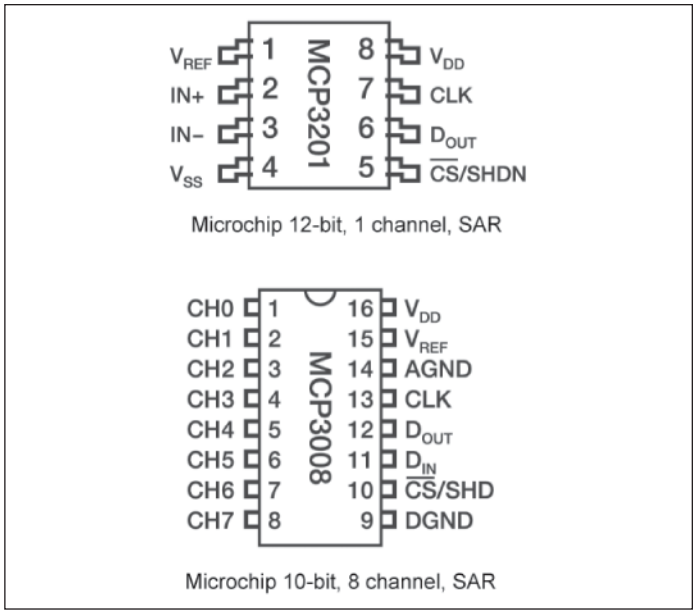


Figure 2: *The SAR converter, regardless of resolution, usually has at least two ground connects: AGND and DGND. The converters illustrated here are the MCP3201 and MCP3008 from Microchip.*

An Intuitive Approach to Mixed Signal Layout – Part 4

Higher resolution SAR converters (16- and 18-bit converters) require a little more consideration in terms of separating the digital noise from the quiet analog converter and power planes. When these devices are interfaced to a microcontroller, external digital buffers should be used in order to achieve clean operation. Although these types of SAR converters typically have internal double buffers at the digital output, external buffers are used to further isolate the digital bus noise from the analog circuitry in the converter. An appropriate power strategy for this type of system is shown in Figure 3.

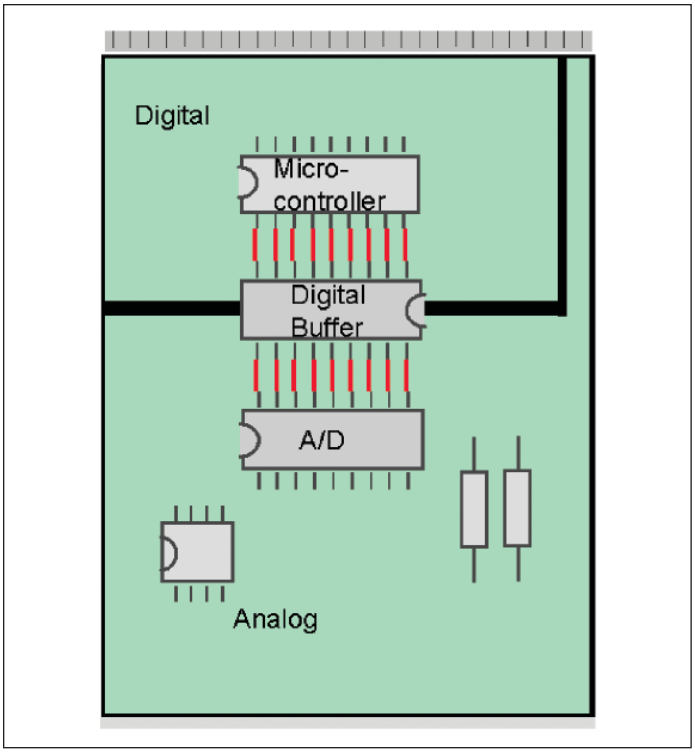


Figure 3: *With high-resolution SAR A/D converters, the converter power and ground should be connected to the analog planes. The digital output of the A/D converter should then be buffered, using external 3-state output buffers. These buffers provide isolation between the analog and digital side, in addition to high-drive capability.*

Precision Sigma-Delta Layout Strategies

The silicon area of the precision Sigma-Delta A/D converter is predominately digital. In the early days, when this type of converter was being produced, this shift in the paradigm prompted users to separate the digital noise from the analog noise by using the PCB planes. As with the SAR A/D Converter, these types of A/D converters can have multiple analog- and digital ground and power pins. Once again, the common tendency of a digital or analog design engineer is to try separating these pins into separate planes.

Unfortunately, this tendency is misguided, particularly if you intend to solve critical noise problems with the 16-bit to 24-bit accuracy devices.

With high-resolution Sigma-Delta converters that have a 10 Hz data rate, the clock (internal or external) to the converter could be as high as 10 MHz or 20 MHz. This high frequency clock is used for switching the modulator and running the oversampling engine. With these circuits, the AGND and DGND pins are connected together on the same ground plane, as is the case with the SAR converter. Additionally, the analog and digital power pins are connected together, preferably on the same plane. The requirements on the analog and digital power planes are the same as with the high-resolution SAR converters.

A ground plane is mandatory, which implies that a double-sided board is needed at minimum. On this double-sided board, the ground plane should cover at least 75% of the area if not more. The purpose of this ground plane layer is to reduce grounding resistance and inductance as well as provide a shield against electro-magnetic interference (EMI) and radio-frequency interference (RFI). If circuit interconnect traces need to be put on the ground-plane side of the board, they should be as short as possible and perpendicular to the ground current return paths.

Conclusion

You can get away without separating the analog and digital pins of low precision A/D converters, such as 6-, 8- or maybe even 10-bit converters. But as the resolution/accuracy increases with your converter selection, the layout requirements also become more stringent. In both cases, with high resolution SAR A/D converters and Sigma-Delta converters these devices need to be connected directly to the lower noise analog ground and power planes.

An Intuitive Approach to Mixed Signal Layout – Part 5

The Trouble With Troubleshooting Your Layout Without The Right Tools

When you're trying to solve a signal integrity problem, the best of all worlds is to have more than one tool to examine the behavior of a system. If there is an A/D converter in the signal path, there are three fundamental issues that can easily be examined when assessing the circuit's performance. All three of these methods evaluate the conversion process as well as its interaction with the layout and other portions of the circuit. The three areas of concern encompass the use of frequency analysis (FFTs), time analysis, and DC analysis techniques. This article will explore the use of these tools to identify the source of problems as it relates to the layout implementation of circuits. We will explore how you decide what to look for, where to look, how to verify problems through testing and how to solve the problems that are identified. The circuit that was built and is used in the following discussion is shown in Figure 1.

Power Supply Noise

A common source of interference in circuit applications is from the power supply. This interference signal is typically injected through the power supply pins of the active devices. For instance, a time based plot of the output of the A/D converter in Figure 1 is given in Figure 2. In this figure, the sample speed for the A/D converter was 40 ksps and 4096 samples were taken.

In this case, the instrumentation amplifier, voltage reference and A/D converter do not have by-pass capacitors installed. Additionally, the inputs to the circuit are both referenced to a low noise, DC voltage source of 2.5V.

Further investigations into the circuit shows that the source of the noise seen on the time plot comes from the switching power supply. An inductive choke is added to the circuit along with bypass capacitors. One 10 µF is positioned at the power supply and three 0.1 µF capacitors are placed as close to the supply pins of the active elements as possible. Now the generation of a new time plot seems to produce a solid DC output and this is verified with the Histogram results, shown in Figure 3. The data shows these changes eliminated the noise source from the signal path of the circuit.

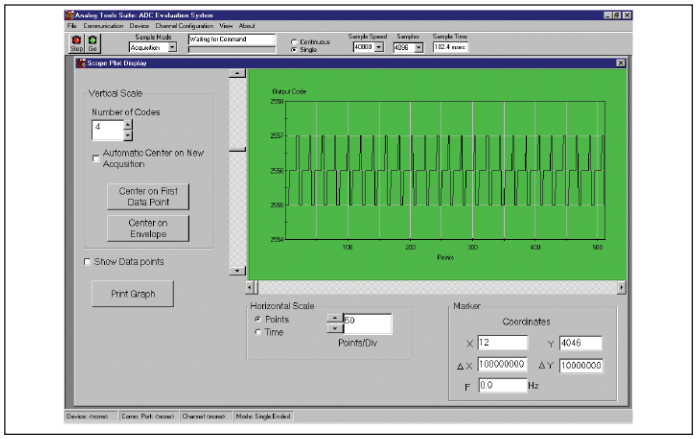


Figure 2: *The time domain representation of this data from the 3201, 12-bit A/D converter produces an interesting periodic signal. This signal source was traced back to the power supply.*

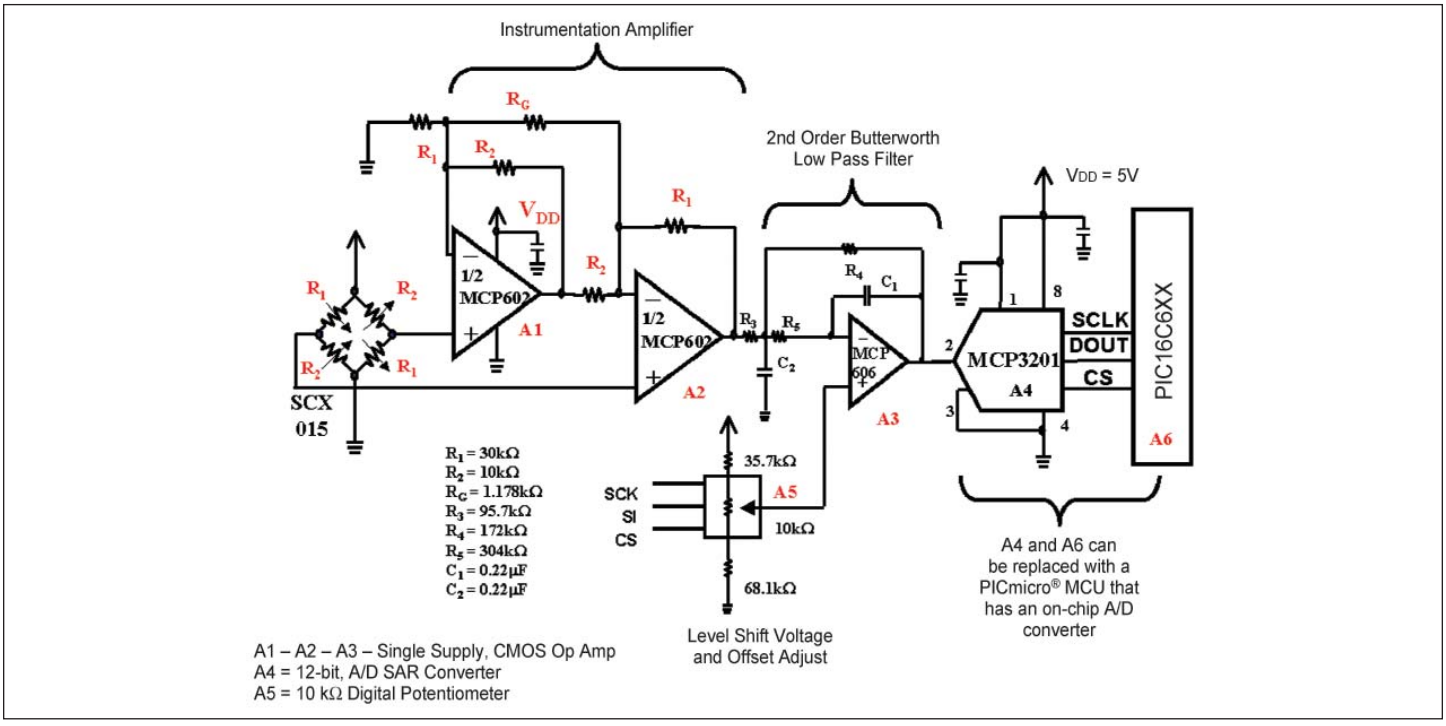


Figure 1: *The voltage at the output of the SCX015 pressure sensor is gained by the instrumentation amplifier (A1 and A2). Following the instrumentation amplifier a low pass filter (A3) is inserted to eliminate aliased noise from the 12-bit A/D converter conversion.*

An Intuitive Approach to Mixed Signal Layout – Part 5

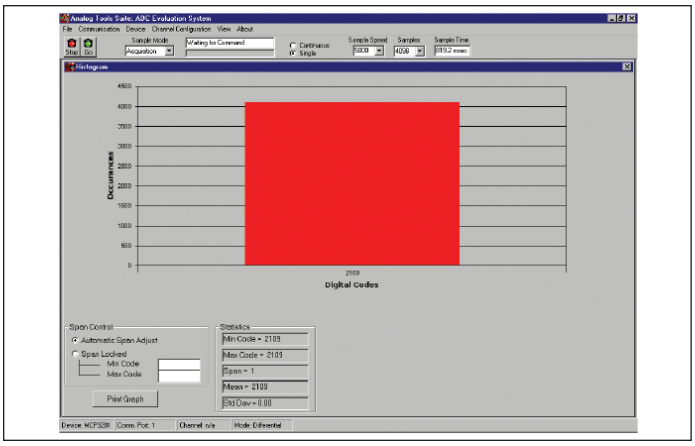


Figure 3: *Once the power supply noise has been sufficiently reduced, the output code of the MCP3201 is consistently one code, 2108*

Interfering External Clocks

Another source of systematic noise can come from clock sources or digital switching in the circuit. If this type of noise is correlated with the conversion process, it won't appear as interference in the conversion process. However, if it is uncorrelated, it can easily be found with an FFT analysis.

An example of clocking signal interference is shown in the FFT plot in Figure 4. With this plot, the circuit shown in Figure 1 is used with the by-pass capacitors installed. The spurs seen in the FFT plot shown in Figure 4 are generated by a 19.84 MHz clock signal on the board. In this instance, layout has been done with little regard for trace to trace coupling. The negligence to this detail appears in the FFT plot.

This problem can be solved by changing the layout to keep high impedance analog traces away from digital switching traces or implementing an anti-aliasing filter in the analog signal path prior to the A/D converter. Random trace to trace coupling is somewhat more difficult to find. In these instances, time domain analysis can be more productive.

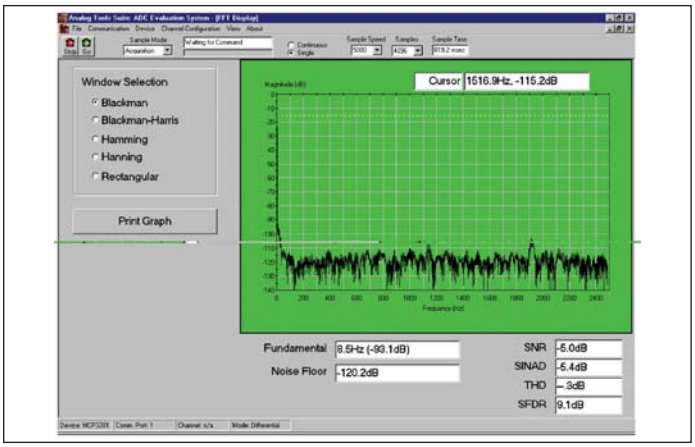


Figure 4: *Digital noise coupled into analog traces is sometimes misunderstood as broadband noise. An FFT plot easily pulls out this so called "noise" into an identifiable frequency so the source can be identified.*

Improper Use of Amplifiers

Returning to the circuit shown in Figure 1, a 1 kHz AC signal is injected at the positive input to the instrumentation amplifier. This signal would not be characteristic of this pressure sensing, however, this example is used to illustrate the influence of devices in the analog signal path.

The performance of this circuit with the above conditions is shown in the FFT plot in Figure 5. It should be noticed that the fundamental seems to be distorted and there are numerous harmonics with the same distortion. The distortion is caused by overdriving the amplifier slightly into the rails. The solution to this problem is to lower the amplifier gain.

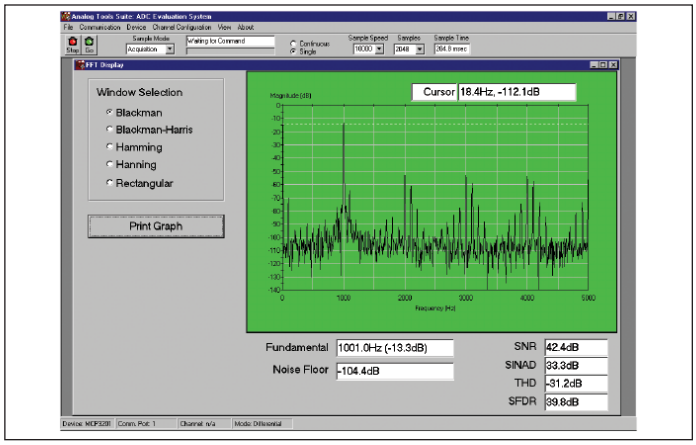


Figure 5: *Slightly overdriving an amplifier can generate a distortion in the signal. The FFT plot of this type of conversion quickly points out that the signal is distorted.*

Conclusion

Solving signal integrity problems can take a great deal of time particularly if you don't have the tools to tackle the tough issues. The three best analysis tools to have in your "box of tricks" are the frequency analysis (FFT), time analysis (scope photo) and DC analysis (Histogram) tools. We used many of these tools to identify the power supply noise, external clock noise and overdriven amplifier distortion.

An Intuitive Approach to Mixed Signal Layout – Part 6

Layout Tricks For A 12-Bit Sensing System

When I started writing this article I thought a "cookbook" approach would be appropriate when describing the implementation of a good 12-bit layout. My assumption behind this type of approach is that a reference design could be provided, which would make the layout implementation easy. But I struggled with this topic long enough to find that this notion was fairly unrealistic.

Because of the complexity of this problem, I am going to provide basic guidelines ending with a review of issues to be aware of while implementing your layout design. Throughout this discussion I will offer examples of good and bad layout implementations. I am doing this in the spirit of discussing concepts and not with the intent of recommending one layout as the only one to use.

The application circuit that I'm going to use is a load cell circuit that accurately measures the weight applied to the sensor, then displays the results on an LCD display screen. The circuit diagram for this system is shown in Figure 1. The load cell that I used can be purchased from Omega (LCL-816G). My sensor model for the LCL-816G is a four element resistive bridge that requires voltage excitation. With a 5V excitation voltage applied to the high side of the sensor, the full scale output swing is a ±10 mV differential signal with a 32 ounce maximum excitation. This small differential signal is gained by a two-op amp instrumentation amplifier. I chose a 12-bit converter to match the required precision of this circuit. Once the converter digitizes the voltage presented at its input, the digital code is sent to a microcontroller using the converter's SPI™ port. The microcontroller then uses a look-up table to convert the digital signal from the ADC into weight. Linearization and calibration activities can be implemented with controller code at this point if need be. Once this is done the results are sent to the LCD display. As a final step, I wrote the firmware for the controller. Now the design is ready to go to board layout.

One Major Step Towards Disaster

As I look at this complete circuit diagram I am tempted to use an auto router tool in my layout software. This is my first mistake. I have found that when I use this type of tool I often will go back and make significant changes to the layout. If the tool is capable of implementing layout restrictions, I may have a fighting chance. If my auto-routing tool does not have a restriction option, the best approach is to not use it at all.

General Layout Guidelines

Device Placement

Now that I am working on this layout manually, my first step is to place the devices on the board. This critical step is done effectively because I am keeping track of my noise-sensitive devices and noise-creator devices. There are two guidelines that I use to accomplish this task:

1. Separate the circuit devices into two categories: high speed (>40 MHz) and low speed. When you can, place the higher speed devices closer to the board connector/power supply.
2. Separate the above categories into three subcategories: pure digital, pure analog and mixed signal. With this delineation, place the digital devices closer to the board connector/power supply.

The board layout strategy should map the diagram shown in Figure 2. Notice Figure 2a, the relationship of high speed versus slower speeds to the board connector/power supply. In Figure 2b, the digital and analog circuit is shown as being separate from the digital devices, which are closest to the board connector/power supply. The pure analog devices are furthest away from the digital devices to insure that switching noise is not coupled into the analog signal path. The layout treatment of the A/D converters is discussed in detail in part 4 of this 6-part series (*Layout Techniques To Use As The ADC Accuracy And Resolution Increase*).

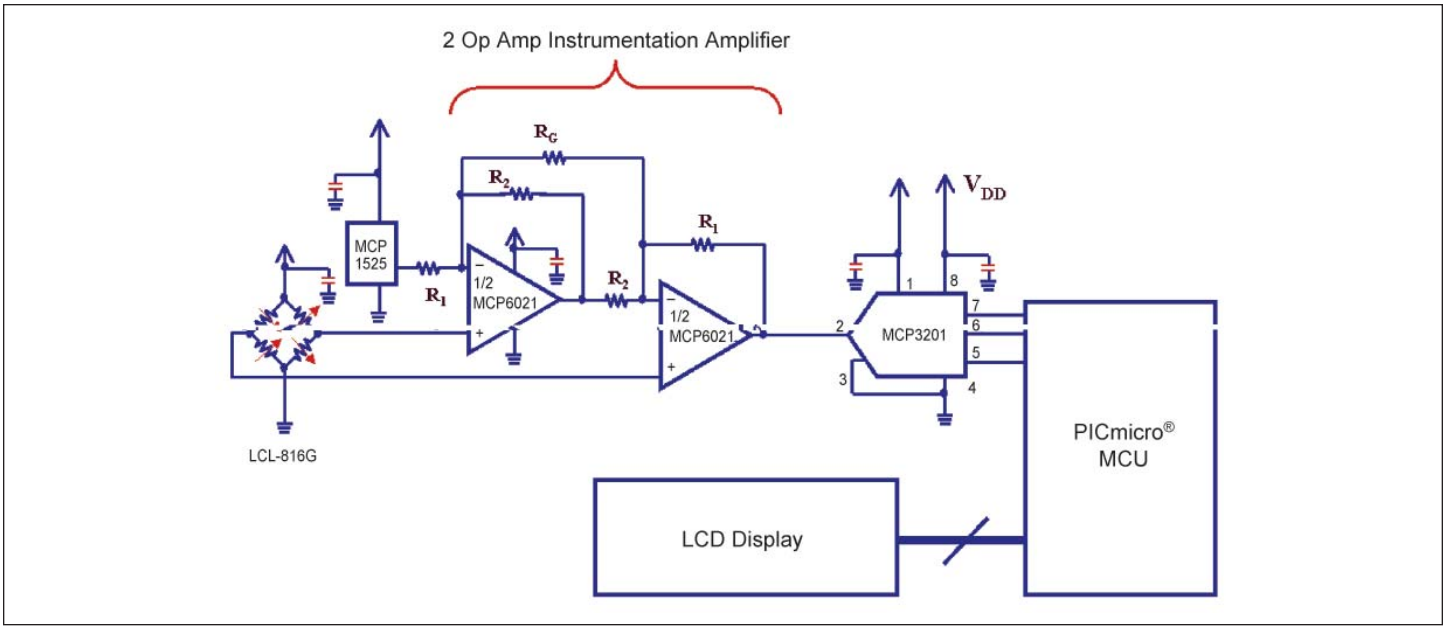


Figure 1: *The signal at the output of the load-cell sensor is gained by a two-op amp instrumentation amplifier, filtered and digitized with a 12-bit A/D Converter, MCP3201. The result of each conversion is displayed on the LCD display*

An Intuitive Approach to Mixed Signal Layout – Part 6

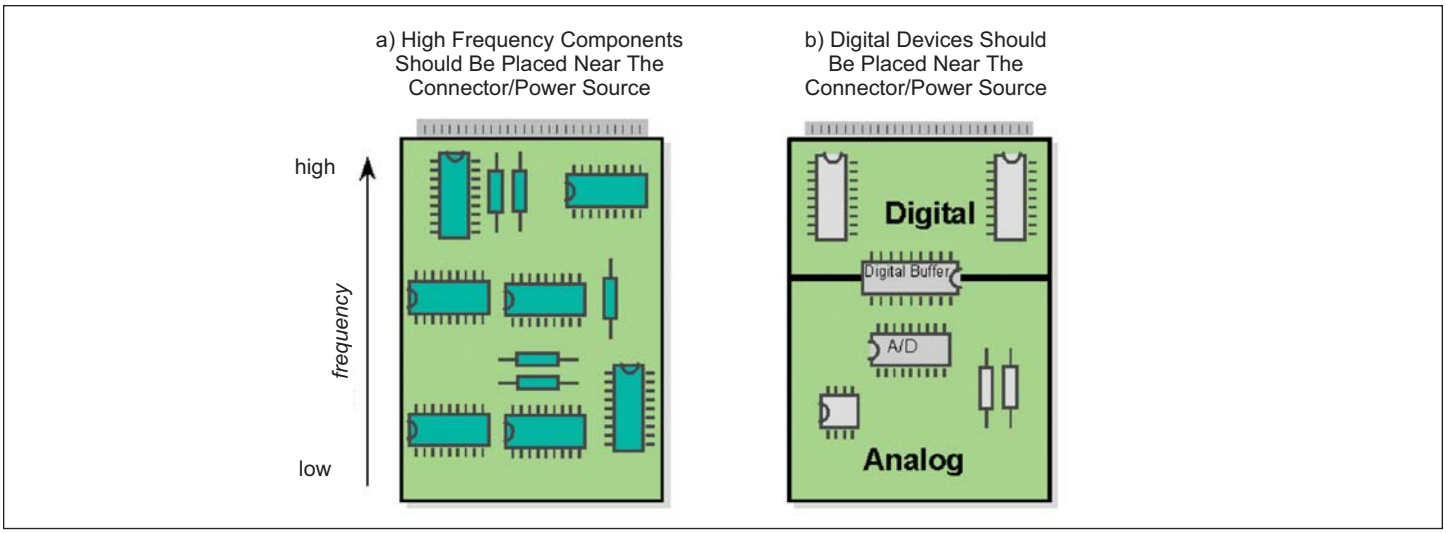


Figure 2: *The placement of active components on a PCB is critical in precision 12-bit+ circuits. This is done by placing higher frequency components (a) closer to the connector and digital devices (b) closer to the connector.*

Ground and Power Supply Strategy

Once I determine the general location of the devices, my ground planes and power planes are defined. My strategy of the implementation of these planes is a bit tricky.

First of all, it is dangerous for me not to use a ground plane in a PCB implementation. This is true particularly in analog and/or mixed-signal designs. One issue is that ground noise problems are more difficult to deal with than power supply noise problems because analog signals are referenced to ground. For instance, in the circuit shown in Figure 1, the A/D converter's inverting input pin (MCP3201) is connected to ground. Secondly, the ground plane also serves as a shield against emitted noise. Both of these problems are easy to resolve with a ground plane and nearly impossible to overcome if there is no ground plane.

However, with my small design, I assume that I won't need a ground plane. A ground plane-less layout implementation of the circuit in Figure 1 is shown in Figure 3.

Does my "no ground plane is required" theory play out? The proof is in the pudding, or data. In Figure 4, 4096 samples were taken from the A/D converter and logged. No excitation is applied to the sensor when this data is taken. With this circuit layout, the controller is dedicated to inter facing with the converter and sending the converter's results to the LCD display.

Figure 5 shows the same device layout shown in Figure 3 but a ground plane on the bottom layer is added. The ground plane (Figure 5b) has a few breaks due to signal. These breaks should be kept to a minimum. Current return paths should not be "pinched" as a consequence of these traces restricting the easy flow of current from the device to the power connector. The histogram for the A/D converter output is shown in Figure 6. Compared to Figure 4, the output codes are much tighter. The same active devices were used for both tests. The passive devices were different causing a slight offset difference.

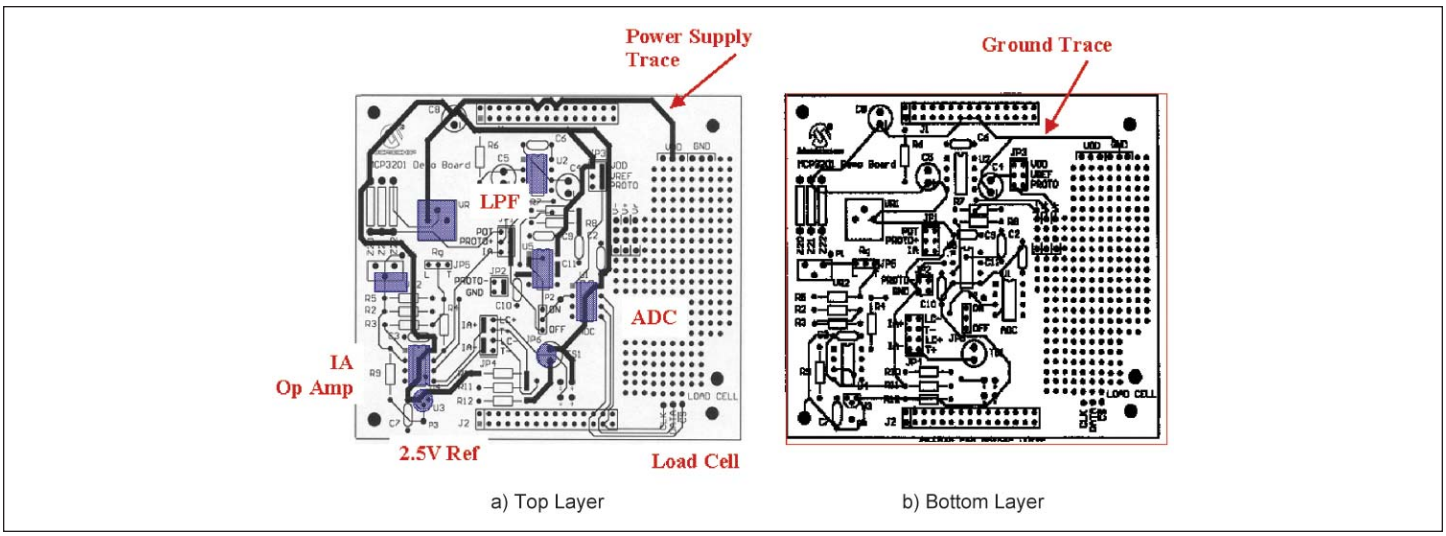


Figure 3: *Layout of the top (a) and bottom (b) layers of the circuit in Figure 1. Note that this layout does not have a ground or power plane. Note that the power traces are made considerably wider than the signal traces in order to reduce power supply trace inductance.*

An Intuitive Approach to Mixed Signal Layout – Part 6

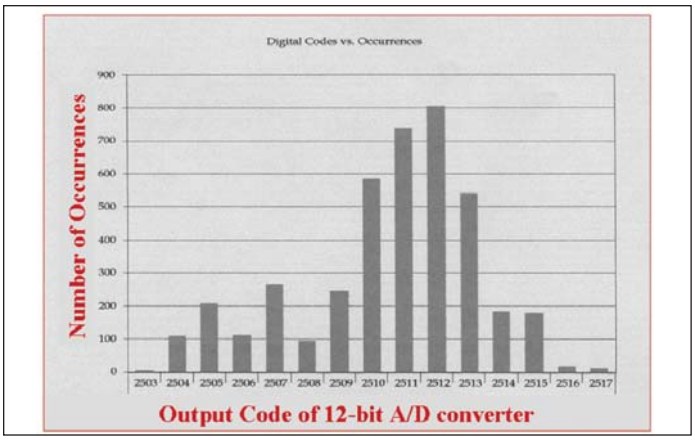


Figure 4: *This is a histogram of 4096 samples from the output of the A/D converter from a PCB that does not have a ground or power plane as shown in the PCB layout in Figure 3. The code of the noise from the circuit is 15 codes wide.*

It is clear from my data that a ground plane does have an effect on the circuit noise. When my circuit did not have a ground plane, the width of the noise was ~15 codes. When I added a ground plane, I improved the performance by almost 1.5X or 15/11. It should be noted that my test set up was in the lab where EMI interference is relatively low.

Because of the noise shown with the A/D converter my digital code is assignable to the op-amp noise and the absence of an anti-aliasing filter. If my circuit has a "minimum" amount of digital circuitry on board, a single ground plane and a single power plane may be appropriate. My qualifier "minimum" is defined by the board designer. The danger of connecting the digital and analog ground planes together is that my analog circuitry can pick-up the noise on the supply pins and couple it into the signal path. In either case, my analog and digital grounds and power supplies should be connected together at one or more points in the circuit to insure that my power supply, input and output ratings of all of the devices are not violated.

The inclusion of a power plane in a 12-bit system is not as critical as the required ground plane. Although a power plane can solve many problems, power noise can be reduced by making the power traces two or three times wider than other traces on the board and by using by-pass capacitors effectively.

Signal Traces

My signal traces on the board (both digital and analog) should be as short as possible. This basic guideline will minimize the opportunities for extraneous signals to couple into the signal path. One area to be particularly cautious of is with the input terminals of analog devices. These terminals normally have a higher impedance than the output or power supply pins. As an example, the voltage reference input pin to the A/D converter is most sensitive while a conversion is occurring. With the type of 12-bit converter I have in Figure 1, my input terminals (IN+ and IN-) are also sensitive to injected noise. Another potential for noise injection into my signal path is the input terminals of an operational amplifier. These terminals have typically 10^9 to $10^{13}\Omega$ input impedance.

My high impedance input terminals are sensitive to injected currents. This can occur if the trace from a high impedance input is next to a trace that has fast changing voltages, such as a digital or clock signal. When a high impedance trace is in close proximity to a trace with these types of voltage changes, charge is capacitively coupled into the high impedance trace.

The relationship between two traces is shown in Figure 7. In this diagram the value of the capacitance between two traces is primarily dependent on the distance (d) between the traces and the distance that the two traces are in parallel (*L*). From this model, the amount of current generated into the high impedance trace is equal to:

$I = C\ dV/dt$

Where: I = current that appears on the high impedance trace
C = value of capacitance between the two PCB traces
dV = change in voltage of the trace that is switching
dt = amount of time that the voltage change took to get from one level to the next

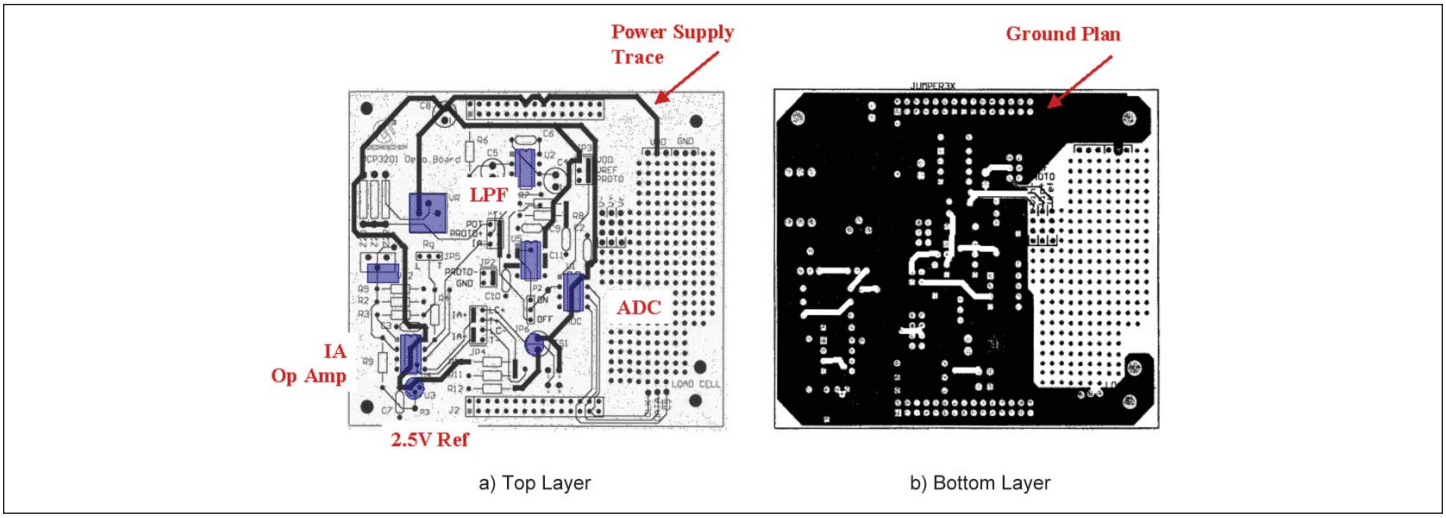


Figure 5: *Layout of the top and bottom layers of the circuit in Figure 1. Note that this layout DOES have a ground plane.*

An Intuitive Approach to Mixed Signal Layout – Part 6

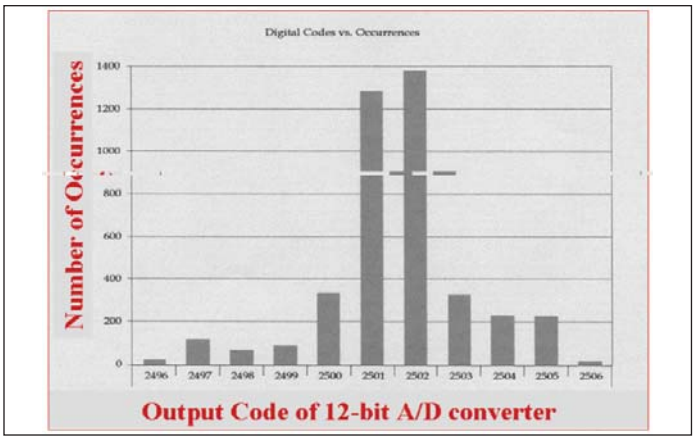


Figure 6: *This is a histogram of 4096 samples from the output of the A/D converter on the PCB that has a ground plane as shown in the PCB layout in Figure 5. The code width of the noise is now 11 codes wide.*

Did I Say By-pass And Use An Anti-Aliasing Filter?

Although this article is about layout practices, I thought it would be a good idea to cover some of the basics in circuit design. A good rule concerning by-pass capacitors is to always include them in the circuit. If they are not included the power supply noise may very well eliminate any chance for 12-bit precision.

By-pass Capacitors

By-pass capacitors belong in two locations on the board: one at the power supply (10 µF to 100 µF or both) and one for every active device *(digital and analog)*. The value of the *device's* by-pass capacitor is dependent on the *device* in question. If the bandwidth of the *device* is less than or equal to ~1 MHz, a 1 µF will reduce injected noise dramatically. If the bandwidth of the *device* is above ~10 MHz, a 0.1 µF capacitor is probably appropriate. In between these two frequencies, both or either one could be used. Refer to the manufacturer's guidelines for specifics.

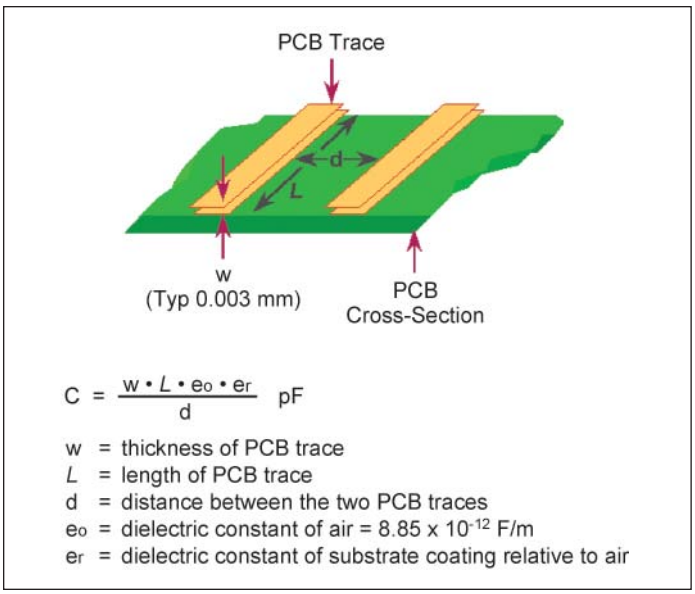


Figure 7: *A capacitor can be constructed on a PCB by placing two traces in close proximity. With this PCB capacitor, signals can be coupled between the traces.*

Every active device on the board requires a by-pass capacitor. It must be placed as close as possible to the power supply pin of the device as shown in Figure 5. If two by-pass capacitors are used for one device, the smaller one should be closest to the device pin. Finally, the lead length of the by-pass capacitor should be as short as possible.

Anti-Aliasing Filters

You will note that the circuit in Figure 1 does not have an anti-aliasing filter. As the data shows, this oversight has caused noise problems in the circuit. When this board has a 4th order, 10 Hz, anti-aliasing filter inserted between the output of the instrumentation amplifier and the input of the A/D converter, the conversion response improves dramatically. This is shown in Figure 8.

Analog filtering can remove noise superimposed on the analog signal before it reaches the A/D converter. In particular, this includes extraneous noise peaks. Analog-to-Digital converters will convert the signal that is present on its input. This signal could include that sensor voltage signal or noise. The anti-aliasing filter removes the higher frequency noise from the conversion process.

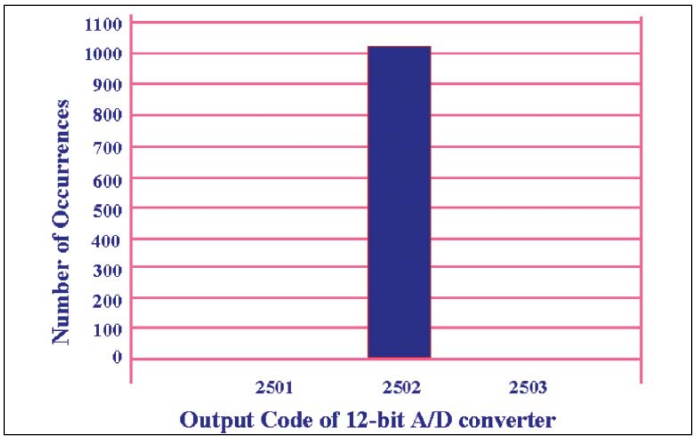


Figure 8: *This diagram shows the conversion results of the circuit in Figure 1 plus a 4th order, anti-aliasing filter. Additionally, the board layout includes a ground plane.*

PCB Design Check List

Good 12-bit layout techniques are not difficult to master as long as you follow a few guidelines:

1. Check device placement versus connectors. Make sure that high-speed devices and digital devices are closest to the connector.
2. Always have at least one ground plane in the circuit.
3. Make power traces wider than other traces on the board.
4. Review current return paths and look for possible noise sources on ground connects. This is done by determining the current density at all points of the ground plane and the amount of possible noise present.
5. By-pass all devices properly. Place the capacitors as close to the power pins of the device as possible.
6. Keep all traces as short as possible.
7. Follow all high impedance traces looking for possible capacitive coupling problems from trace to trace.
8. Make sure your signals in a mixed-signal circuit are properly filtered.

Keeping Power Hungry Circuits Under Thermal Control

Projectors, large power supplies, datacom switches and routers, pose an interesting heat dissipation problem. These applications consume enough power to prompt a designer to cool off the electronics with a fan. If the appropriate airflow across the electronics is equal to or less than six to seven Cubic Feet per Minute (CFM), a good choice of fan would be the DC brushless fan.

The fan speed of a DC brushless fan can be driven and controlled by the electronics in a discrete solution, a microprocessor circuit or a stand-alone fan controller IC. A discrete solution can be highly customized but can be real-estate hungry. Although this solution is a low cost alternative, it is challenging to implement "smart" features, such as predictive fan failure or false fan failure alarm rejection. Additionally, the hardware troubleshooting phase for this system can be intensive as the feature set increases.

If you have a multiple fan application, the best circuit to use is a microcontroller-based system. With the microcontroller, all the fans and temperatures of the various environments can be economically controlled with this one chip solution and a few external components. The "smart" features that are difficult to implement with discrete solutions are easily executed with the microcontroller. The firmware of the microcontroller can be used to set threshold temperatures and fan diagnostics for an array of fans. Since the complexity of this system goes beyond the control of one fan, the firmware overhead and firmware debugging can be an issue.

For a one-fan circuit, the stand-alone fan controller IC is the better choice. The stand-alone IC has fault detect circuitry that can notify the system when the fan has failed, so that the power consuming part of the system can be shut down. The stand-alone IC fan fault detection capability rejects glitches, ensuring that false alarms are filtered. It can economically be used to sense remote temperature with a NTC thermistor or with the internal temperature sensor on-chip. As an added benefit, the stand-alone IC can be used to detect the fan faults of a two-wire fan, which is more economical than its three-wire counterpart.

Regardless of the circuit option that is used, there are three primary design issues to be considered in fan control circuits, once the proper location of the fan is determined. These three design issues are: fan excitation, temperature monitoring and fan noise.

The circuit in Figure 1 illustrates how a two-wire fan can be driven with a stand-alone IC. In this circuit, the TC647B performs the task of varying the fan speed based on the temperature that is sensed from the NTC thermistor. The TC647B is also able to sense fan operation, enabling it to indicate when a fan fault has occurred.

The speed of a brushless DC fan can be controlled by either varying the voltage applied to it linearly or by pulse width modulating (PWM) the voltage. The TC647B shown in Figure 1, drives the base of transistor Q1 with a PWM waveform, which in turn drives the voltage that is applied to the fan.

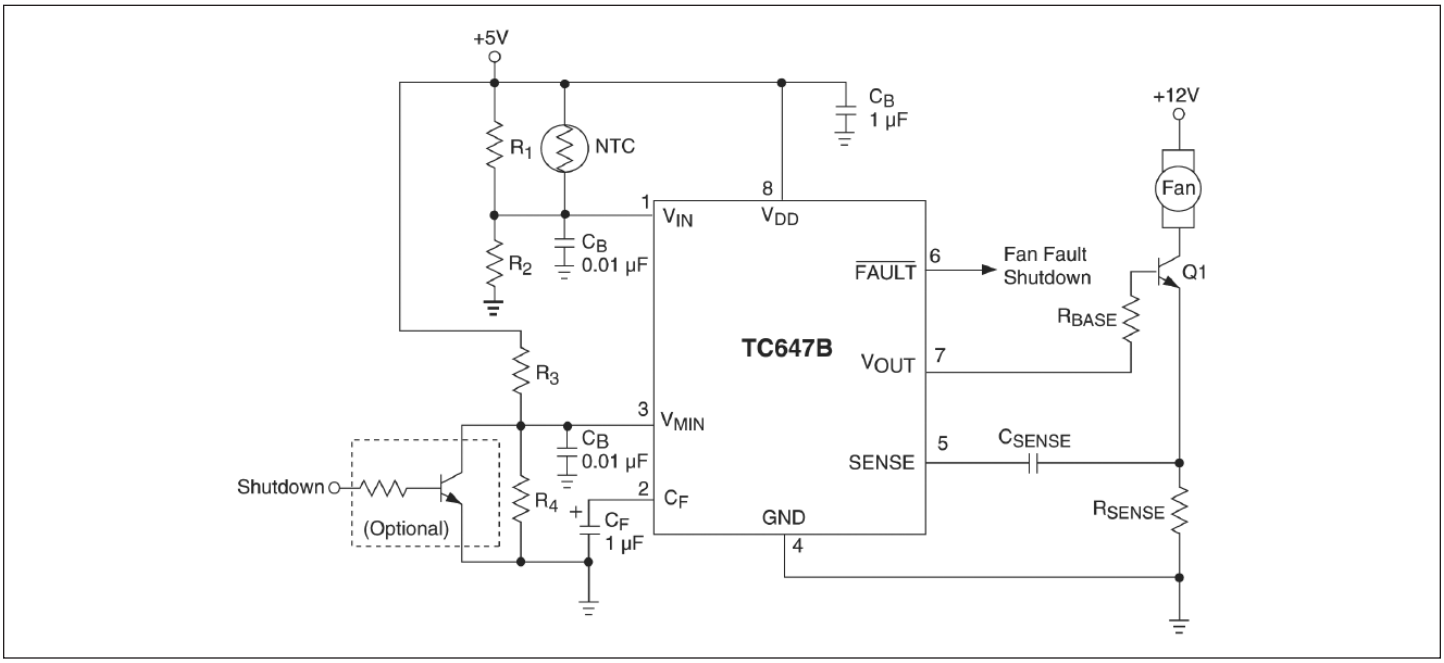


Figure 1: *A two-wire fan can easily be driven and controlled by a thermistor-connected TC647B.*

By varying the pulse width of the PWM waveform, the speed of the fan can be increased or decreased. The pulse width modulation method of fan speed control is more efficient than the linear regulation method.

The voltage across RSENSE and the voltage at the SENSE pin during PWM mode operation are shown in Figure 2. The voltage at the sense resistor has both DC and AC content. The AC content is generated by the commutation of the current in the fan motor windings. These voltage transients across RSENSE are coupled through CSENSE to the SENSE pin of the TC647B. This removes the DC content of the sense resistor voltage. There is an internal resistor, 10 kΩ to ground, on the SENSE pin. The SENSE pin senses voltage pulses, which communicate fan operation to the TC647B. If pulses are not detected by the SENSE pin for one second, a fault condition is indicated by the TC647B.

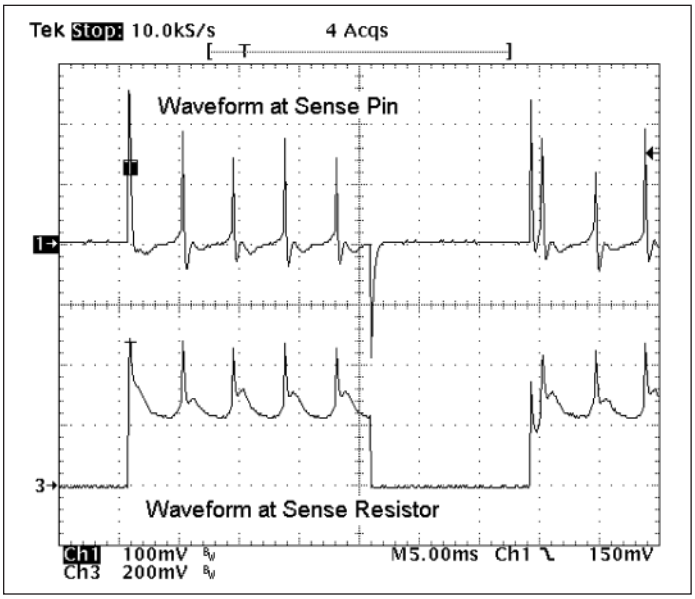


Figure 2: *The fan response (across RSENSE) to the PWM signal at VOUT, is shown in the bottom trace. The capacitively coupled signal to the SENSE pin of the TC647B is shown in the top trace.*

The temperature can easily be measured with an economic solution, such as a thermistor. The thermistor is fast, small, requires a two-wire interface and has a wide range of outputs. As an added benefit, the layout flexibility is enhanced by being able to place the thermistor remote from the TC647B. Although thermistors are non-linear, they can be linearized over a smaller temperature range (±25°C) with the circuits shown in Figure 3. This linearization and level shifting is done using standard, 1% resistors.

Although temperature proportional fan speed control and fan fault detection for two-wire fans can be implemented in a discrete circuit or the microcontroller version, it requires a degree of attention from the designer. The TC647B is a switch mode two-wire brushless DC fan speed controller. Pulse Width Modulation (PWM) is used to control the speed of the fan in relation to the thermistor temperature. Minimum fan speed is set by a simple resistor divider on VMIN. An integrated Start-up Timer ensures reliable motor start-up at turn-on, coming out of shutdown mode or following a transient fault with auto-fan restart capability.

The TC647B also uses Microchip's FanSense™ technology, which improves system reliability. All of these features included in a single chip, gives the designer a leg up in a single fan implementation.

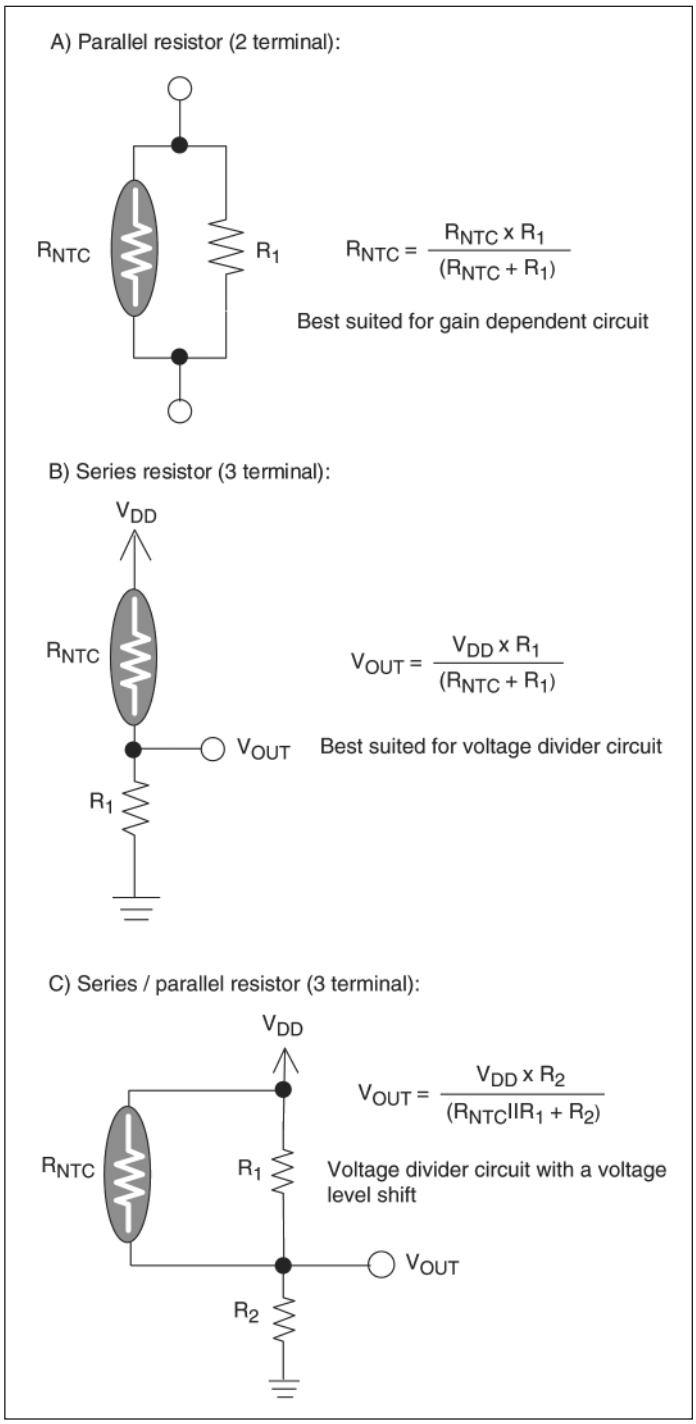


Figure 3: *A thermistor can be linearized over 50°C with a standard resistor (A and B) as well as level shifted (C) to match the input requirements of the TC647B.*

Instrumentation Electronics At A Juncture

Process control and instrumentation solutions rose out of the 1970s/1980s revolution in electronics. From that endeavor the well-known instrumentation amplifier came into existence. Structures like a three op amp design, followed by a two-op amp version were built discretely with a few resistors and op amps. This solution was later made available on an integrated chip. It may seem that things haven't changed much since then, but not so. The digital revolution, that is just coming into its own, is now encroaching on that traditional analog territory.

Instrumentation amplifiers are good for gaining differential input signals and rejecting common mode noise, but fall short when there are multiple sensor inputs that need to be integrated into the system. For instance, a pressure sensor or load cell require an instrumentation amplifier to change their differential output signal into a single voltage. But often these systems need temperature data for calibration. This temperature data is acquired through a separate signal path.

An alternative to having two separate signal paths is to use a single-ended input/output Programmable Gain Amplifier (PGA). With this device, the signal subtraction, common mode noise rejection and some filtering of the differential input signal is performed inside the microcontroller. The PGA also allows for multiple input channels, which is configurable using the SPI™ port. A large number of sensors can be configured to the PGA inputs. An example is shown in Figure 1.

The type of resistive sensor bridge, shown in Figure 1, is primarily used to sense pressure, temperature or load. An external A/D converter and the PGA can easily be used to convert the difference voltage from these resistor bridge sensors to usable digital words. A block diagram of Microchip's PGA is shown in Figure 2.

At the input of this device there is a multiplexer, which allows the user to interface to multiple inputs. This multiplexer is directly connected to the non-inverting input of a wide bandwidth amplifier. The programmable closed loop gain of this amplifier is implemented using an on-chip resistor ladder. The eight programmable gains are, 1, 2, 4, 5, 8, 10, 16 and 32.

The multiplexer and high-speed conversion response of the PGA and A/D combination allows a differential input signal to be quickly sampled and converted into their 12-bit digital representation. The PIC® microcontroller subtracts the two signals from CH0 and CH1. While the subtraction of the two signals is implemented to calculate the sensor response, the lower frequency common mode noise is also eliminated.

Although it is simple to measure temperature in a stand-alone system without the help of the PGA, a variety of problems can be eliminated by implementing temperature sensing capability in a multiplexed environment. One of the main advantages is that a second signal path to the microcontroller can be eliminated, while still maintaining the accuracy of the sensing system. The multiplexed versions of PGAs are the MCP6S22 (two channel), MCP6S26 (six channel) and MCP6S28 (eight channel). The most common sensors for temperature measurements are the thermistor, silicon temperature sensor, RTD and thermocouple. Microchip's PGAs are best suited to inter face to the thermistor or silicon temperature sensor. Photo sensors bridge the gap between light and electronics. The PGA is not well suited for precision applications such as, CT scanners, but they can be effectively used in position photo sensing applications. The multiplexer and high-speed conversion response of the PGA and A/D combination allows the photo sensor input signal to be sampled and converted in the analog domain and quickly converted to the digital domain. This photo sensing circuit is appropriate for signal responses from DC to ~100 kHz.

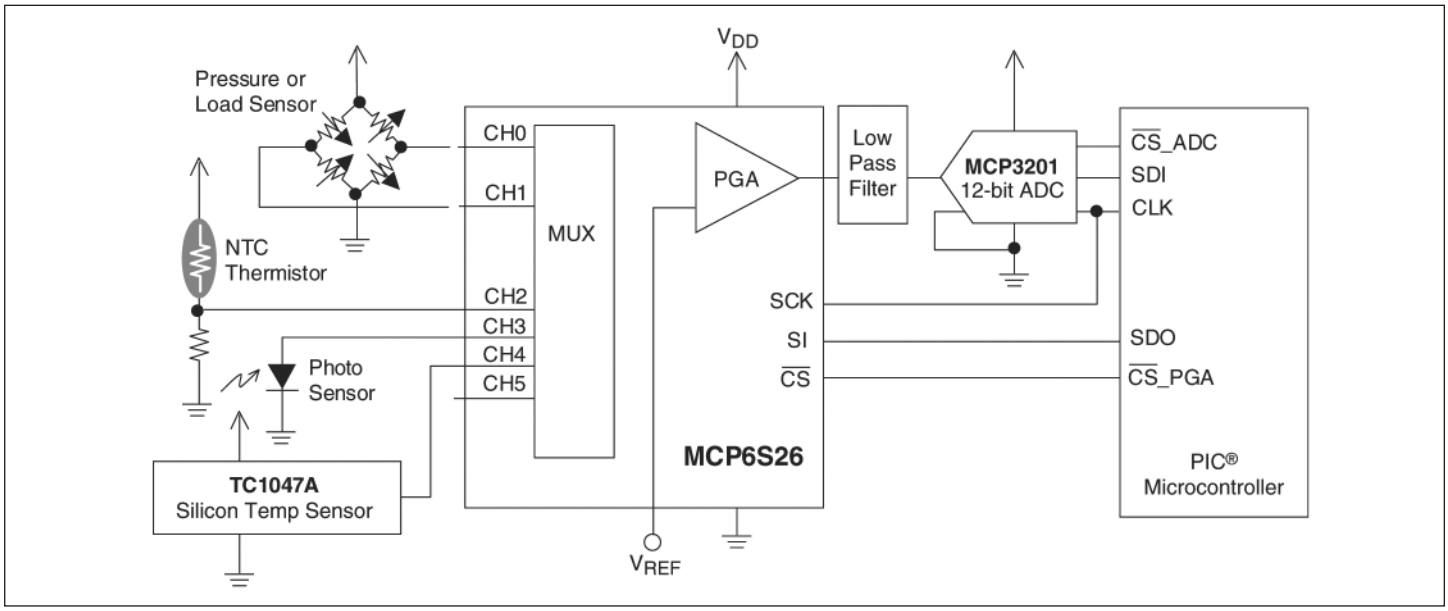


Figure 1: *The PGA device can be used to gain signals from a variety of sensors, such as a resistive bridge, an NTC temperature sensor, a silicon photo sensor or a silicon temperature sensor.*

Analog Design Notes

The MCP6S2X is a PGA family that uses a precision, wide bandwidth internal amplifier. This precision device not only offers excellent offset voltage performance, but the configurations in these sensing circuits are easily designed without the headaches of stability that the stand-alone amplifier circuits present to the designer. Stability with these programmable gain amplifiers has been built-in.

For more information, access the following list of references at: www.microchip.com.

Recommended References

AN248 “Interfacing MCP6S2X PGAs to PICmicro® Microcontroller”, Ezana Haile, Microchip Technology Inc.

AN251 “Bridge Sensing with the MCP6S2X PGAs”, Bonnie C. Baker, Microchip Technology Inc.

AN865 “Sensing Light with a Programmable Gain Amplifier”, Bonnie C. Baker, Microchip Technology Inc.

AN867 “Temperature Sensing with a Programmable Gain Amplifier”, Bonnie C. Baker, Microchip Technology Inc.

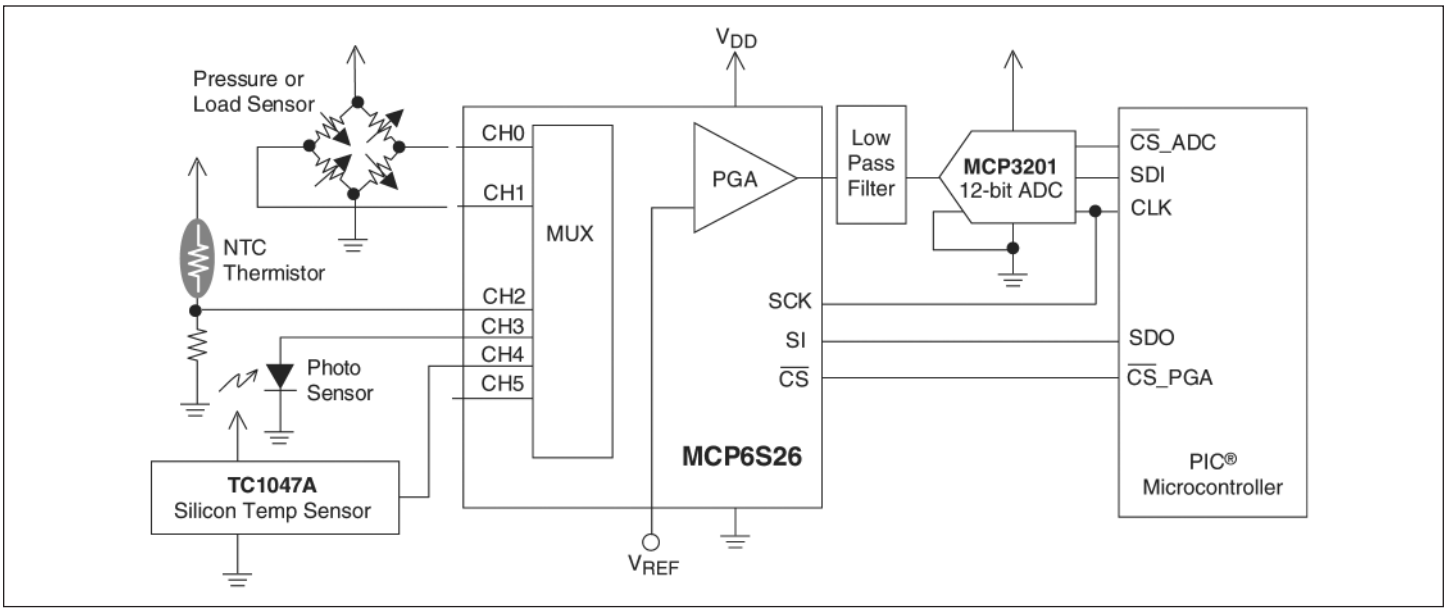


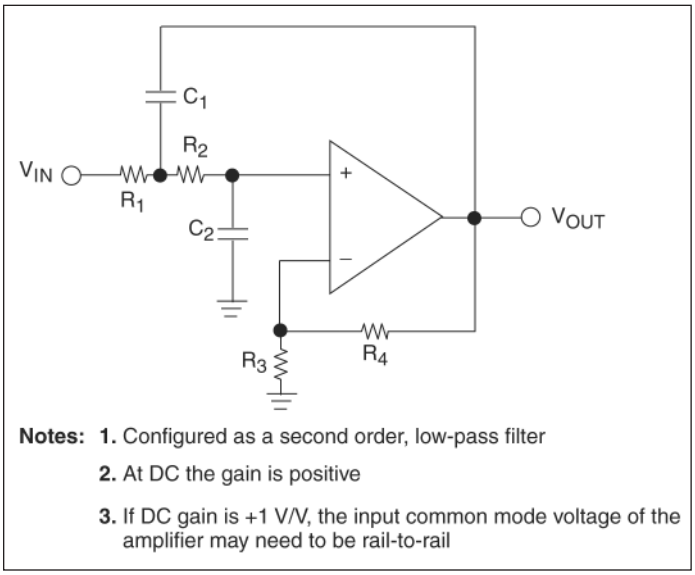
Figure 2: *Programmable Gain Amplifier (PGA) Block Diagram. The PGA has an internal amplifier that is surrounded by a programmable resistor ladder. This ladder is used to change the gain through the SPI™ port. An analog multiplexer precedes the non-inverting input of the amplifier to allow the user to configure this device from multiple inputs.*

Select The Right Operational Amplifier For Your Filtering Circuits

Analog filters can be found in almost every electronic circuit. Audio systems use them for preamplification and equalization. In communication systems, filters are used for tuning specific frequencies and eliminating others. But if an analog signal is digitized, low-pass filters are always used to prevent aliasing errors from out-of-band noise and interference.

Analog filtering can remove higher frequency noise superimposed on the analog signal before it reaches the Analog-to-Digital converter. In particular, this includes low-level noise as well as extraneous noise peaks. Any signal that enters the Analog-to-Digital converter is digitized. If the signal is beyond half of the sampling frequency of the converter, the magnitude of that signal is converted reliably, but the frequency is modified as it aliases back into the digital output. You can use a digital filter to reduce the noise after digitizing the signal, but keep in mind the rule of thumb: "Garbage in will give you garbage out".

The task of selecting the correct single supply operational amplifier (op amp) for an active low-pass filter circuit can appear overwhelming, as you read any op amp data sheet and view all of the specifications. For instance, the number of DC and AC Electrical Specifications in Microchip's 5 MHz, single supply, MCP6281/2/3/4 data sheet is twenty-four. But in reality, there are only two important specifications that you should initially consider when selecting an op amp for your active, low-pass filter. Once you have chosen your amplifier, based on these two specifications, there are two additional specifications that you should consider before reaching your final decision. The most common topologies for second order, active low-pass filters are shown in Figure 1 and Figure 2.



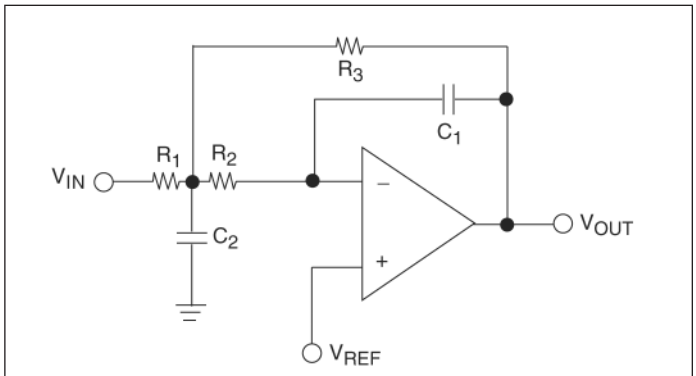
Notes: **1.** Configured as a second order, low-pass filter

2. At DC the gain is positive

3. If DC gain is +1 V/V, the input common mode voltage of the amplifier may need to be rail-to-rail

Figure 1: *Second order, Sallen-Key, Low-pass filter.*

In Figure 1, the non-inverting Sallen-Key is designed so that the input signal is not inverted. A gain option is implemented with R_3 and R_4. If you want a DC gain of +1 V/V, R_3 should be removed and R_4 should be shorted. A second order, Multiple Feedback configuration is shown in Figure 2. With this circuit topology, the input signal is inverted around the reference voltage, V_{REF}. If a higher order filter is needed, both of these topologies can be cascaded.



Notes: **1.** Configured as a second order, low-pass filter

2. At DC the gain is negative

3. Will usually require a voltage reference in single supply applications

Figure 2: *Second order, Multiple Feedback, Low-pass filter.*

The two key specifications that you should initially consider when designing with either of these topologies is Gain Bandwidth Product and Slew Rate. Prior to the selection of the op amp, you need to determine the filter cutoff frequency (f_C), also known as the frequency where your filter starts to attenuate the signal. Sometimes, in literature, you will find that this is called the passband frequency. Once this is done, the filter design software program, FilterLab® (available at www.microchip.com), can be used to determine the capacitor and resistor values.

Since you have already defined your cutoff frequency, selecting an amplifier with the right bandwidth is easy. The closed-loop bandwidth of the amplifier must be at least 100 times higher than the cutoff frequency of the filter. If you are using the Sallen-Key configuration and your filter gain is +1 V/V, the Gain Bandwidth Product (GBWP) of your amplifier should be equal to or greater than 100 f_C. If your closed loop gain is larger than +1 V/V, your GBWP should be equal to or greater than 100 $G_{CLN}f_C$, where G_{CLN} is equal to the non-inverting closed-loop gain of your filter. If you are using the Multiple Feedback configuration, the GBWP of your amplifier should be equal to or greater than 100*(-G_{CLI} + 1)f_C, where G_{CLI} is equal to the inverting gain of your closed-loop system.

Microchip's gain bandwidth op amp products are shown in Table 1.

In addition to paying attention to the bandwidth of your amplifier, the Slew Rate should be evaluated in order to ensure that your filter does not create signal distortions. The Slew Rate of an amplifier is determined by internal currents and capacitances. When large signals are sent through the amplifier, the appropriate currents charge these internal capacitors. The speed of this charge is dependent on the value of the amplifier's internal resistances, capacitances and currents. In order to ensure that your active filter does not enter into a slew condition you need to select an amplifier such that the Slew Rate ($2\pi V_{OUT\ P\text{-}P}\ f_C$), where $V_{OUT\ P\text{-}P}$ is the expected peak-to-peak output voltage swing below f_C of your filter.

There are two, second order specifications that affect your filter circuit. These are Input Common Mode Voltage Range (V_{CMR}), for the Sallen-Key circuit and Input Bias Current (I_B). In the Sallen-Key configuration, V_{CMR} will limit the range of your input signal. The power supply current may or may not be a critical specification unless you have an application on a power budget.

Another second order specification to consider is the Input Bias Current. This specification describes the amount of current going in or out of the input pins of the amplifier. If you are using the Sallen-Key filter configuration, as shown in Figure 1, the input bias current of the amplifier will conduct through R_2. The voltage drop caused by this error will appear as an input offset voltage and input noise source. But more critical, high input bias currents in the nano or micro ampere range may motivate you to lower your resistors in your circuit. When you do this, you will increase the capacitors in order to meet your filter cutoff frequency requirements. Large capacitors may not be a very good option because of cost, accuracy and size. Also, be aware that this current will increase with temperature. Notice that most of the devices in Table 1 have Input Bias Current specifications in the pA range, therefore, higher value resistors are permissible.

If you follow these simple guidelines you will find that designing a successful low-pass filter is not that difficult and you will quickly have a working circuit.

Recommended References

AN699 "Anti-Aliasing, Analog Filters for Data Acquisition Systems", Bonnie C. Baker, Microchip Technology Inc.

FilterLab® Analog Filtering Software tool is available at: www.microchip.com

Device	GBWP (Typ)	Slew Rate (V/µs, Typ)	Input Common Mode Voltage with V_{DD} = 5V (V)	Input Bias Current at Room Temperature (Typ)
MCP6041/2/3/4	14 kHz	0.003	-0.3V to 5.3V	1 pA
TC1029/30/34/35	90 kHz	0.035	-0.2V to 5.2V	50 pA
MCP6141/2/3/4	100 kHz	0.024	-0.3V to 5.3V	1 pA
MCP606/7/8/9	155 kHz	0.08	-0.3V to 3.9V	1 pA
MCP616/7/8/9	190 kHz	0.08	-0.3V to 4.1V	-15 nA
MCP6001/2/4	1 MHz	0.6	-0.3V to 5.3V	1 pA
TC913	1.5 MHz	2.5	4.5V (V_{DD} = 6.5V)	90 pA (max)
MCP6271/2/3/4	2 MHz	0.9	-0.3V to 5.3V	1 pA
MCP601/2/3/4	2.8 MHz	2.3	-0.3V to 3.8V	1 pA
MCP6281/2/3/4	5 MHz	2.5	-0.3V to 5.3V	1 pA
MCP6021/2/3/4	10 MHz	7.0	-0.3V to 5.3V	1 pA
MCP6291/2/3/4	10 MHz	7.0	-0.3V to 5.3V	1 pA

Table 1: The four basic specifications shown will guide you in selecting the correct op amp for your low-pass filter.

Ease Into The Flexible CANbus Network

CANbus networks have been around for over 15 years. Initially this bus was targeted at automotive applications, requiring predictable, error-free communications. Recent falling prices of CAN (Controller Area Network) system technologies have made it a commodity item. The CANbus network has expanded past automotive applications. It is now migrating into systems like industrial networks, medical equipment, railway signaling and controlling building services (to name a few). These applications are utilizing the CANbus network, not only because of the lower cost, but because the communication that is achieved through this network is robust, at a bit rate of up to 1 Mbits/sec.

A CANbus network features a multi-master system that broadcasts transmissions to all of the nodes in the system. In this type of network, each node filters out unwanted messages. A classical client/server network (such as Ethernet) relies on network addressing to deliver data to a single node. If multiple nodes exist in this network, a star configuration implements a centralized control (Figure 1). Fewer microcontrollers are needed to perform the varied tasks, but the MCUs are usually more complex with higher pin counts.

In contrast, every node in a CAN system receives the same data at the same time. By default, CAN is message-based, not address-based. Multiple nodes are integrated in the system using a distributed control implementation (Figure 1). One of the advantages of this topology is that nodes can easily be added or removed with minimal software impact. The CAN network requires intelligence on each node, but the level of intelligence can be tailored to the task at that node. Consequently, these individual controllers are usually simpler, with lower pin counts. The CAN network also has higher reliability by using distributed intelligence and fewer wires.

Ethernet differs from CAN in that Ethernet uses collision detection at the end of the transmission. At the beginning of the transmission, CAN uses collision detection with resolution. When a collision occurs during arbitration between two or more CAN nodes that transmit at the same time, the node(s) with the lower priority message(s) will detect the collision. The lower priority node(s) will then switch to receiver mode and wait for the next bus idle to attempt transmission again.

The winning transmitter will continue to send its message as if nothing happened. Response time to collision resolution is faster because the correction occurs at the beginning of the transmission during arbitration of a message and the high priority message is not destroyed.

The CANbus network specification, written by Bosch, has been standardized by ISO and SAE. The entire CAN specification is standardized in ISO 11898-1. ISO 11898-2 contains the CAN physical layer specification. The CAN specification is not completely standardized in the SAE specification.

CANbus communication is achieved using message frames. The three types of frames are data, remote and error. Each frame has internal fields that define the type of frame that is being sent and then provides the pertinent information. For instance, a data frame is constructed with 6 fields: arbitration, control, data, CRC (Cyclic Redundancy Check), acknowledge and end-of-frame. During transmission, the arbitration field is used by every node on the network to identify and/or resolve collisions. The arbitration field is also used to identify the message type and destination. The control frame defines the data frame length. The data frame contains data and has the specified number of bytes per the control frame. The CRC frame is used to check for data errors. And finally, every transmission requires an acknowledge frame from all of the receivers on the CAN network.

In the CAN network multi-master environment, nodes can be added or removed without significant consequence to the operation and reliability of the system. An example of a single node for a CAN network is shown in Figure 2. In this diagram, pressure is measured using a Motorola® pressure sensor, MPX2100AP. The differential output voltage of this sensor is gained by a discrete instrumentation amplifier and filtered by a fourth order, low pass, active filter. The signal is then converted to a digital code with a 12-bit A/D converter, MCP3201. The receiving microcontroller sends the data to the CAN controller. The common language between the nodes is generated and maintained by the CAN controller and the voltage compliance to the network is managed by the CAN driver.

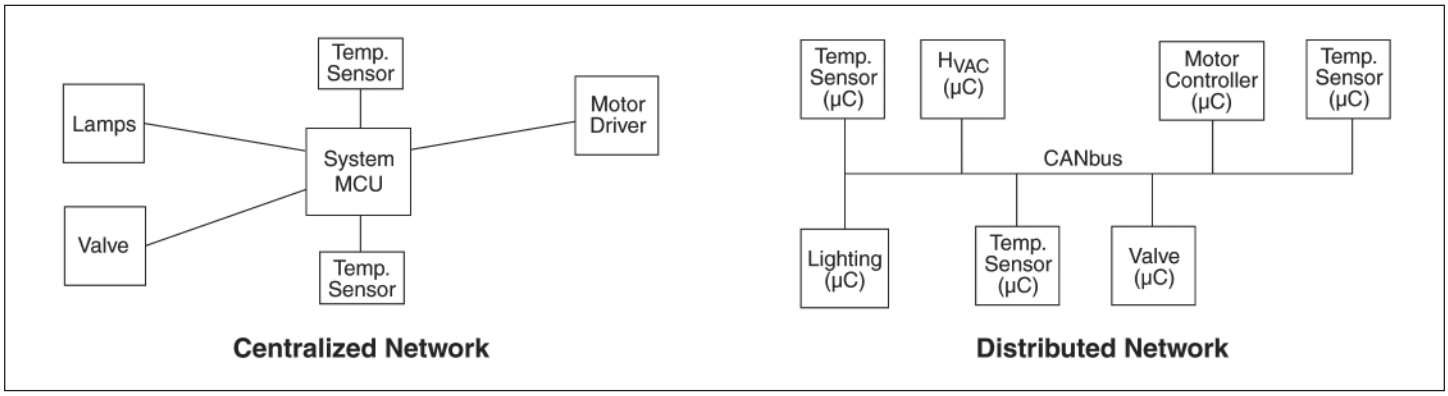


Figure 1: *For multi-task networks, a Centralized Network is usually used for Ethernet systems. If a node is added to this system, the system MCU could require significant modifications. With CAN networks, the Distributed Network is implemented. A node can easily be added or taken out of the system with minimal firmware changes.*

Each node in a CAN network can perform a unique function. Although Figure 2 illustrates a pressure sensing system, other types of systems can complement your application. Additionally, this block diagram of a CAN node can be implemented in a variety of ways. For instance, in the initial build, the microcontroller could have the CAN controller integrated on-chip. At a later date, nodes can easily be added with minimal software impact. When you are ready to add, enhance or build a small stand-alone network, the combination of an MCP2515 with a simple microcontroller would be a good choice.

The MCP2515 stand-alone CAN controller implements version 2.0B of the CAN specification. It is capable of transmitting and receiving both standard and extended data and remote frames. The MCP2515 has two acceptance masks and six acceptance filters that are used to remove unwanted messages. The 4-wire interface between the MCP2515 and the controller is SPI™. The MCU pins used for SPI can be recovered if the MCP2515 RXnBF pins are configured as GP output and the TXnRTS pins are configured as GP input.

The MCP2515 has three main blocks:

1. The CAN module, which includes the CAN protocol engine, masks, filters, transmits and receives buffers

2. The control logic and registers that are used to configure the device and its operation

3. The SPI protocol block

Typically, each node in a CAN system must have a device to convert the digital signals generated by a CAN controller, to signals suitable for transmission over the bus cabling. The device also provides a buffer between the CAN controller and the high-voltage spikes that can be generated on the CANbus by outside sources (EMI, ESD, electrical transients, etc.). The MCP2551 high-speed CAN, fault-tolerant device provides the interface between a CAN protocol controller and the physical bus. The MCP2551 has differential transmit and receive capability for the CAN protocol controller and is fully compatible with the ISO 11898 standard, including 24V requirements. It will also operate at speeds of up to 1 Mbits/sec.

This serial communications protocol supports distributed real-time control with a sophisticated level of security. The CANbus time-proven performance ensures predictable error-free communications for safety conscious application environments. It is able, through arbitration, to prioritize messages. The configuration is flexible at the hardware, as well as the data link layer, where many of the transmission details can be modified by the designer. This is done, while at the same time there is system-wide data consistency.

Recommended References

AN212 “SmartSensor® CAN Node Using the MCP2510 and PIC16F876”, Stanczyk, Mike, Microchip Technology Inc.

AN228 “A Physical Layer Discussion”, Richards, Pat, Microchip Technology Inc.

AN754 “Understanding Microchip’s CAN Module Bit Timing”, Richards, Pat, Microchip Technology Inc.

“High-Speed CAN Transceiver”, Microchip MCP2551 product data sheet, DS21667

“Stand-Alone CAN Controller with SPI™ Interface”, Microchip MCP2515 product data sheet, DS21801

“Wireless CAN Yard Lamp Control”, Dammeyer, John, Circuit Cellar, August 2003, page 12

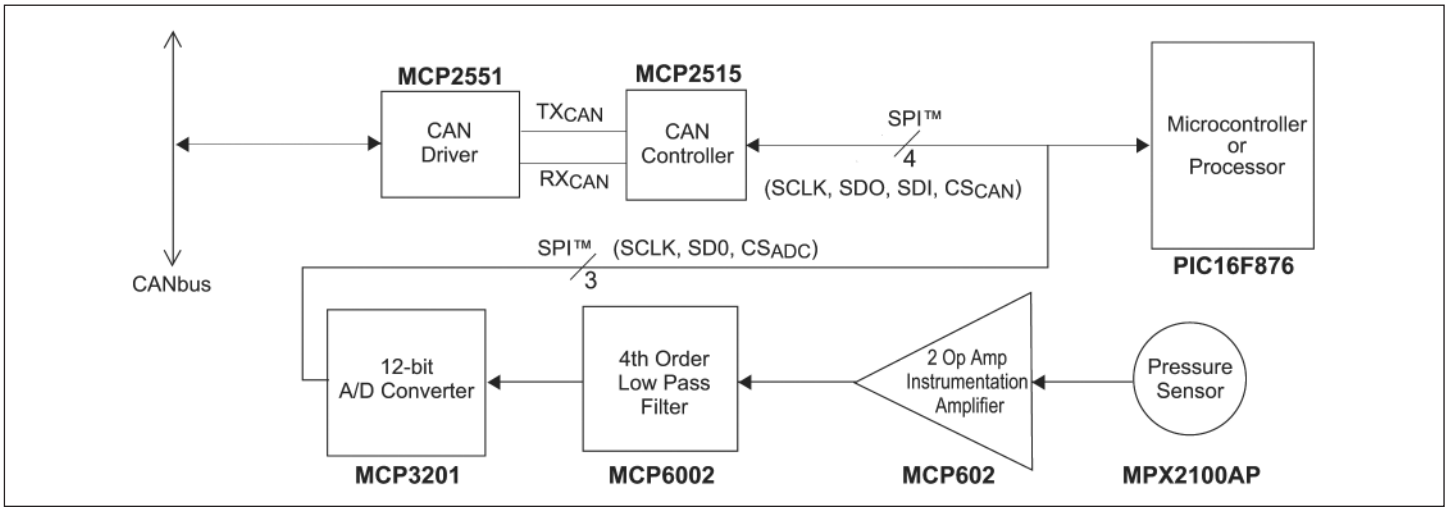


Figure 2: *This is an example of a single node for a CAN network. All of the elements for appropriate communication on the network are implemented through the CAN driver (MCP2551), CAN controller (MCP2515) and the microcontroller.*

Analog Design Notes

Notes:

Notes:

Analog Design Notes

Analog and Interface Attributes

Robustness

- MOSFET Drivers lead the industry in latch-up immunity/stability

Low Power/Low Voltage

- Op Amp family with the lowest power for a given gain bandwidth
- 600 nA/1.4V/14 kHz bandwidth Op Amps
- 1.8V charge pumps and comparators
- Lowest power 12-bit ADC in a SOT-23 package

Integration

- One of the first to market with integrated LDO with Reset and Fan Controller with temperature sensor
- PGA integrates MUX, resistive ladder, gain switches, high-performance amplifier, SPI™ interface

Space Savings

- Resets and LDOs in SC70, A/D converters in a 5-lead SOT-23 package
- CAN and IrDA® Standard protocol stack embedded in an 18-pin package

Accuracy

- Offset trimmed after packaging using non-volatile memory

Innovation

- Low pin-count embedded IrDA Standard stack, FanSense™ technology
- Select Mode™ operation

For more information, visit the Microchip web site at: www.microchip.com/analogtools

Analog and Interface Products

Thermal Management

- Temperature Sensors
- Fan Speed Controllers/ Fan Fault Detectors

Power Management

- LDO & Switching Regulators
- Charge Pump DC/DC Converters
- Power MOSFET Drivers
- PWM Controllers
- System Supervisors
- Voltage Dectectors
- Voltage References

Battery Management

- Li-Ion/Li-Polymer Battery Chargers
- Smart Battery Managers

Interface

- CAN Peripherals
- Infrared Peripherals
- LIN Transceiver
- Serial Peripherals
- Ethernet Controller

Mixed-Signal

- A/D Converter Families
- Digital Potentiometers
- D/A Converters
- V/F and F/V Converters
- Energy Measurement ICs

Linear

- Op Amps
- Programmable Gain Amplifiers
- Comparators
- Linear Integrated Devices

Worldwide Sales and Service

At Microchip, we know that it takes more than product specifications to create loyal customers. In addition to a broad product portfolio, we understand the value of a complete design solution. That's why we maintain a worldwide network of sales and support. Our global network of experienced field application engineers and technical support personnel are ready to provide product and system assistance to help you further streamline your design, prototype and production activities.

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