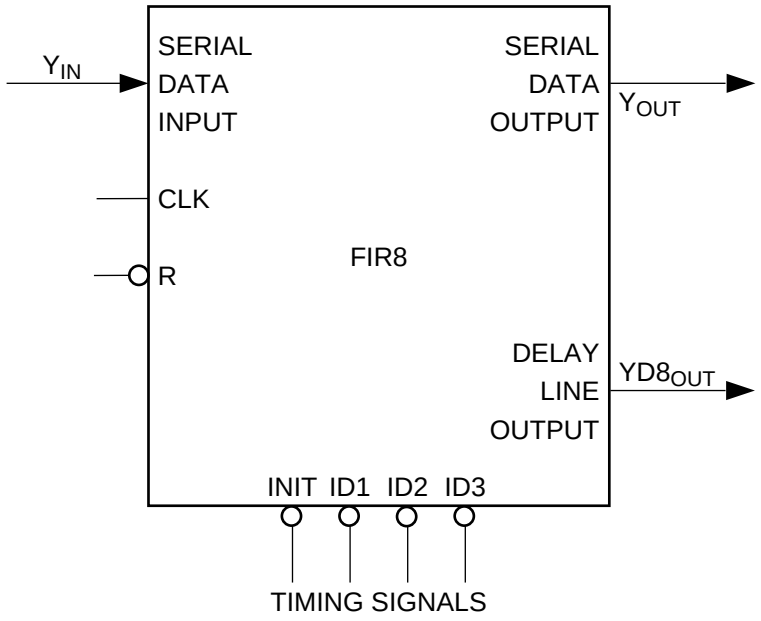
Standard 8-tap FIR Filter Macro (FIR8)



- Efficient – Digital Filter fits into smallest AT6000 Family Member (AT6002)
- Variable coefficient-type design
- Coefficient update in real-time via partial dynamic reconfiguration
- Bit-Serial Digital Signal Processing
- 5M-Samples/second – maximum sample rate

Macro Statistics for "FIR8"

Utilization Summary	Utilized
Speed (MHz)	83.3
Delay (ns)	12.0
Cells	883
Size (x * y)	34 x 53
Gates (ASIC)	3045
Power (mA/MHz) (80% duty cycle)	1.048

The 8-tap FIR Filter consists of an array of serial-parallel multipliers with coefficient storage, delay shift-registers, and the serial column adder as shown in the diagram. The coefficients are stored as constant cells in the Atmel AT6000 FPGA architecture. This provides the compact and efficient storage of a fixed-coefficient scheme but is variable in real-time through the use of Cache-Logic™ (dynamic partial reconfiguration of the FPGA). Any one or more of the coefficients can be modified by sending the appropriate bit-stream(s) to the FPGA. While the updates occur, the filter continues to operate undisturbed as does the rest of the circuitry in the array. This is another unique benefit of Atmel FPGAs.

The serial-parallel multipliers (SPM) are produced by the Component Generator, which allows specification of coefficient word-width and data representation format (signed or unsigned). The resulting SPM hard macro can be used repeatedly with identical performance. Carry-save adders (CSADDI) are used to build up the serial column adder (SCADSI), which acts as a simultaneous accumulator. Bit-serial arithmetic units layout in fine-grain FPGA architectures very efficiently. Using the cell-to-cell interconnection permits excellent device utiliza-

FPGA Digital Filter

Application Note

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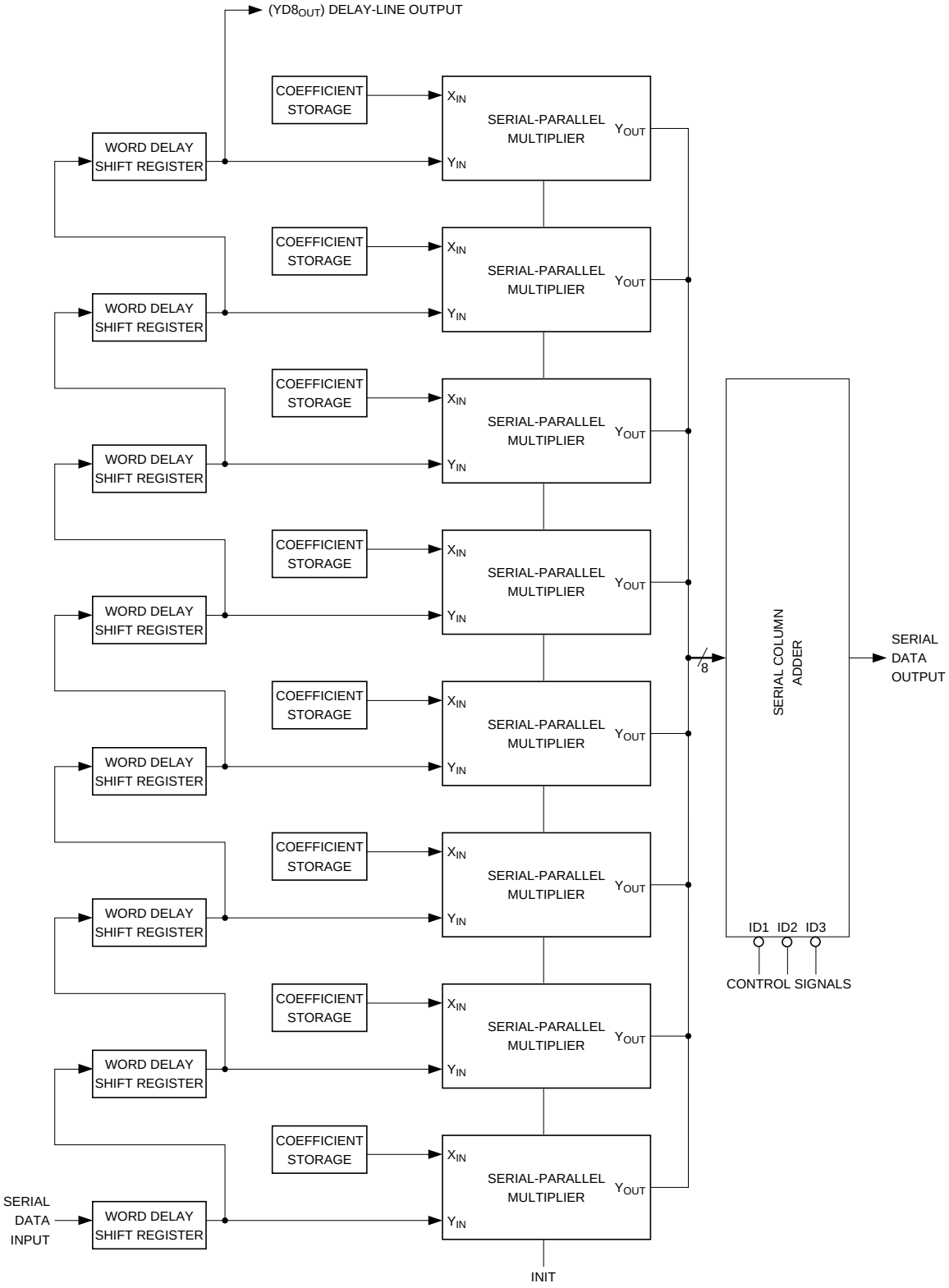
tion coupled with high-speed performance.

The balance of the FIR filter elements are the input-word delay stages that are implemented as shift-registers and the coefficient storage. The SPM and other bit-serial arithmetic functions usually have a latency of one-bit time. Delay stages compensate for this latency by providing additional bit-time delays in addition to the product delay. The total delay-storage requirements will vary depending on the filter architecture, internal precision, and output overflow requirements. In this example, we are summing the outputs from the eight taps using the SCADSI circuit. This adder tree has three levels of bit-serial adders and hence a latency of 3 bits. Therefore, the total delay word-length requirement is 20 bits, 16 for the product length, 1 for the SPM, and 3 for the SCADSI, allowing ample precision for summation overflow. The shift registers and constants are specified to the Component Generator and the macros are created in minutes.

Control of the filter is achieved by generating an initialization signal at each new sample time. This single clock-cycle wide pulse is delivered to the filter as the LSB of each sample is presented to the multipliers. This signal insures that the carry signals are reset at the beginning of each process cycle. Delayed versions of this signal are input to the serial column adder, initializing each carry-save adder in the adder tree.

QuickChange

In support of the CacheLogic capability, Atmel has developed QuickChange™, a multi-parameter specification software tool that allows the designer to interactively specify multiple parameters for digital filters, convolvers, and other compute-oriented hardware. After completing the design with an initial set of parameters, the designer simply invokes QuickChange from the Atmel design environment. QuickChange searches the design for filter coefficients or other parameters, logically groups them and displays them in a graphical user-interface. The designer can then specify as many replacement sets of parameters as desired. The QuickChange tool then generates the FPGA bit-streams for each new parameter or sets of parameters. These small bitstream files, called “windowed” bit-streams, partially reconfigure the FPGA without affecting the operation of existing logic.


(YD8OUT) DELAY-LINE OUTPUT
COEFFICIENT STORAGE
WORD DELAY SHIFT REGISTER
XIN
YIN
SERIAL-PARALLEL MULTIPLIER
YOUT
8
SERIAL COLUMN ADDER
SERIAL DATA OUTPUT
ID1 ID2 ID3
CONTROL SIGNALS
SERIAL DATA INPUT
INIT