ANTC204

SY88149NDL and SY88349NDL Burst Mode Limiting Post Amplifiers

Introduction

This document explains how to use the SY88149NDL and SY88349NDL burst mode limiting amplifiers in different applications including 1G/10GEPON, XGPON.1, GE-PON/GPON, Gigabit Ethernet, Fibre Channel, OC-3/12/24 SONET/SDH, and OBSAI/CPRI.

The SY88149NDL (resp. SY88349NDL) is a high-sensitivity limiting post amplifier that can amplify signals as small as $5mV_{PP}$ with data rates up to 1.25Gbps (resp. 2.5Gbps). The parts offer LOS or SD outputs depending on the LOS/SD SEL option. The LOS/SD output can be fed back to the JAM input for output stability when there is no data present at the input. LOS/SDLVL sets the threshold for the input signal detection.

Both amplifiers offer a fast SD assert (LOS de-assert) time of 5ns and a fast SD de-assert (LOS assert) time of 5ns if manual RESET is used or 120ns if /AUTORESET is used.

Noise Discriminator

The noise discriminator feature is intended for PON OLT applications with high-gain burst-mode TIAs where noise can trigger a false LOS de-assert or SD assert while no input data is present. The noise discriminator will filter input data through a series of specialized circuits that will only trigger LOS/SD on the rising edge of a valid PON 1.244Gbps (resp. 2.488Gbps) preamble bit stream (10101). The SY88149NDL (resp. SY88349NDL) noise discriminator is designed to accept a 1.244Gbps ±300Mbps (resp. 2.488Gbps ±300Mbps) preamble burst. Any other bit pattern will be rejected. If this part is used at any other data rate, the noise discriminator should be disabled.

The noise discriminator, implemented in the edge detector circuit, can be selected or bypassed by selecting the proper resistor value using the settings at the LOS/SDSEL pin, as shown in the table below.

Table 1. Truth Table for SD/LOS Select and Noise Discriminator function

LOS/SDSEL Pin	LOS/SD Selection	Noise Discriminator	Input To JAM	Outputs
0Ω to VCC	SD	Enabled	HIGH	Enabled
0Ω to VCC	SD	Enabled	LOW	Disabled
16kΩ to VCC	SD	Disabled	HIGH	Enabled
16kΩ to VCC	SD	Disabled	LOW	Disabled
16kΩ to GND	LOS	Disabled	HIGH	Disabled
16kΩ to GND	LOS	Disabled	LOW	Enabled
0Ω to GND	LOS	Enabled	HIGH	Disabled
0Ω to GND	LOS	Enabled	LOW	Enabled

RESET vs. /AUTORESET Operation in Burst Mode Applications

The user can chose to de-assert SD (assert LOS) using either /AUTORESET mode or manual RESET. In /AUTORESET mode, the SD de-asserts (LOS asserts) automatically within 120ns after the last high-to-low transition of the input data burst. If the /AUTORESET function is disabled, SD must be de-asserted (LOS asserted) manually by applying a RESET pulse at RESET pin.

AC or DC Coupling and Burst Mode Receiver Challenges

The receiver should be able to support data signals with long strings of consecutive identical bits (CID) and power shift from strong bursts to weak bursts (and vice versa) to avoid getting errors. These two situations won't be an issue if the receiver link from the photodiode–TIA (ROSA) to the limiting amplifier to the CDR is DC-coupled and doesn't contain any coupling capacitors. Unfortunately, DC-coupling the limiting amplifier to the TIA requires the output of the TIA and the input of the LA to have compatible common mode voltages, and it is unlikely to find a TIA-LA on the market that satisfies that condition. Therefore, to have more choice in parts selection, the module designer will more likely use AC coupling between the TIA and LA.

AC-coupling the TIA to the LA comes with some issues the designer should address by using better architecture and appropriate component values. The two issues that face the use of AC coupling are the presence of long strings of consecutive identical digits (CID) and receiver threshold settlement time during large power shifts between strong and weak bursts.

CID

CID is defined as consecutive identical digits and may vary from one protocol to another and may be either consecutive '1' or consecutive '0'. It is up to the module designer to ensure that the module will correctly handle the number of CIDs for the particular application(s).

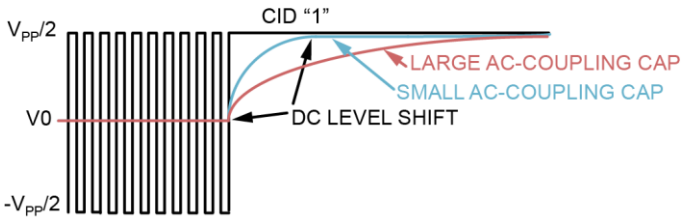

Figure 1. Effect of CID "1"

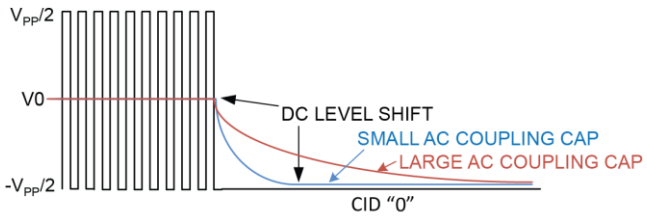

Figure 2. Effect of CID "0"

A small value coupling capacitor will create a higher low-cut-off frequency (the cap and the termination creates a high-pass filter) that may cause errors with low-frequency data, especially in the presence of long strings of CID. Additionally, this condition makes the middle of the data eye wander with low-frequency data components. Therefore, the value of the cap should be large enough to set the low frequency cut-off well below the lowest frequency component (created by CID) and minimize DC level wander with low-frequency components.

Receiver Threshold Settling Time in Burst Mode Applications

As can be seen in Figure 3, when the data at the input of the receiver switches from a strong burst to a weak burst, the DC components of the data signal decays exponentially with time. If a large value is selected for the coupling cap, the data's DC level may not settle to the baseline within allowed deviation during the preamble time and will lead to errors in data detection. In other words, the time constant created by the coupling cap should be small enough to make the receiver threshold settlement transparent to strong burst-weak burst transitions.

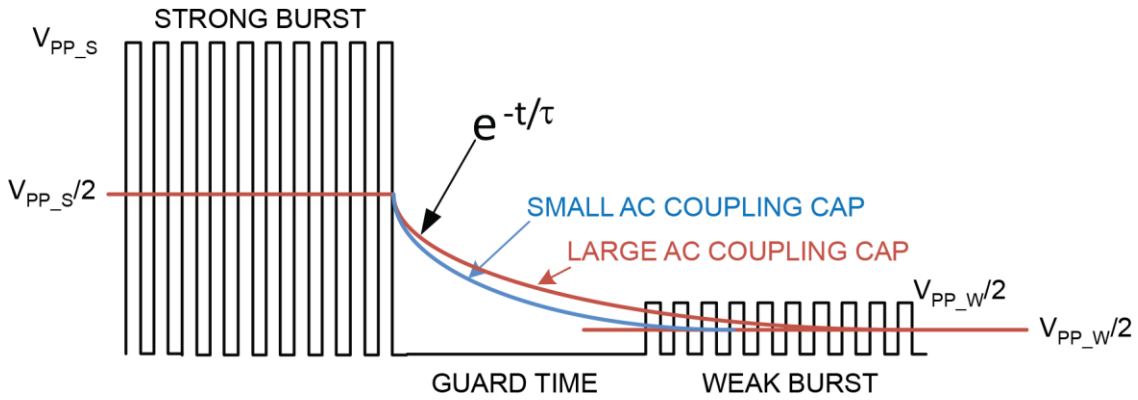

Figure 3. Effect of strong burst-weak burst transition

CID and Receiver Threshold Settling Time Solution

To improve the receiver threshold settlement time, which requires a short time constant, and the CID problem, which requires a long time constant, the circuit can be designed with two low-frequency cut-off frequencies: one low enough to be used for CID and one high enough to improve the receiver's settlement time between bursts. The circuit in Figure 4 below can be used to achieve that.

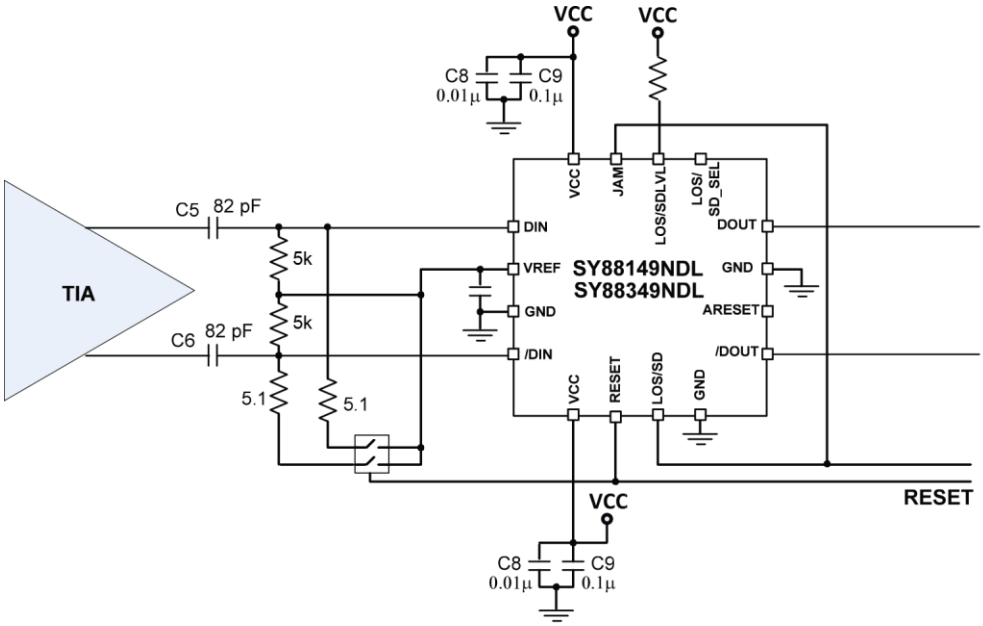

Figure 4. Solution based on two time constants

The output of the TIA is coupled to the input of the LA with a small cap (C5=C6=82pF). The termination at the input of the limiting amplifier is switched between a low value (5.1Ω) during guard time between the two bursts and part of the preamble of the second burst, and then switched to a higher value of a few kilo-ohms (5kΩ in Figure 4). The lower value allows for a fast threshold acquisition while the higher value allows for a smaller threshold droop during CID.

The corresponding two cut-off frequencies are:

- Lower low frequency cut-off = 2.4MHz, selected when RESET=LOW to support CID.
- Higher low frequency cut-off = 2.4GHz, selected when RESET=HIGH to allow the receiver to settle during preamble.

The selection between the two termination resistors, which determines the two low-frequency cut-offs, is done by applying a RESET signal that closes the switches when it's high. The RESET signal should start during the guard time and end either during the guard time or after a few bits of the second burst preamble, as shown in Figure 6 and Figure 9. This allows for a fast ONU#2 threshold acquisition (short time constant selected when RESET applied) and minimizes the threshold droop during CID and guard time when RESET is LOW (longer constant time selected).

The RESET will also reset the noise discriminator circuitry in the SY88149NDL (resp. SY88349NDL) to get ready for data detection after the end of the RESET.

Effect of RESET Signal on SD/LOS Timing

Noise Discriminator (ND) Disabled

If the noise discriminator (ND) is disabled and the RESET signal is applied during the guard time between the two ONUs data and ends before the preamble of the ONU#2, as shown in Figure 5, there will be no impact on SD or LOS assert or de-assert time. However, the threshold acquisition time won't be the fastest because the DC level will first settle to VREF and then to the ONU#2 data threshold during the preamble.

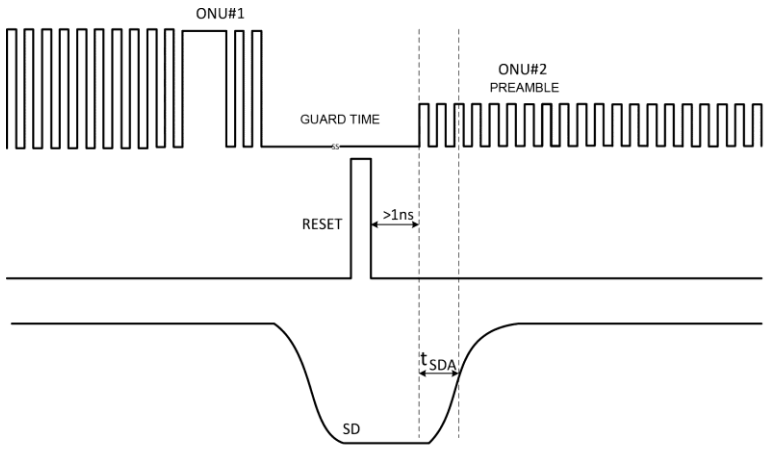

Figure 5. RESET ends before preamble with ND disabled

To improve the threshold acquisition and receiver settlement time between two bursts, the RESET can be applied during the guard time and ends during the preamble of ONU#2, as shown in Figure 6. Keeping the RESET during a few bits of the preamble will allow for a fast acquisition of the ONU#2 data threshold using the shorter time constant.

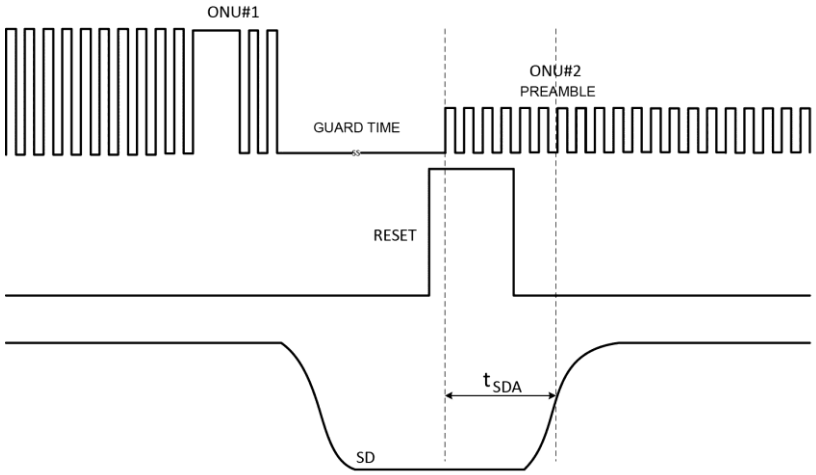

Figure 6. RESET ends during preamble with ND disabled

This improvement comes at the price of a delay in the SD assert (LOS de-assert) because the data is not detected during the bits of the preamble overlapped by the RESET signal. To minimize that delay, the overlap between RESET and the preamble should be kept to the minimum that eliminates or minimizes the droop in the data DC component.

If the RESET is applied during the preamble or DATA, as shown in Figure 7, SD (or LOS) will generate a glitch before stabilizing. SD asserts high during the first bits of the preamble, then de-asserts low with RESET to assert high again during the preamble or during the data bits following the end of RESET.

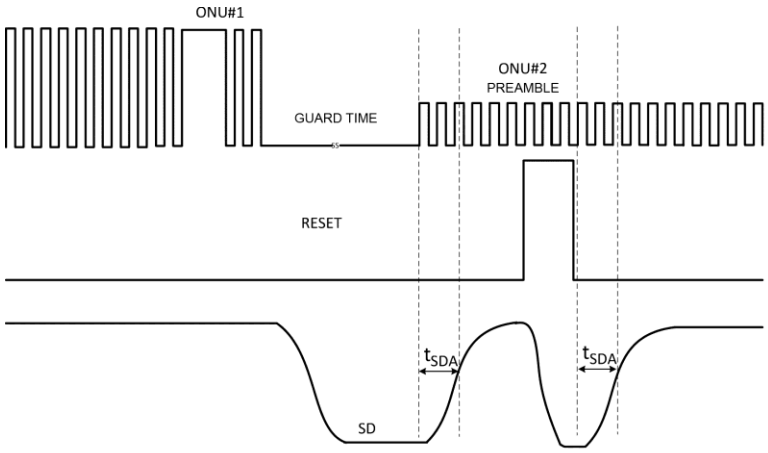

Figure 7. RESET applied during preamble or data with ND disabled

Noise Discriminator Enabled

Please note that to initialize the ND circuitry, a RESET pulse must be applied after power ON.

If the noise discriminator is enabled and the RESET is applied during the guard time and ends before the preamble of ONU#2, as shown in Figure 8, the SD assert time will be the combination of the noise discriminator data detection time (4 bits) and the delay between data detection and SD asserting high.

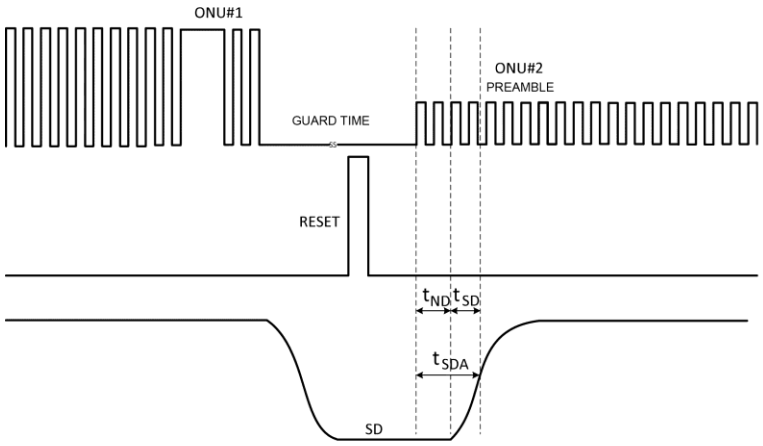

Figure 8. RESET ends before preamble with ND enabled

If the noise discriminator is enabled, and the RESET is applied during the guard time and ends during the preamble of ONU#2 (Figure 9), the SD assert time will be the combination of the delay from the start of the preamble to the first bit "1" following the end of RESET, the noise discriminator data detection time (4 bits), and the delay between data detection and SD assert.

CAUTION:

If the RESET is applied during guard time and extends into the preamble, the SD assert delay will vary depending on where the end of the RESET signal occurs. In other words, the SD assert time won't be repetitive. Therefore, this way of applying RESET is not recommended if the shortest and stable SD assert time is required.

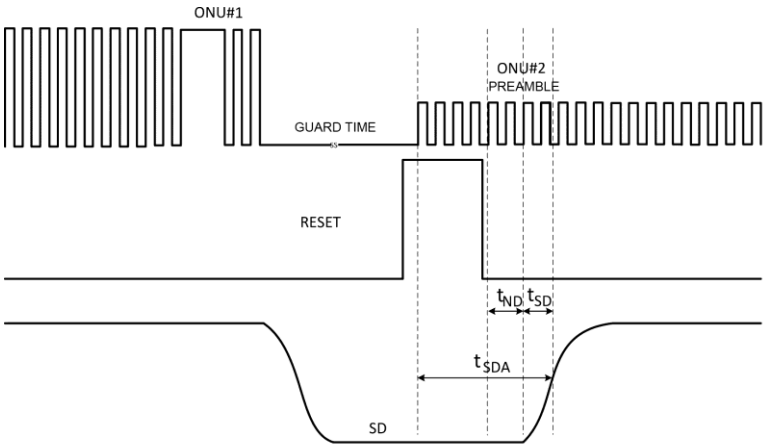

Figure 9. RESET ends during preamble and ND enabled

If the RESET is applied during the preamble or DATA, as shown in Figure 10, and ND is enabled, SD (or LOS) will generate a glitch before stabilizing. SD asserts high during the first bits of the preamble, then de-asserts low with RESET to assert high again during the preamble. If RESET ends during data, SD asserts high only if the ND detects the sequence of 4 bits (1010) in the data bits following the end of RESET.

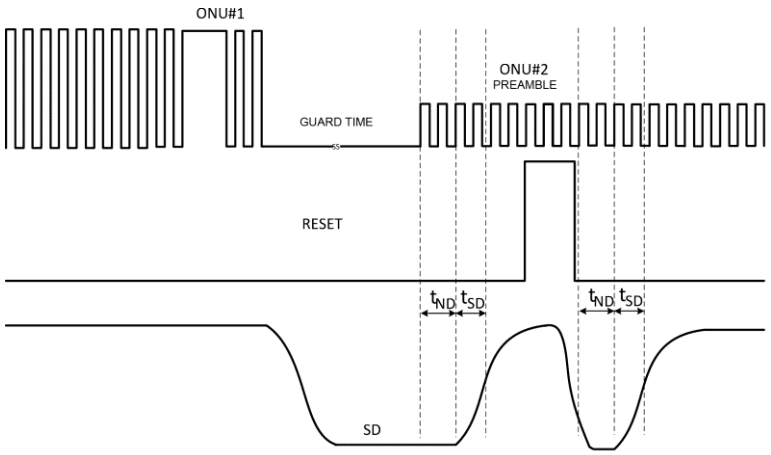

Figure 10. RESET applied during preamble or data with ND enabled

Continuous Mode Applications

For continuous mode applications, the SY88149NDL and SY88349NDL limiting amplifiers can be used as typical continuous mode LA, AC, or DC (assuming common mode voltage levels are the same) coupled to the TIA. To preserve the fast SD/LOS fast assert/de-assert time, the coupling capacitors' values should be kept to the smallest that can support CID for the application.

MICREL, INC. 2180 FORTUNE DRIVE SAN JOSE, CA 95131 USA
TEL +1 (408) 944-0800 FAX +1 (408) 474-1000 WEB http://www.micrel.com