AN1311

Single Cell Input Boost Converter Design

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INTRODUCTION

Currently, many portable battery-powered applications use multiple cell batteries for power. In some cases, the product form factor is driven by the size of the battery pack.

This application note introduces and details design equations and trade-offs that facilitate the use of single cell input synchronous boost converters from the Microchip MCP1640/B/C/D family of devices.

These single cell input boost converters enable startup from very low input voltage sources. The MCP1640/B/C/D converters will start from a 0.65 V source and operate down to 0.35 V, while boosting the output voltage from 2.0 V to 5.5 V. Two typical application schematics are shown in Figure 1. Efficiency is maximized over the entire load range by auto switching from a Pulse Skipping, or Pulse Frequency Modulation (PFM) mode to a continuous 500 kHz Fixed Frequency mode by using MCP1640/MCP1640C devices. For applications that cannot tolerate the low frequency Pulse Skipping mode or the output ripple voltage associated with it, the MCP1640B/D devices switch at a continuous fixed pulse width modulation frequency of 500 kHz. In addition to dual switching modes, the MCP1640/B/C/D family of devices offers two disable options. In the True Output Disconnect option (MCP1640/MCP1640B devices), the output of the synchronous boost converter is open and the typical diode path from input to output is removed, isolating the input from the output. In the Input Bypass option (MCP1640C/D devices), the input is connected to the output using the synchronous P-Channel switch. During this mode, the quiescent current draw from the battery is less than 1 µA typical. The Input Bypass mode provides voltage to power a load in deep sleep with the ability to boost the voltage up to the levels that are necessary for normal operation.

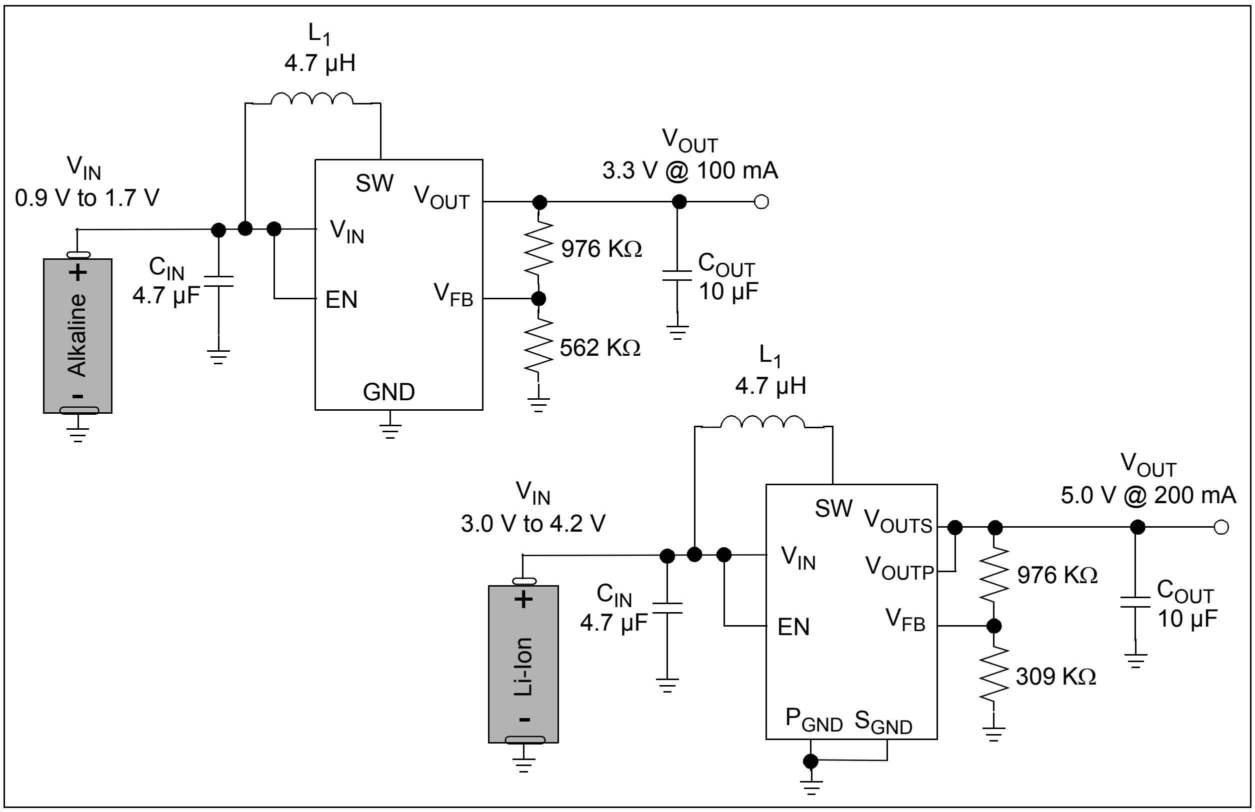

FIGURE 1: *Typical MCP1640 Applications.*

BOOST CONVERTER ANALYSIS

Boost Converter Operation

The Inductive Switch mode boost power converter is used to step up a lower voltage to a higher voltage. The boost topology requires an inductor, switch, diode, and output capacitor. To analyze the operation of a boost converter, it is assumed that the output voltage ripple is low or DC. In practice this assumption is normally valid for DC-DC converters.

However, in many boost converters, the DC current flows from input to output through an inductor L_1 and a diode. And, in typical applications, when the boost converter is turned off, this can drain the battery.

In MCP1640/B/C/D devices, the diode is replaced with a P-Channel MOSFET that acts like a diode, i.e., it turns on to forward current from input to output and turns off to block reverse current from output to input. An internal switch blocks the forward diode path of the P-Channel while the converter is disabled. Figure 2 represents the basic components of a synchronous boost regulator.

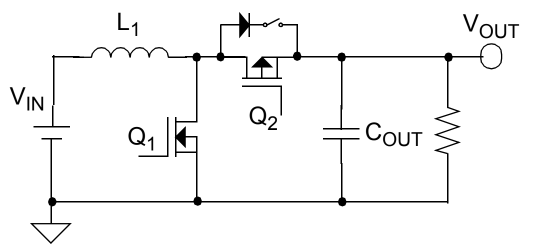

FIGURE 2: *Boost Converter Topology.*

SWITCH CLOSED

At the beginning of the cycle, switch Q_1 is turned ON. During this time, the output current is supplied by the output capacitor C_{OUT}, and magnetic field energy is stored in inductor L_1. With Q_1 ON, the inductor current ramps up at a constant rate of V_{IN} (Input Voltage) divided by the inductance of L_1. The diagram in Figure 3 represents the Switch Closed state.

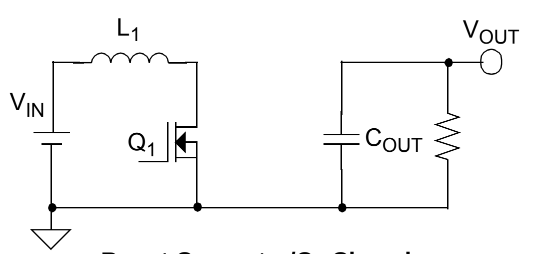

FIGURE 3: *Switch Q_1 ON.*

SWITCH OPEN

At the end of the Pulse Width Modulation (PWM) cycle, the boost switch Q_1 turns off. The inductor current must—and will—continue to flow, finding a path through Q_2. This current now supports the load, in addition to replenishing the current removed from C_{OUT} during the switch ON time. The diagram in Figure 4 represents the Switch Open state.

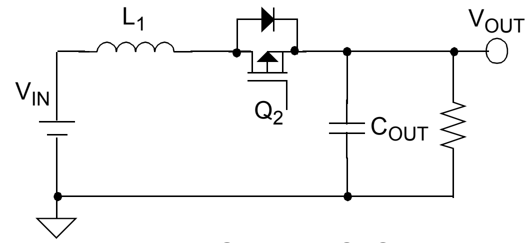

FIGURE 4: *Switch Q_1 OFF.*

For steady state operation, the energy that is removed from C_{OUT} during the switch ON time must be replaced with exactly the same amount of energy during the switch OFF time. In addition to the charge-time balance on the output capacitor C_{OUT}, the inductor current ramp during the switch ON time must be exactly equal to the inductor current ramp during the switch OFF time to achieve steady state PWM switching. For steady state operation, the applied volt-time on the inductor must be balanced or equal in magnitude, and opposite in direction, for the switch ON and OFF time. This forms the basis for our first equation:

EQUATION 1: INDUCTOR VOLT-TIME BALANCE

$$V_{IN} \times t_{on} = (V_{OUT} - V_{IN}) \times t_{off}$$

Using the inductor volt-time balance and replacing the switch ON time with duty cycle D, and the switch OFF time with 1-D, the inductor volt-time balance can be used to derive the switch duty cycle D.

EQUATION 2: DUTY CYCLE BALANCE

$$D = (V_{OUT} - V_{IN}) / V_{OUT}$$

Inductor Current Operating Modes

CONTINUOUS INDUCTOR CURRENT MODE

In the previous derivation, there are two inductor volt-time states.

- State 1: V_{IN} is applied across L_1.
- State 2: V_{OUT}-V_{IN} is applied across L_1.

For steady state operation, current must be flowing in L_1 at all times.

However, as the boost output current lowers, another state is entered. In this third state, the inductor current reaches zero. This adds another term to the volt-time balance equation.

Figure 5 represents Continuous Inductor Current mode.

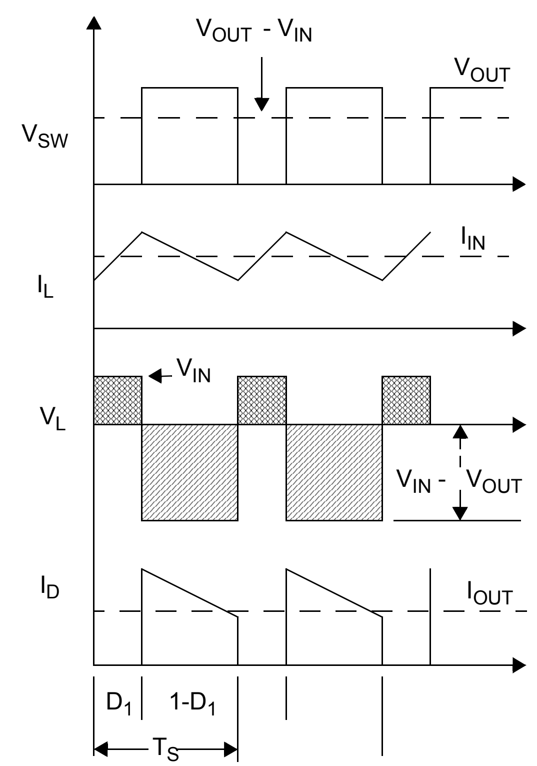

FIGURE 5: Continuous Inductor Current Waveforms.

DISCONTINUOUS INDUCTOR CURRENT MODE

During Discontinuous Inductor Current mode, the inductor current reaches zero prior to the end of the cycle. This operating mode does not impact the regulation of the boost converter.

Discontinuous mode is entered when the output power (V_{OUT} * I_{OUT}) is less than the amount of energy stored in the inductor multiplied by the switching frequency ($(1/2*L*I_{LPK}^2)*F_{SW}$). As the load is reduced, the inductor current will eventually reach 0A. If the load is further reduced, the duty cycle must also be reduced to prevent overcharging the output capacitor or losing voltage regulation.

To derive the duty cycle equation for Discontinuous mode, the same procedure (that was used for Continuous mode) applies. In the Discontinuous equation, there are three states, versus the two for Continuous mode.

- State 1: switch is ON, the current is ramping in the inductor, and the voltage applied is +V_{IN}.
- State 2: switch is OFF, the current is ramping down, and inductor voltage is -(V_{OUT}-V_{IN})
- State 3: switch is OFF, the inductor current has reached zero, and the inductor voltage is zero.

By adding the third state the duty cycle solution becomes more difficult; but it is solvable, through the use of two equations.

Since the inductor current ramp up must be equal to the inductor current ramp down (see Figure 6), the following relationship can be derived:

EQUATION 3: INDUCTOR CURRENT BALANCE

$$V_{OUT} = V_{IN} \times \frac{(D1 + D2)}{D2}$$

Figure 6 represents Discontinuous Inductor Current mode.

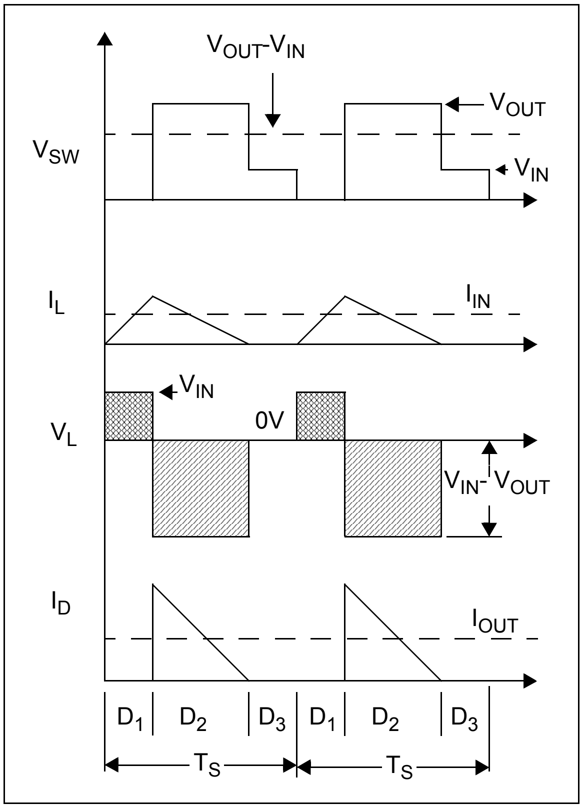

FIGURE 6: Discontinuous Inductor Current Waveforms.

For DC-DC converter analysis, the output energy is equal to the input energy, assuming efficiency is 100%. Using this relationship, the following equation can be written to determine the output current. The output current is equal to the average inductor current during the switch off time.

EQUATION 4:

$$I_{OUT} = \frac{1}{T_S} \times \left(\frac{1}{2} \times I_{LPK} \times D2 \times T_S\right)$$

Substitute V_{IN}/L* T_{ON} for I_{LPK} to simplify.

EQUATION 5:

$$I_{OUT} = \frac{1}{2} \times \left(\frac{V_{IN}}{L} \times D1 \times T_S \times D2\right)$$

The derivation is reduced to two equations and two unknowns. Solving each equation for D2 and setting them equal to each other results in the following solution, after substituting V_{OUT}/R for I_{OUT}.

Solving for V_{OUT} results in two solutions. Disregarding the imaginary solution, and substituting V_{OUT} and V_{IN} back into the previous D2 equations, and solving for D1, results in the following discontinuous duty cycle equation:

EQUATION 6: DISCONTINUOUS DUTY CYCLE

$$D1 = \frac{1}{R_{LOAD} \times T_s} \times \frac{(2 \times R_{LOAD} \times T_s \times V_{OUT} \times L \times (V_{OUT} - V_{IN}))^{1/2}}{V_{IN}}$$

CONTINUOUS VS. DISCONTINUOUS BOUNDARY

When the inductor current reaches zero at the same time the switch turns back on, it is defined as the boundary between continuous and discontinuous inductor current. To calculate the load for this boundary condition, use the energy stored per cycle and convert it to load current.

Pulse Frequency Modulation (PFM)

The MCP1640/MCP1640C devices can operate in a third mode, Pulse Frequency Modulation (PFM) mode. PFM mode is entered when the output current reduces below a predetermined threshold. In PFM mode, the inductor peak current is fixed at a value that is higher than required to keep the output in regulation. This pumps the output voltage up; pulsing stops when the output voltage reaches the maximum limit, and the device enters a low quiescent current state to minimize the current draw on the battery. Higher output voltage ripple is a result of the PFM mode. Figure 7 shows PFM mode waveforms versus Pulse-Width Modulation (PWM) mode waveforms for 1 mA load current.

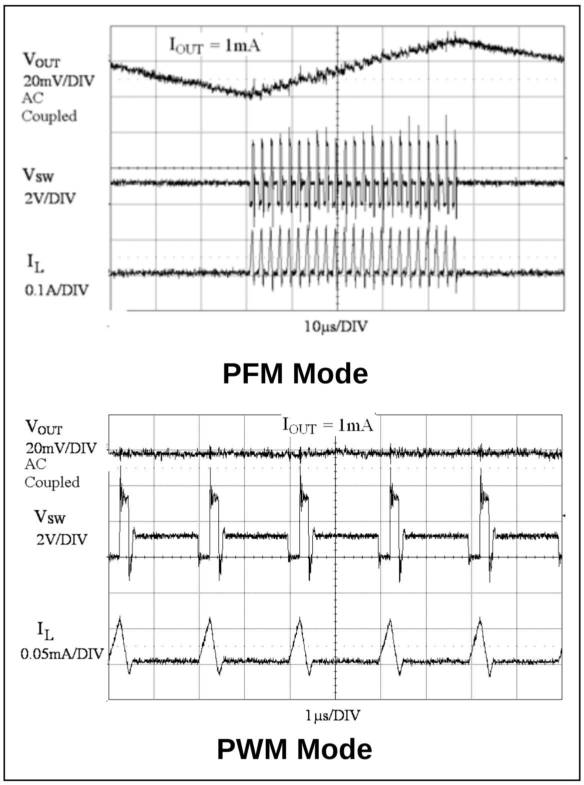

FIGURE 7: PFM Operation vs. PWM Operation.

The MCP1640B/D devices do not enter PFM mode, and the peak inductor current continues to reduce with load while the devices operate in normal Discontinuous Inductor Current mode. Compared to PFM mode, the output ripple voltage is lower and the device switches at a constant frequency of 500 kHz. This is desirable for applications that have audio or low-frequency signals. The disadvantage of not entering PFM mode is the lower efficiency. Figure 8 compares PFM/PWM mode efficiency with PWM-only mode efficiency.

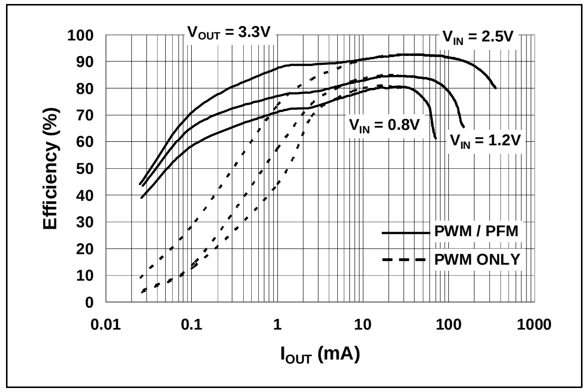

FIGURE 8: Efficiency, PFM and PWM Operating Modes.

The P-Channel Synchronous rectifier switch turns off when the inductor current reaches zero, for all devices and modes of operation. This prevents current from flowing backwards from output to input, keeping the efficiency high. For ultra light loads, pulse skipping does occur when operating in PWM-only mode. The peak current in the inductor is low, keeping the ripple voltage low. Figure 9 graphs the current at which the MCP1640B/D devices begin to skip pulses versus the input voltage.

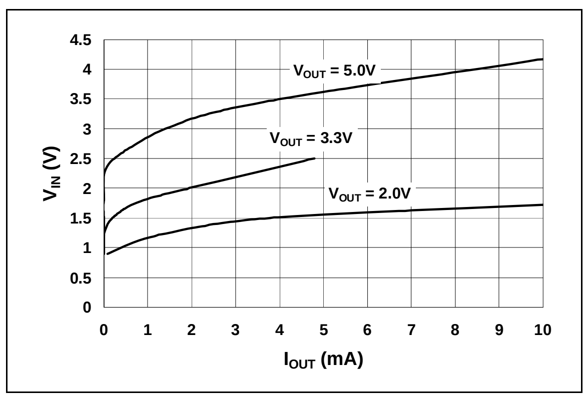

FIGURE 9: Pulse Skipping Threshold Voltage vs. Load Current.

Peak Current Mode Control

The MCP1640/B/C/D family of devices uses peak current mode control. This control method reduces the order of the power system to one versus two, when compared to voltage mode control. The device block diagram is represented in Figure 10.

Peak current mode control compares the peak switch (or inductor current) with the output of the error amplifier. As the load demands change, the error amplifier (with integrated compensation) changes to set the proper peak current for voltage regulation.

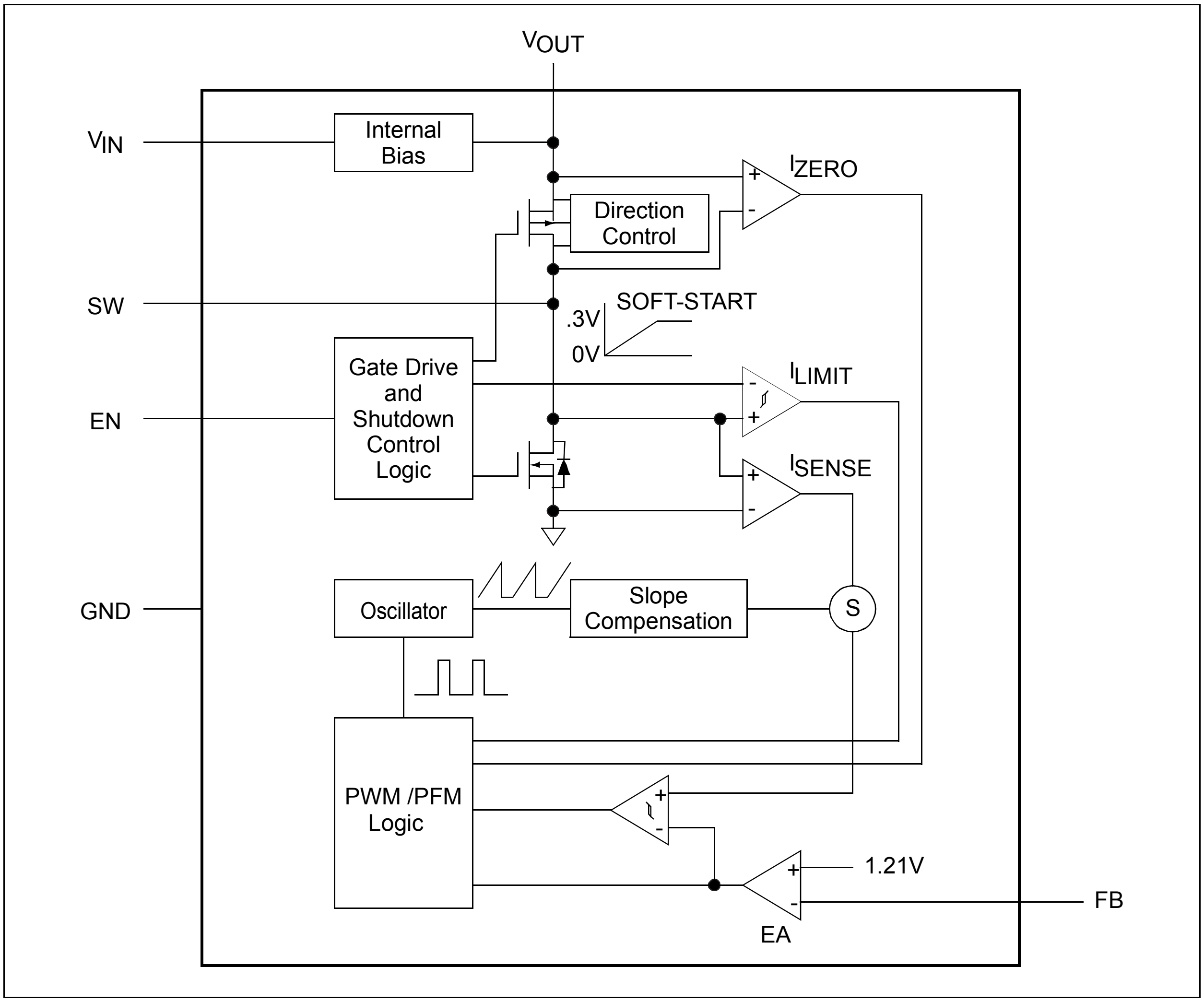

FIGURE 10: *Peak Current Mode Control.*

For sudden changes in load, the peak current mode control provides a fast response. The response is a function of the inductor value and the output capacitor value. Since the compensation for the MCP1640/B/C/D family is integrated, there are limits on the range of inductance and output capacitance that can be used. For peak current mode control, applications that operate with over 50% duty cycle, slope compensation is necessary to maintain stability. Slope compensation is added to the current sense signal internally to the device. This also limits the variation in inductance that can be used. A peak current limit is set by limiting the height of the sensed switch current to a safe value. The MCP1640/B/C/D family of devices limits the peak current to 850 mA typically.

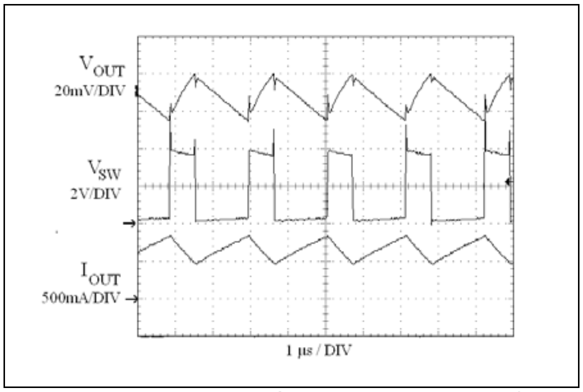

FIGURE 11: *Inductor Current Waveform, 850 mA Peak Limit.*

The range of the boost inductor and minimum output capacitor are limited. Table 1 provides some guidance for how much variation can be used. In most cases, a 4.7 µH inductor and 10 µF capacitor are recommended for boost inductance and output capacitance.

Input capacitance should be a minimum of 4.7 µF. Additional capacitance should be added for applications that are located far from the battery, or source, and have high source impedance. For low input voltage and high output current applications, 10 µF is recommended.

For very low load applications, smaller output capacitors can be used. The value depends on the input voltage, output voltage, and output current.

TABLE 1: LIMITS ON BOOST INDUCTANCE AND OUTPUT CAPACITANCE

V_{OUT}	L_{MIN}	L_{MAX}	C_{MIN}
2.0 V	2.2 µH	4.7 µH	10 µF
3.3 V	4.7 µH	10 µH	10 µF
5.0 V	4.7 µH	15 µH	10 µF

EFFICIENCY AND PERFORMANCE

Converter efficiency is highly dependent on the input and output voltage, and current conditions. The dominant loss for the MCP1640/B/C/D family is resistance, so lower input/output voltage efficiency is lower in efficiency than higher input/output voltage applications. Other factors that can impact efficiency are the losses in the inductor and capacitor, mostly the resistive losses of the inductor. Larger inductors result in lower resistance and higher efficiency, the trade-off being size and cost.

QUIESCENT CURRENT, LEAKAGE CURRENT AND HOW IT RELATES TO BATTERY LIFE

The MCP1640/B/C/D family of devices operate with very low quiescent current (I_Q). The typical I_Q for the devices, while operating in PFM mode, is 19 µA. For applications that have a low Sleep mode current, this can result in substantial average battery current. For some multi-cell or coin cell applications, a Bypass mode that uses the integrated P-Channel MOSFET to connect the input to the output can be used to provide bias power to the load. When regulated voltage is needed, the EN input pin is pulled high and the output is regulated to the desired voltage. In Shutdown mode, the bypass current consumption is less than 1 µA, extending battery life. The output true-disconnect option isolates the input from the output by reversing the integrated P-Channel MOSFET body diode. In Shutdown mode, the output voltage is 0V and the typical I_Q is less than 1 µA.

APPLICATIONS AND CONSIDERATIONS

Low Voltage Startup

The MCP1640/B/C/D family of devices is capable of starting with a very low input voltage with a load applied. The low voltage startup begins with the P-Channel MOSFET turning on to charge the output voltage up to the input voltage. Once the output voltage is charged, the N-Channel begins to switch, pumping the output voltage up to approximately 1.6 V. At this voltage, the internal bias switches from the input to the output. Typically the device can start with 0.65 V applied to the input. Typical startup waveforms are shown in Figure 12.

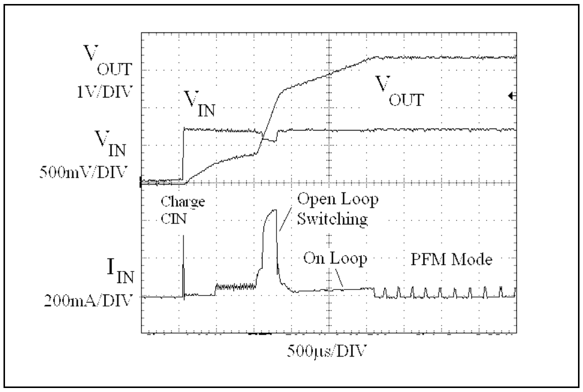

FIGURE 12: Low Voltage Startup.

Low Input Voltage High Output Current Operation

While operating at low input voltage and high output current, the input current of a MCP1640/B/C/D device can reach its peak limit. The peak current is typically limited to 850 mA, but can be as low as 600 mA. The peak input current can be estimated by calculating the output power (V_{OUT} * I_{OUT}), dividing the product (output power) by the input voltage, and dividing the quotient by the estimated efficiency. The final result is the average input current.

High Duty Cycle Operation

While operating at low input voltage and high output voltage, the duty cycle of MCP1640/B/C/D devices can approach the maximum limit of 91% typical. For example, when operating at 0.9 V with a 5.0 V output, the calculated duty cycle $((V_{OUT}-V_{IN})/V_{OUT})$ = 82%. When taking efficiency into account, the actual duty cycle can approach 90%. This results in some PWM jitter and even loss of output voltage regulation. A maximum duty cycle limit is necessary for any boost converter; practical limits from 90% to 92% allow for high step up ratios.

4.7 µF Output Capacitors

Though 10 µF of output capacitance is recommended for most applications, 4.7 µF ceramic output capacitors can be used under certain restrictions. Converter stability and output voltage ripple will be affected by the reduction of output capacitance.

STABILITY USING 4.7 µF OUTPUT CAPACITORS

The MCP1640/B/C/D family of devices has peak current mode control with internal compensation and adaptive slope compensation to match the inductor down-slope. For 4.7 µH inductors and 10 µF capacitors, the devices offer high phase and gain margin over the entire input voltage, output voltage, and output current operating range.

Figure 13 shows that the converter 0dB cross-over frequency is approximately 15 kHz with 60 degrees of phase margin and 15 dB of gain margin.

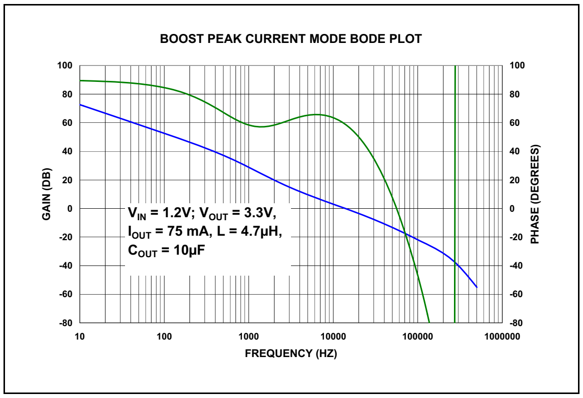

FIGURE 13: *Bode Plot 4.7 µH, 10 µF Output Capacitor Continuous Current Mode.*

Figure 14 shows the system bode plot for the same conditions as Figure 13, with the output capacitor changed to 4.7 µF.

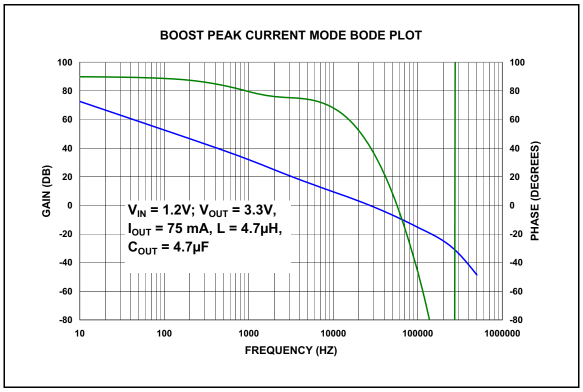

FIGURE 14: *Bode Plot 4.7 µH, 4.7 µF Output Capacitor Continuous Current Mode.*

When using a 4.7 µF output capacitor, the 0 dB cross-over is pushed out to almost 30 kHz, providing a faster responding system. However, the phase margin is reduced to less than 40 degrees and the gain margin to approximately 10 dB. A phase margin of 40 degrees is considered marginal for stability; as the input voltage changes, the phase margin will continue to decrease to the point of instability. An unstable converter results in a low frequency AC content to the output ripple that can be in the audible frequency range.

While operating in Discontinuous Inductor Current mode, the converter stability is changed, and the order of the system is reduced by one, resulting in an increase in phase margin. A bode plot of the converter while operating in Discontinuous mode is shown in Figure 15. The 0 dB crossover is approximately 28 kHz, the phase margin is approximately 60 degrees and the gain margin is high—greater than 20 dB. As shown, the converter is stable while operating in the Discontinuous mode.

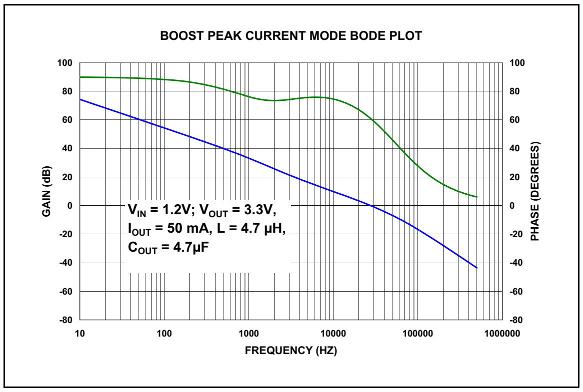

FIGURE 15: *Bode Plot 4.7 µH, 4.7 µF Output Capacitor Discontinuous Current Mode.*

In summary, to reduce the output capacitor to 4.7 µF, the converter must be operating in Discontinuous Inductor Current mode, which limits the maximum output current. Table 2 can be used as a guide:

TABLE 2: MAX I_{OUT} FOR DISCONTINUOUS MODE

	2.0 V	**3.3 V**	**5.0 V**
1 Cell Input V_{IN} = 0.9 V to 1.6 V	I_{OUT}< 25 mA	I_{OUT}< 35 mA	I_{OUT}< 50 mA
2 Cell Input V_{IN} = 1.8 V to 3.2 V		I_{OUT}< 15 mA	I_{OUT}< 80 mA
3.3 V Input			I_{OUT}< 150 mA

Sub 2V Output Applications

The MCP1640/B/C/D family of devices operates from an internal voltage that selects the maximum voltage between V_{IN} and V_{OUT}. During startup, the maximum voltage is V_{IN}, While up and running, the maximum voltage is V_{OUT}. For a single cell input, 1.8 V output applications, it is recommended that the inductor is changed from 4.7 µH to 2.2 µH and the output capacitor is changed to 20 µF. For single cell inputs, the output current range for 1.8 V V_{OUT} applications is limited to 100 mA for operation down to 0.9 V. Figure 16 represents the device efficiency while operating with a 1.8 V output.

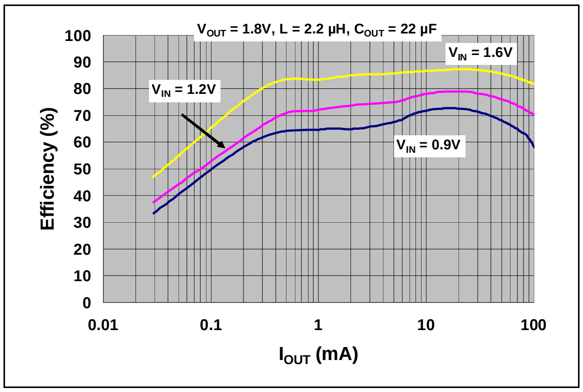

FIGURE 16: 1.8V Output Efficiency.

For 1.8 V output applications, the PFM/PWM current threshold will vary as a result of lower internal bias voltage and lower internal gate drive voltage. Figure 17 represents the PWM/PFM mode threshold current plotted versus input voltage.

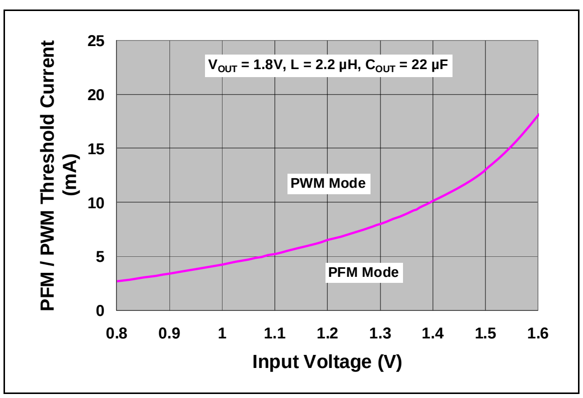

FIGURE 17: 1.8V Output PFM/PWM Threshold Current.

Due to rising threshold voltages at cold temperatures, it is recommend that the MCP1640/B/C/D minimum output voltage is 1.8 V for ambient temperatures greater than 0°C. For output currents less than 40 mA, a 3.3 µH inductor and a 10 µF output capacitor can be used when operating from a single cell alkaline input.

CONCLUSION

The MCP1640/B/C/D family of devices enables operation from a single cell input, delivers high efficiency, is small in size, and provides excellent dynamic performance. Like most DC-DC converters, the details of topology operation can be understood by balancing the volt-time on the inductor (or charge-time on the capacitor). Integrated compensation (error amplifier and slope) make stabilizing the DC-DC converter straight forward while using the standard 4.7 µH inductor and 10 µF output capacitor. Under limited output current and input voltage range, the inductor and capacitor values can be changed to further reduce solution size, cost, and operating range.

NOTES:

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