AN1278

Interleaved Power Factor Correction (IPFC) Using the dsPIC® DSC

Authors: *Vinaya Skanda and Anusheel Nahar*
Microchip Technology Inc.

INTRODUCTION

Digital power supplies are used in a wide variety of applications ranging from telecommunication power supplies and base stations to air conditioners and other home appliances. All of these applications predominantly use a Power Factor Correction (PFC) stage to improve the input power factor, voltage regulation and Total Harmonic Distortion (THD) of the input current. Without such a PFC stage, the current drawn will have significant harmonic contents due to the discontinuous currents drawn over a short duration. This, in turn, will result in increased network losses, radiated emission and total harmonic distortion. At higher power levels, these problems become more pronounced, thereby reducing overall efficiency of the system.

The standard boost converter topology is the preferred method for implementing the digital PFC. It operates the converter in Continuous Conduction Mode (CCM), thereby significantly reducing input current harmonics. The application note AN1106, *"Power Factor Correction in Power Conversion Applications Using the dsPIC® DSC"* (DS01106), describes the digital implementation of a single-stage PFC using a dsPIC® Digital Signal Controller (DSC).

This application note focuses on the design of an Interleaved Power Factor Correction (IPFC) converter. It explains the digital implementation of the IPFC on a 16-bit fixed point dsPIC DSC, containing the theoretical aspects of functioning, and MATLAB® modeling. This application note also provides hardware design guidelines and explains how to install and configure the IPFC reference board. The IPFC reference design is intended to aid the user in the rapid evaluation and development of PFC using the dsPIC DSC.

The low-cost and high-performance capabilities of the dsPIC DSC, combined with a wide variety of power electronic peripherals, such as an Analog-to-Digital Converter (ADC), Pulse-Width Modulator (PWM) and Analog Comparator, help to simplify the digital design and development of power-related applications.

Some advantages of using a digital implementation for IPFC are:

- Easy implementation of sophisticated control algorithms
- Flexible software modifications to meet specific customer needs
- Simpler integration with other applications

The controller and hardware design guidelines and techniques described here can be used to create well-formed maintainable applications. The software developed for the IPFC design is highly flexible, so it can be customized and configured to meet the needs of the specific application.

SIGNIFICANCE OF POWER FACTOR

To better understand Power Factor (PF), it is important to know that power has two components:

- Real Power
- Reactive Power

Real Power is the power that is actually consumed and registered on the electric meter at the consumers' location. It performs the actual work, such as creating heat, light and motion. Real Power is expressed in kW and is registered as kWH on an electric meter.

Reactive Power is required to maintain and sustain the Electromagnetic Field (EMF) associated with the industrial inductive loads. Reactive Power is measured in kVAR.

The total required power capacity including the real and the reactive components is known as Apparent Power, expressed in kilovolt ampere (kVA).

Power Factor is a parameter that gives the amount of real power used by any system in terms of the total apparent power. Power Factor becomes an important measurable quantity because it often results in significant economic savings. Equation 1 defines the Power Factor.

EQUATION 1:

$$Power\ Factor = \frac{Real\ Power}{Apparent\ Power}$$

When this ratio deviates from one, the input contains phase displacement and harmonic distortion or both, and either one degrades the Power Factor. Thus, the power considered as Reactive power in the system is due to two reasons:

- Phase shift of current with respect to voltage, resulting in displacement
- Harmonic content present in current, resulting in distortion

These two factors define Displacement Factor and Distortion Factor, respectively, which provide the Power Factor as shown in Equation 2.

Most power conversion applications use the PFC stage as the first stage in an AC-to-DC converter to improve the displacement and distortion factors so that minimum Apparent Power can be obtained from the supply. To reduce the losses in a power line and a power generator, minimum apparent power is absorbed from the supply, resulting in the improvement of power quality and overall efficiency of the system. The basic function of the PFC stage is to make the input current drawn from the system sinusoidal and in phase with the input voltage.

EQUATION 2: DISPLACEMENT AND DISTORTION FACTOR

Power Factor = Displacement Factor x Distortion Factor

$$PowerFactor = \underbrace{\cos\phi}_{\text{Displacement Factor}} \cdot \underbrace{\sqrt{\frac{1}{1+(I_2/I_1)^2+(I_3/I_1)^2+\ldots}}}_{\text{Distortion Factor}} = \frac{\cos\phi}{\sqrt{1+THD^2}}$$

$$THD = \sqrt{(I_2/I_1)^2+(I_3/I_1)^2+\ldots}$$

where:

$\cos\phi$ = Displacement factor of the voltage and current

THD = Total Harmonic Distortion

I_1 = Current drawn from the supply at fundamental frequency

I_2 = Current drawn from the supply at double the fundamental frequency and so on

TOPOLOGICAL CONSIDERATIONS OF TWO-PHASE IPFC

Figure 1 depicts the simplified block diagram of the two stage IPFC system and its interface with a dsPIC DSC device. This system is an AC-to-DC converter, which converts the AC input supply voltage to a regulated DC output voltage and maintains a high input PF. The IPFC converter uses two boost converters, which are parallel coupled and are 180º out of phase current controlled with respect to each other.

A dsPIC DSC device is used to implement the control algorithm. The following signals are input to the dsPIC DSC and to the control algorithm (see Figure 1):

- Rectified input voltage (V_{AC})
- Rectified input current (I_{AC})
- DC bus voltage (V_{DC})
- MOSFET1 current (I_{m1})
- MOSFET2 current (I_{m2})

The dsPIC DSC generates two PWM pulses: PWM1 and PWM2, which control the two IPFC converters. The two individual converter switch currents (I_{m1} and I_{m2}) are monitored to ensure equal sharing of the load between the two stages.

The first stage in the IPFC system is an input rectifier, which converts the alternating voltage at power frequency into unidirectional voltage. This rectified voltage is fed to the PFC converter circuit to produce a smooth and constant DC voltage to the load. The choice of the control system depends upon the type of the PFC converter used.

To determine the type of PFC converter to be used, the three basic topologies are compared: buck, boost, and buck-boost (see Figure 2). Table 1 shows the feature differences among these three topologies. On comparing the different topologies, the boost converter topology is selected because it offers the following major features:

- Continuous Conduction mode operation
- No crossover distortions
- Positive output voltage polarity
- Output voltage is higher than the input voltage
- Lower cost

Boost Topology

A boost topology PFC converter boosts the input voltage and shapes the inductor current similar to that of the rectified AC voltage. The voltage rating of the power switch is equal to the output voltage rating of the converter. The basic boost converter circuit is shown in Figure 3.

The boost topology PFC converter can be operated in Continuous Conduction mode unlike other basic topologies, such as the buck converter or buck-boost converter. This mode reduces harmonic content in the input current. However, the operation in continuous conduction region depends on the inductor value and the amount of load on the system.

FIGURE 1: TWO-PHASE IPFC BLOCK DIAGRAM

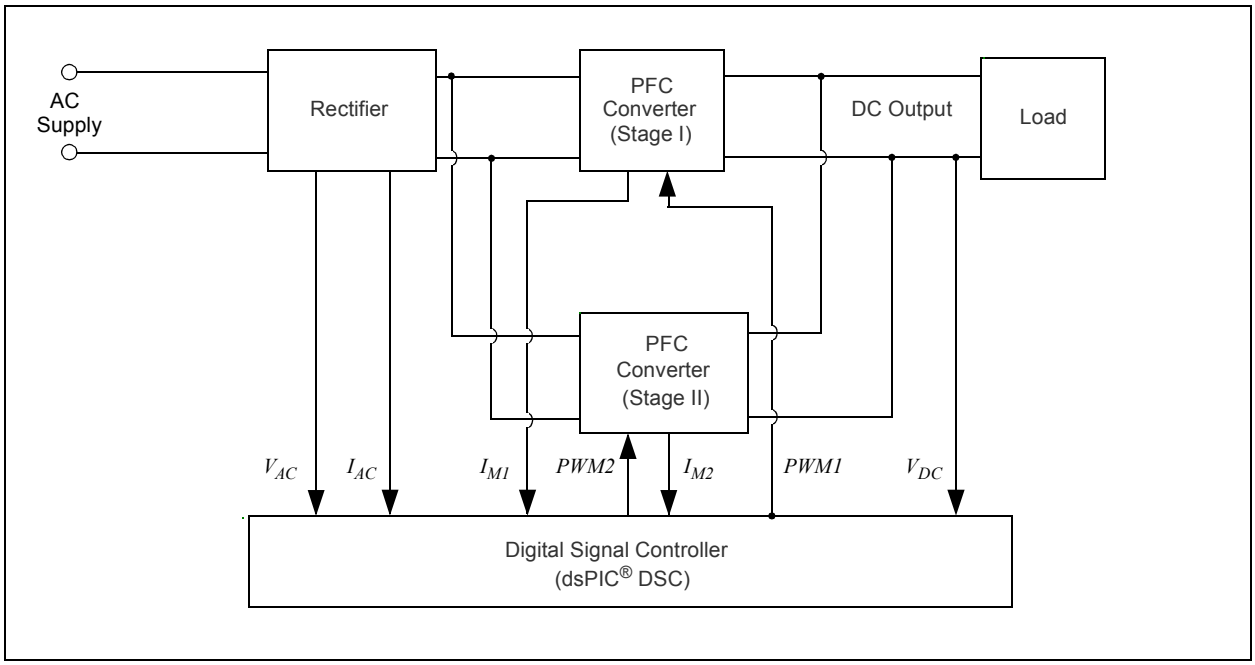


FIGURE 2: POWER CONVERSION TOPOLOGIES

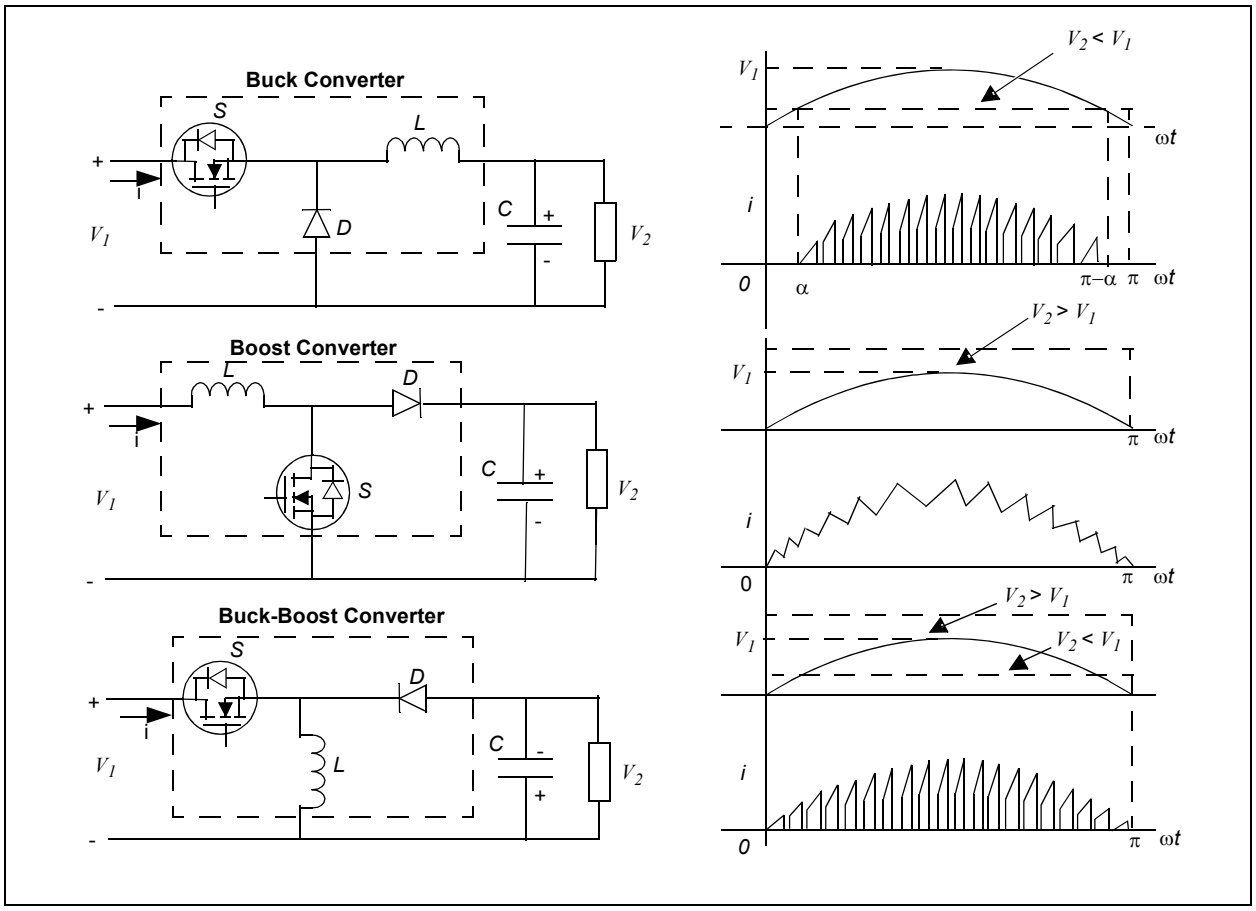


TABLE 1: COMPARISON OF DIFFERENT PFC TOPOLOGIES

Type of Converter	Output Voltage Polarity	Crossover Distortion	Line Current Shape
Buck	Positive	Yes	Always Discontinuous
Boost	Positive	No	Continuous
Buck-Boost	Negative	No	Always Continuous

Note: Based upon load conditions and inductor value, boost converters can be operated in Continuous Conduction mode.

IPFC DIGITAL DESIGN

In general, the PFC offers the following advantages:

- Lower energy and distribution costs
- Reduced losses in the electrical system during distribution
- Better voltage regulation
- Increased capacity to serve power requirements

The following are the limitations of a single-stage PFC when compared to an IPFC converter:

- Current ripple cancellation is not possible
- Unequal sharing of load when two converters are in parallel
- Large PFC inductor volume

The IPFC converter can overcome these limitations. It contains two boost converters, which are parallel coupled and are 180º out of phase current controlled with respect to each other, as shown in Figure 3.

At the input side, the total input current (I_{AC}) drawn from the source equals the sum of the two inductor currents (I_{L1} and I_{L2}). Because the ripple currents through the two inductors are out of phase, they cancel each other and reduce the total ripple current in the input side. At a duty cycle of 50%, the best cancellation of ripple currents is possible.

At the output side, current through the output capacitor (I_C) equals the sum of the two diode currents (I_{D1} and I_{D2}) minus the output current (I_{LOAD}).

FIGURE 3: IPFC BOOST CONVERTER CIRCUIT

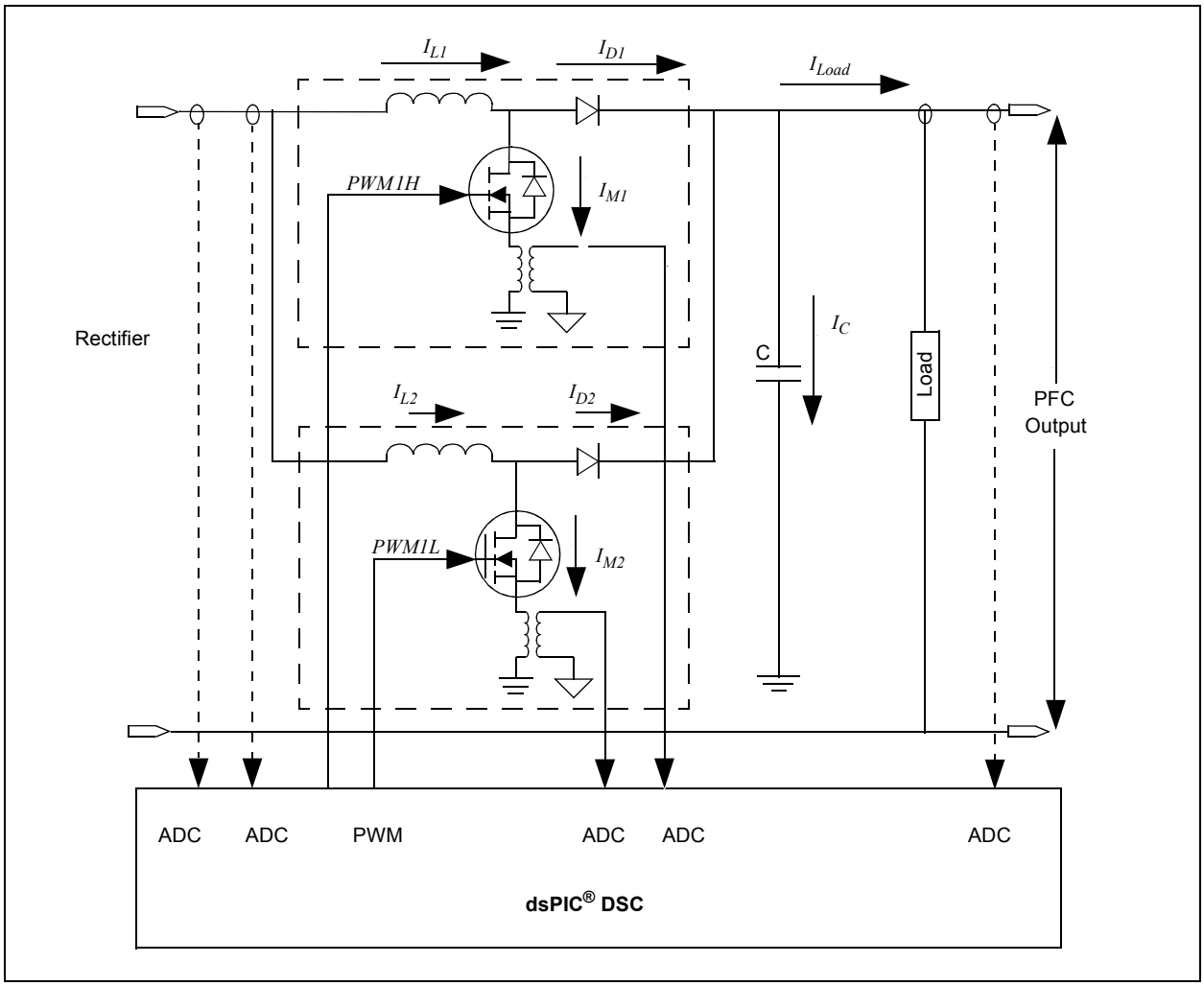
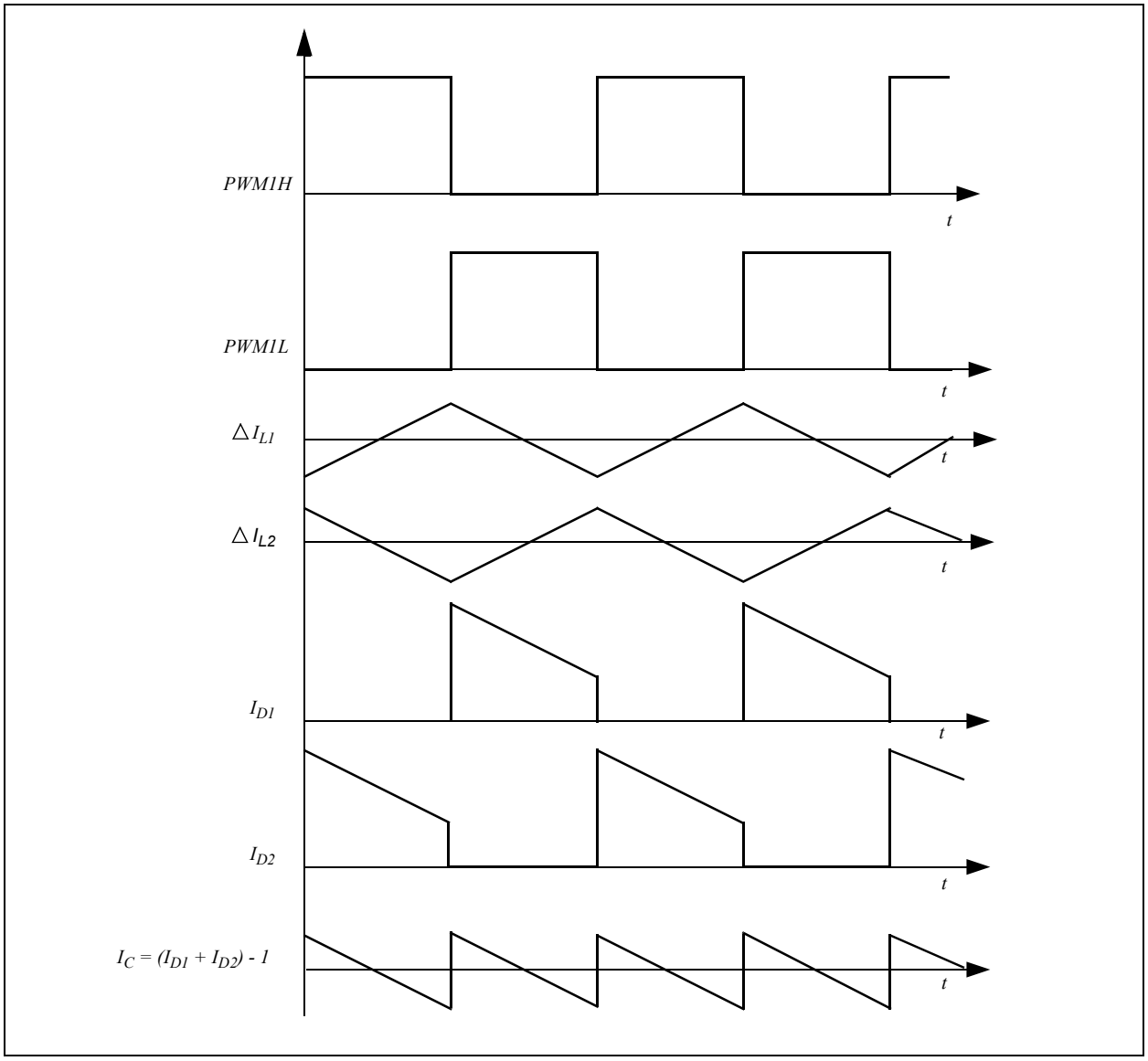


FIGURE 4: IPFC SIGNALS



Average Current Mode Control

The IPFC system uses the average current mode control method to meet the system requirements. The IPFC system uses the average current mode control method to meet the system requirements. For PFC, this control method is used to regulate DC output voltage while keeping the input current shape sinusoidal and in phase with the input voltage.

The control method operates in Continuous Conduction mode in most parts of the operating regions of the converter. The operation is primarily based on the value of the load current at any point and the selection of the inductor.

The various advantages offered by the Average Current Mode Control over other methods include:

- Suitable for operation at higher power levels
- Less ripple current in the inductors
- Reduces EMI filter requirements
- Less RMS current will be drawn from the power supply
- Continuous Conduction mode operation is possible

To derive the sine shape for the average inductor current, either a sinusoidal pattern can be generated in software or the rectified voltage itself can be used as a reference. Here, the rectified voltage is used to get the necessary shape of inductor current. T_S is the total PWM switching period, t_{ON} is the MOSFET conduction time, and t_{OFF} is the time during which the MOSFET is turned off. The control system controls the t_{ON} time in order to derive the necessary shape of the inductor current (see Figure 5). Figure 6 shows the block diagram of the digital average current mode control scheme.

FIGURE 5: IPFC INPUT CURRENT WAVEFORM

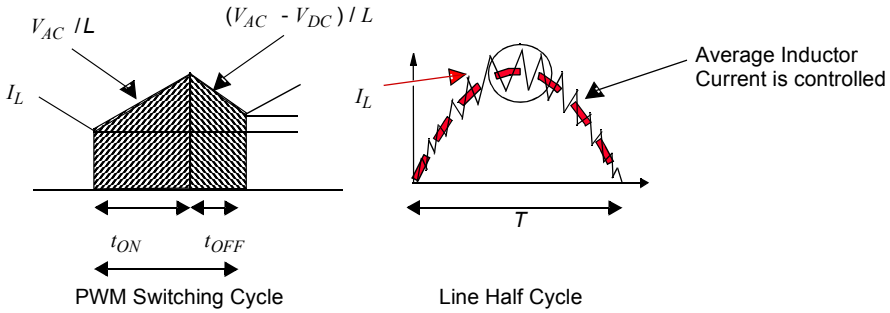
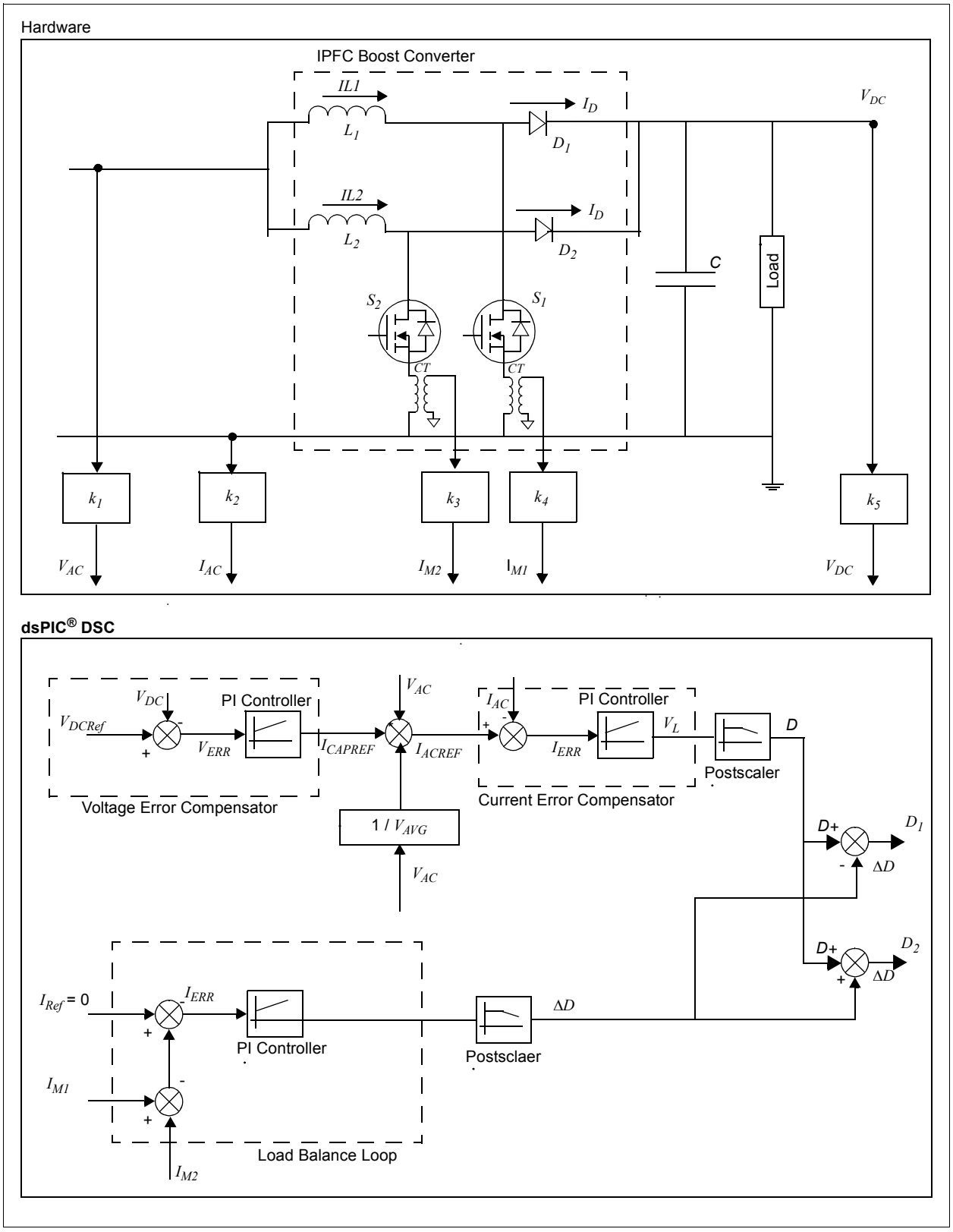


FIGURE 6: AVERAGE CURRENT MODE CONTROL FOR IPFC



Control Loops

The IPFC control system includes the following control loops:

- Voltage Control Loop
- Current Control Loop
- Load Balance Control Loop
- Input and Output Voltage Decoupling Loop

VOLTAGE CONTROL LOOP

This is a PI controller and the outermost loop in the control system. This loop regulates the output voltage regardless of any variations in load current (I_{Load}) and the supply voltage (V_{AC}). These are the inputs to the voltage control loop:

- Reference DC voltage (V_{DCREF})
- DC bus voltage (V_{DC})

The output of the voltage control loop is a control signal, which determines the reference current (I_{ACREF}) for the current control loop.

The voltage control loop executes at a rate of 2 kHz and the bandwidth of the voltage control loop is 10 Hz. The bandwidth is selected such that the effect of the input frequency ripple on the output DC voltage can be minimized at 100 Hz or 120 Hz.

CURRENT CONTROL LOOP

This is a PI controller and the inner loop of the control system. This loop corrects the error between these two currents, which are the inputs to the current control loop:

- Reference current signal (I_{ACREF})
- Input current (I_{AC})

The output of the current control loop is a control signal, which ensures that the input current (I_{AC}) follows the reference current (I_{ACREF}).

The current control loop executes at a rate of 50 kHz and its bandwidth is 4 kHz for a switching frequency of 100 kHz. The current control loop bandwidth and the execution rate should be much faster than that of the voltage control loop because it has to correctly track the semisinusoidal waveform whose frequency is twice the input frequency. The output of the current control loop decides the duty cycle ‘D’ required to switch the MOSFETs.

LOAD BALANCE CONTROL LOOP

The individual output voltage of each boost converter may differ by a small value. This drift is possible because of differences in the internal characteristics of the MOSFETs, internal resistances of the inductors, capacitors and the diodes. Therefore, when the same duty cycle is applied to both the MOSFETs, it may result in unequal sharing of the load between the two boost converter stages. This necessitates the presence of a load balance control loop that balances the currents in the two boost converter switches, which in turn results in the equal sharing of load between the two converters.

One of the inputs to the load balance control loop is the difference between the two MOSFET currents (I_{M1}- I_{M2}) of the two boost converters. The other input, which acts as a reference to this control loop, is tied to zero. This control loop mainly corrects the difference between the MOSFET currents and brings it close to the reference input, which is zero. The output of the load balance control loop will be a duty correction term (ΔD), which is added to the main duty cycle ‘D’ to get the duty cycle of the first boost converter, D_1. The ΔD term is subtracted from the main duty cycle ‘D’ to determine the duty cycle of the second boost converter, D_2.

INPUT AND OUTPUT VOLTAGE DECOUPLING LOOP

The IPFC also regulates the output DC voltage regardless of variations in the input voltage. This is achieved by decoupling the system from the input voltage. The output of the current error compensator derives the final duty cycle value of the MOSFETs. It considers the variations in the V_{AC} signal.

Digital Design of IPFC

In a dsPIC DSC-based application, the relevant analog parameters are discretized. This enables for easier and a more logical changeover from existing hardware to its digital counterpart. Table 2 shows the various hardware and software design parameters for the IPFC converter.

TABLE 2: HARDWARE AND SOFTWARE DESIGN PARAMETERS

No.	Design Parameter	Symbol	Value
Hardware Parameters			
1	Output power	P_{out}	350 watt
2	Input voltage range (rms)	V_{in}	85V to 265V
3	Input frequency range	f	45 Hz to 66 Hz
4	Output voltage	V_{DC}	400V
5	Output capacitance	C	360 µF
6	Inductance	L_1, L_2	700 µH
7	Switching frequency	f_s	100 kHz
Software Parameters			
1	Voltage control loop frequency	f_{VLoop}	2 kHz
2	Current control loop frequency	f_{ILoop}	50 kHz
3	Load balance control loop frequency	f_{LBLoop}	2 kHz
4	Voltage feedforward loop frequency	f_{FFLoop}	50 kHz
5	Average voltage calculation frequency	f_{AVG}	100 kHz
6	Voltage loop bandwidth	BW_{VLoop}	10 Hz
7	Current loop bandwidth	BW_{ILoop}	4 kHz
8	Integral voltage loop bandwidth	IBW_{VLoop}	2.5 Hz
9	Integral current loop bandwidth	IBW_{ILoop}	1 kHz
10	Load balance loop bandwidth	BW_{LBLoop}	200 Hz

DESIGN OF COMPENSATORS

All the compensators use digitally implemented Proportional-Integral (PI) controllers. The following sections describe the process used to select the proportional and integral gains for the voltage, current and load balance compensators.

Using the design parameters defined in Table 2, the following parameters are calculated (see Equation 3):

- Maximum resistance
- Maximum conductance

EQUATION 3:

$$R_{max} = \frac{V_{max}}{I_{max}}$$

$$R_{max} = \frac{440V}{12.54A} = 35.08\Omega$$

$$\sigma_{max} = \frac{1}{R_{max}}$$

$$\sigma_{max} = \frac{1}{35.08\Omega} = 0.0285\,mho$$

where:

R_{max} = Maximum resistance

σ_{max} = Maximum conductance

VOLTAGE ERROR COMPENSATOR

In the voltage error compensator, the input is the difference in voltages and the output is the capacitor current; therefore, the transfer function has a unit of conductance. The transfer function is divided by the maximum conductance (or multiplied by the maximum resistance) in order to get the output in the range of -1 to +1, similar to per unit quantities.

The proportional gain for the voltage error compensator is derived using the small signal model of the boost converter (see Equation 4).

EQUATION 4:

$$G_a = 2 \times \pi \times C \times BW_{VLoop} \times R_{max}$$

$$G_{sa} = \frac{2 \times \pi \times G_a \times IBW_{VLoop}}{f_{VLoop}}$$

where:

G_a = Proportional Gain for Voltage Error Compensator
G_{sa} = Integral Gain for Voltage Error Compensator
BW_{VLoop} = Voltage Loop Bandwidth
IBW_{VLoop} = Integral Voltage Loop Bandwidth
f_{VLoop} = Voltage Control Loop Frequency

CURRENT ERROR COMPENSATOR

In the current error compensator, the input is the difference in currents and the output is the inductor voltage and therefore, the transfer function has a unit of resistance. This quantity is divided by a factor of maximum resistance (or multiplied by a factor of maximum conductance) to get the output in the range of -1 to +1.

The Proportional Gain for the current error compensator is derived using the small signal model of the boost converter (see Equation 5).

EQUATION 5:

$$R_a = 2 \times \pi \times L \times BW_{ILoop} \times \sigma_{max}$$

$$R_{sa} = \frac{2 \times \pi \times R_a \times IBW_{ILoop}}{f_{ILoop}}$$

where:

R_a = Proportional Gain for Current Error Compensator
R_{sa} = Integral Gain for Current Error Compensator
BW_{ILoop} = Current Loop Bandwidth
IBW_{ILoop} = Integral Current Loop Bandwidth
f_{ILoop} = Current Control Loop Frequency

LOAD BALANCE ERROR COMPENSATOR

Similar to the current error compensator, the load balance compensator is also designed by normalizing the output to a range of -1 to +1.

The proportional gain for the load balance compensator is derived using the small signal model of the boost converter (see Equation 6).

EQUATION 6:

$$K_a = 2 \times \pi \times L \times BW_{LBLoop} \times \sigma_{max}$$

$$K_{sa} = \frac{2 \times \pi \times K_a \times IBW_{LBLoop}}{f_{LBLoop}}$$

where:

K_a = Proportional Gain for Load Balance Error Compensator
K_{sa} = Integral Gain for Load Balance Error Compensator
BW_{LBLoop} = Load Balance Loop Bandwidth
IBW_{LBLoop} = Integral Load Balance Loop Bandwidth
f_{LBLoop} = Load Balance Control Loop Frequency

AVERAGE VOLTAGE CALCULATION

The average value of the rectified input voltage is used to derive the necessary shape of the sine wave. In order to get the half sinusoidal wave shape (i.e., the absolute value of the sine) for the input current, the output of the voltage error compensator is multiplied with a factor of $|sin\theta|$. The resulting value acts as a reference term to the input of the current error compensator. The $|sin\theta|$ can be obtained either by creating a lookup table in software or can be extracted from the inherent shape of V_{AC}, feedback of the rectified AC voltage, which will have the sinusoidal shape.

In this application, the sine wave shape is obtained using the feedback voltage V_{AC}. The instantaneous input rectified voltage V_{AC} is given by Equation 7.

EQUATION 7:

$$V_{AC} = V_m \cdot |Sin\theta|$$

where:

V_m = Peak Voltage of the half sine wave
V_{AC} = Rectified AC voltage

To get the shape of the waveform, regardless of the magnitude of the input voltage, Equation 8 calculates the value of $|sin\theta|$.

EQUATION 8:

$$|sin\theta| = \frac{V_{AC}}{V_M}$$

For a full wave bridge rectifier output voltage, the peak voltage can be expressed in terms of the average voltage (see Equation 9).

EQUATION 9:

$$V_{avg} = \frac{2V_m}{\pi}$$

$$V_m = \frac{\pi V_{avg}}{2}$$

Equation 10 is obtained by replacing the value of V_m in Equation 8. It ensures that the current reference term is multiplied by only the half of the sine wave shape and remains unaffected by the magnitude of the voltage.

EQUATION 10:

$$|sin\theta| = \frac{2V_{AC}}{\pi V_{avg}}$$

Since the average value of the input voltage does not vary widely, the average voltage can be calculated and updated once in many cycles.

INPUT AND OUTPUT VOLTAGE DECOUPLING CALCULATION

In the boost converter circuit, V_{DC} is assumed to be close to the base voltage (i.e., 400V). The following equations are derived using Kirchhoff's laws (see Equation 11).

EQUATION 11:

$$V_{AC} - V_L - (Dd \cdot V_{DC}) = 0$$

$$Dd = (V_{AC} - V_L) / V_{DC}$$

$$D = 1 - Dd = 1 - (V_{AC} - V_L) / V_{DC}$$

where:

V_{AC} = Input Rectified Voltage obtained from the ADC

V_L = Inductor Voltage obtained from the current error compensator

V_{DC} = Output DC Voltage obtained from ADC

D = Main Duty cycle

Dd = Duty cycle of a diode

Thus, it is evident that the effect of input voltage variations is compensated by correcting the main duty cycle (D), which is input to the load balance control loop. The load balance compensator is used to compute load correction term. Using the duty cycle (D) and load correction term, the individual duty cycles for the two boost converters are derived.

Equation 12 describes the final equations that result from the decoupling control loop.

EQUATION 12:

$$D = 1 - \frac{(V_{AC} - V_L)}{V_{DC}}$$

$$D1 = D + \Delta D$$

$$D2 = D - \Delta D$$

where:

D = Main duty cycle (D)

$D1$ = Duty cycle of MOSFET 1 (D1)

$D2$ = Duty cycle of MOSFET 2 (D2)

Performance Improvement by Interleaving Two PFCs

The inductor value is chosen depending on the allowable ripple current in the system. In a single stage PFC converter, for a given power level and the switching frequency, the energy stored in the inductor is calculated using Equation 13. The amount of ripple current, ΔI, determines the value of the inductance 'L'.

EQUATION 13:

$$E_{Singlestage} = \frac{1}{2}LI^2$$

In a two stage IPFC converter, for the same power level and switching frequency, the energy stored in the inductors is computed using Equation 14.

EQUATION 14:

$$E_{Interleaved} = \frac{1}{2}(2L)\left(\frac{I}{2}\right)^2 + \frac{1}{2}(2L)\left(\frac{I}{2}\right)^2$$

Here, the inductance for each stage is 2L, because the ripple current in each stage is half of that of the single stage PFC converter. Because of the interleaving, the ripples tend to cancel out and a better performance for the same component size is obtained. This also results in the lesser total line ripple current. Therefore, the ripple current requirement of the individual stages are reduced, which in turn, reduces the inductance required for each of the stages.

The ripple current (ΔI) is chosen such that it is twice that of the selected value. Therefore, the energy stored in the inductors is computed using Equation 15.

EQUATION 15:

$$E_{Interleaved} = \frac{1}{2}(L)\left(\frac{I}{2}\right)^2 + \frac{1}{2}(L)\left(\frac{I}{2}\right)^2 = \frac{1}{2}E_{Singlestage}$$

Note: For a given ripple content on the AC line current, the inductor size can be reduced significantly by interleaving two boost converters. Conversely, for a given inductor size, the ripple currents can be reduced significantly (see Equation 15).

Function Usage in Software

All the functions used in this application software are developed using the C language. The numerical constants and variables are defined in Q15 format or 1.15 format. Because the selected dsPIC DSC device is a 16-bit digital signal controller, if the gains or constants exceed the range of 16 bits in the intermediate calculations, they are appropriately prescaled to a different format during computation and the end result is again converted to the Q15 format by postscaling them.

Table 3 lists and describes the functions used in the software (see **Appendix A: "Source Code"** for additional information).

TABLE 3: FUNCTION USAGE IN SOFTWARE

File Name	Function Name	Description
Source Files		
main.c	main()	Configures the operating frequency of the device.
		Configures the auxiliary clock module.
		Calls the functions for configuring ADC and PWM modules.
		Checks the fault status.
adc_isr.c	ADCP2Interrupt()	Read values of currents and voltages.
		Checks the fault condition.
		Executes the various control loops, if fault doesn't exist.
		Disables PWM outputs, if fault exists.
InitdsPIC.c	Init_ADC()	Configures the ADC module.
	Init_PWM()	Configure the PWM module.
	Init_IO()	Configures IO ports.
	Init_CMP()	Configures Analog Comparator module.
Vars.c	—	Declaration and Initialization of all the global variables.
compensators.c	VoltageController()	Executes the PI compensator for the voltage error compensator.
	CurrentController()	Executes the PI compensator for the current error compensator.
	FeedForward()	Provides the feedforward term and final duty cycle value.
	AverageVoltageCalc()	Calculates the average value of AC rectified voltage.
	LoadBalance()	Executes the load balance compensator for the two boost converters.
Header Files		
defines.h(1)	—	Defines all the global function prototype and global parameters.
vars.h	—	Includes the supporting file for Vars.c .
		Defines all the extern global definitions.

Note 1: This file is updated based on the type of hardware components used, power level, control loop frequencies, control loop bandwidth and other parameters. After these parameters are entered as per the design, the remaining gains are automatically calculated and scaled by the software. For further details, refer to **Appendix A: "Source Code"**.

Resource Usage in Software

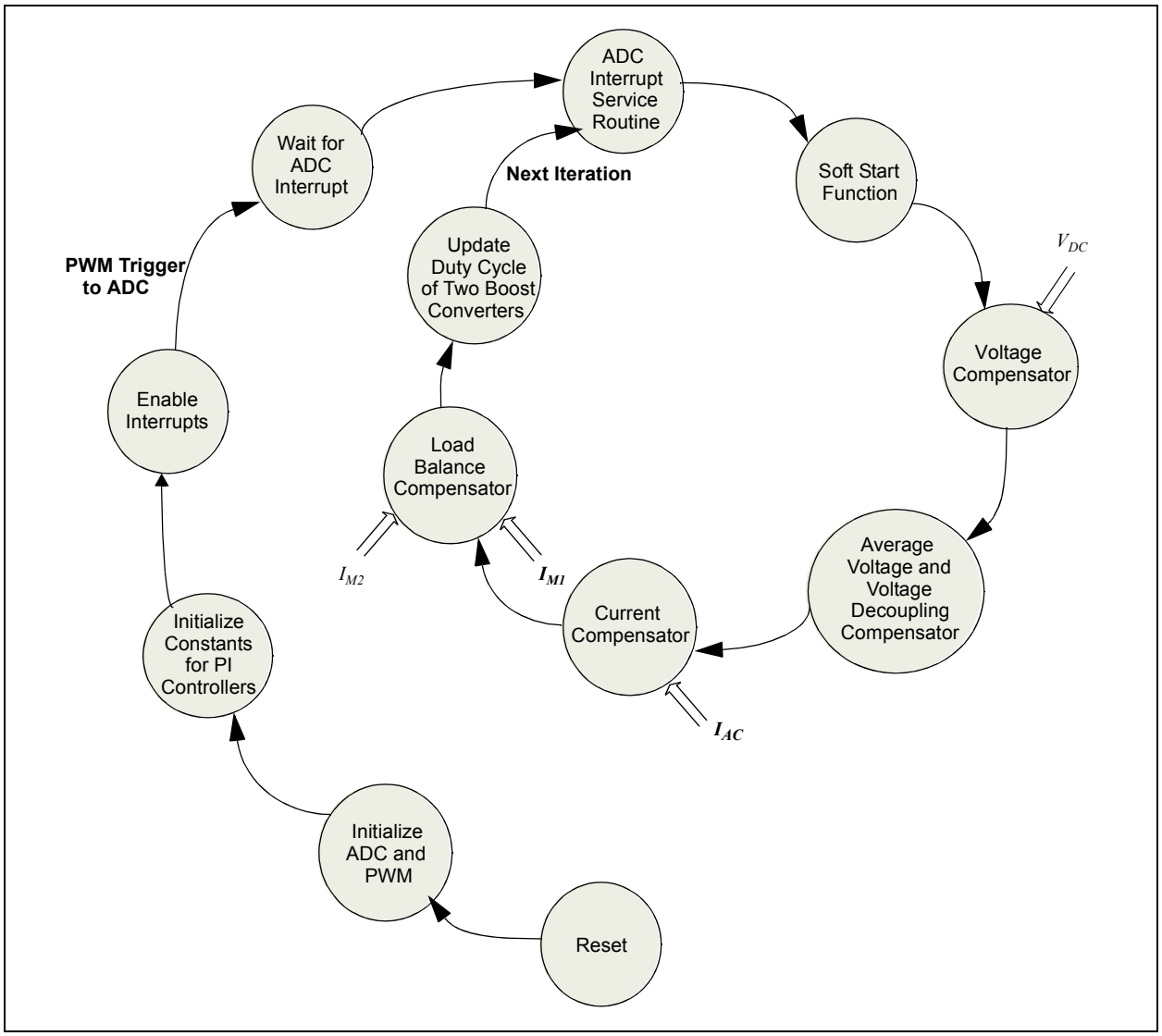
Table 4 lists the resources utilized by the IPFC software when developed on a dsPIC33FJ16GS504 device.

TABLE 4: RESOURCE USAGE IN SOFTWARE

Resource	Components	Value
Memory	Program Memory/Flash	3500 bytes: ~21%
	Data Memory/RAM	110 bytes: ~5%
MIPS/Instruction Cycle	Current Loop	~ 130 cycles @ 50 kHz: 7 MIPS @ 40 MHz
	Voltage Loop	~ 110 cycles @ 2 kHz: 0.3 MIPS @ 40 MHz
	Averaging Loop	70 cycles @ 15 Hz: Negligible@ 40 MHz
	Feed-forward Loop	~ 100 cycles @ 50 kHz: 5 MIPS @ 40 MHz
	Load Balance Loop	~ 90 cycles @ 2 kHz: 0.2 MIPS @ 40 MHz
	Overhead	~ 50 cycles at 50 kHz and ~ 2.5 MIPS at 40 MHz

Note: The entire code, in the worst case, would take on an average of < 15 MIPS = ~38%

FIGURE 7: STATE FLOW DIAGRAM OF DIGITAL IPFC



MATLAB® MODELING

The control system design for the IPFC system is accomplished using the MATLAB SIMULINK® model. The various system gains and the parameter values of the PI controllers and the compensators are derived using this model. This section describes the MATLAB modeling, design considerations for the IPFC system and the design constraints.

Figure 8 shows the IPFC MATLAB model and Figure 9 shows the Digital Control System. Equation 16 lists analytical expressions that describes the boost converter circuit.

EQUATION 16: BOOST CONVERTER

The following are the basic power converter equations for the boost converter:

$$V_L = V_{AC} - Dd \cdot V_{DC}$$

$$I_D = DdI_L$$

$$V_{DC} = \frac{I_C}{sC}$$

$$I_{AC} = \frac{V_L}{sL}$$

The IC is calculated by applying the Kirchhoff's current law at point A (see Figure 8),

$$I_C = I_D - I_{Load}$$

where:

V_{AC} = Input Rectified Voltage

V_L = Inductor Voltage obtained from the current error compensator

V_{DC} = Output DC Voltage obtained from ADC

D = Main Duty cycle

Dd = Duty cycle of a diode

I_D = Diode current

I_{AC} = Rectified AC current

The IPFC circuit performs the following major tasks:

1. Ensures that the input current follows the input supply voltage and assumes the same wave shape as that of the voltage (Distortion Factor).
2. Makes the input current drawn from the system sinusoidal and in phase with the input voltage (Displacement Factor).
3. Maintains boost output voltage at a constant value (usually 400V) under varying load conditions and input voltage. Typically, sine wave input voltage to the rectifier varies from 85V to 265V rms.

The main objective of the control system is to control the inductor current (I_{AC}) in order to track the reference signal (I_{ACREF}) (see Figure 6). This reference signal is in phase with the rectified voltage and therefore, it changes with time.

Typically, the rectified sine voltage has a frequency of 100-120 Hz and it contains higher order harmonics. The reference current signal (I_{ACREF}) will also have the same frequency. Therefore, for reliable command tracking, the bandwidth required for current should be at least 10 times the frequency of I_{ACREF} signal.

For a switching frequency of ~100 kHz, the control loop bandwidth for current is chosen between 4000 Hz and 6000 Hz. The voltage loop bandwidth is chosen to be 10 Hz so that the current signal (100 or 120 Hz) does not get distorted. The zero bandwidth or Integral Voltage Bandwidth selected here is one-fifth to one-fourth of the voltage loop bandwidth.

Because the voltage and current loop bandwidths are far apart, they do not affect each other and are disjointed. So, approximate relations obtained from the characteristic equations are very near to the actual equations.

FIGURE 8: IPFC MATLAB® MODEL

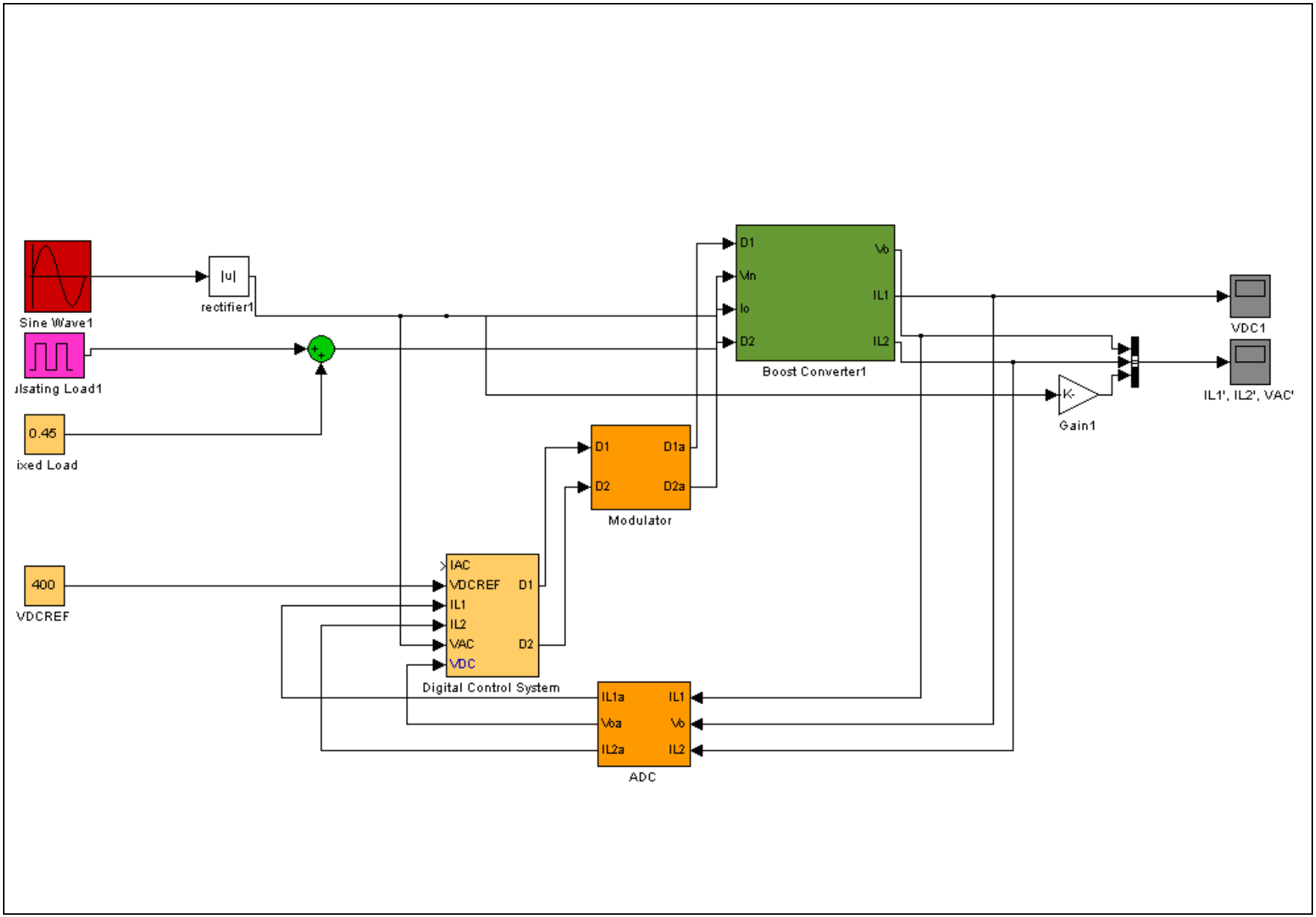
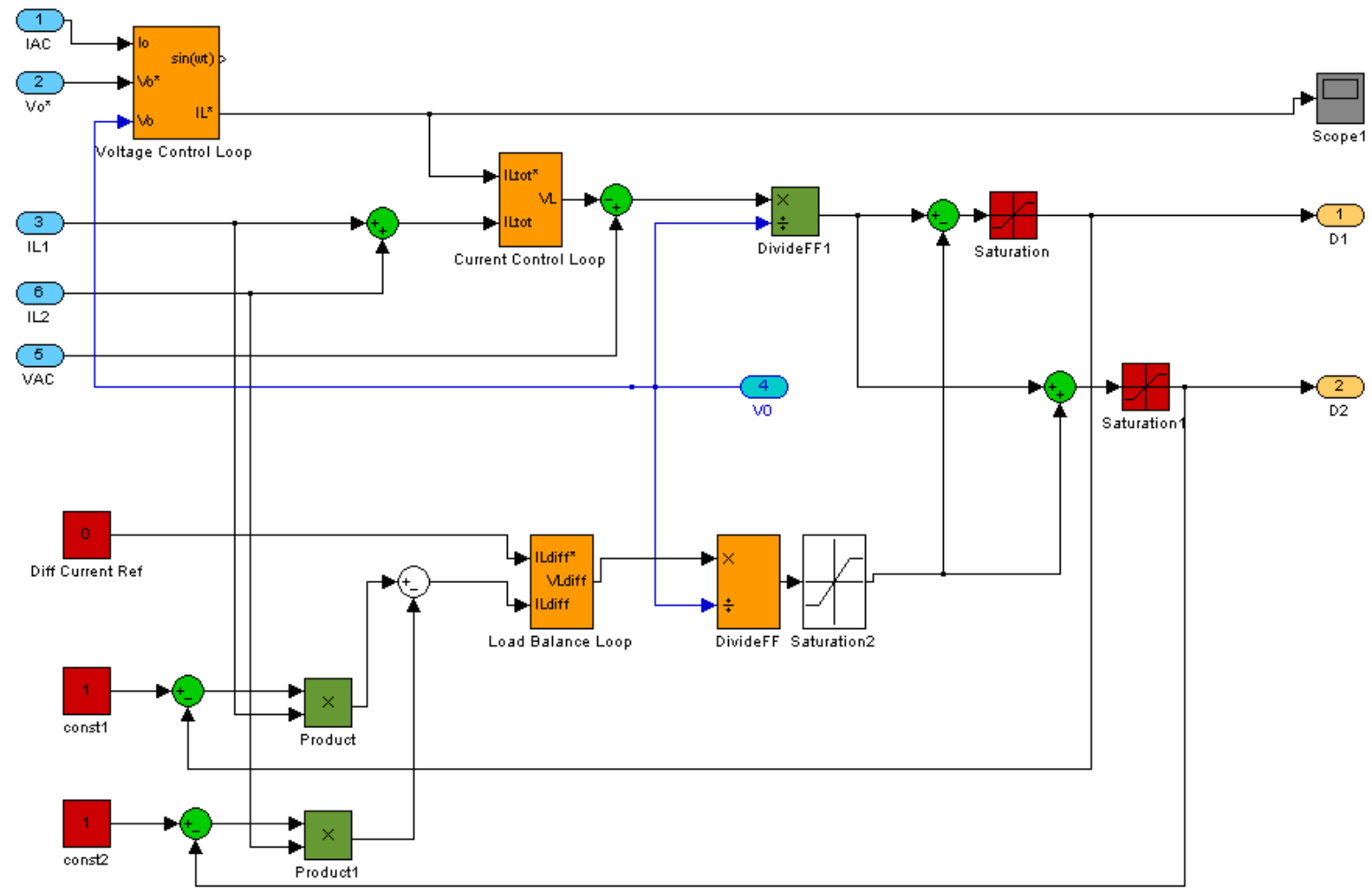


FIGURE 9: IPFC DIGITAL CONTROL SYSTEM MODEL



Input Voltage Feed-forward Compensator

As the voltage loop bandwidth is small, the voltage feed-forward method is used to correct the input voltage change. However, if diode duty cycle Dd is generated using V_{AC} and V_{DC}, the feed-forward is not required.

For the safety reasons, the maximum duty cycle of the MOSFET is limited to 90%. This means that the minimum value for Dd is limited to 10%.

In a typical IPFC circuit, presence of a bulk capacitor results in the slowing varying output voltage, which can be assumed to be constant. For future implementation improvements and to save processor MIPS, the calculation of $1/V_{DC}$, needed for the MOSFET duty cycle determination, can be done at a slow rate of 1 ms, since VDC does not vary much during a 1 ms period, whereas the control loop can be executed every 10 μs (100 kHz).

I_{ACREF} should have the following properties:

- I_{ACREF} should be proportional to V_{AC} or $|sin(\theta)|$
- The diode current ($I_D(t)$) should be proportional to error in output voltage (V_{DCREF} - V_{DC}) so that the error can be reduced to zero by controlling $I_D(t)$.
- I_{AC} should follow the input rectified voltage wave. The output voltage error that occurs due to changes in the load needs to be corrected at a slower rate in order to maintain the shape of the I_{AC}. Therefore, the bandwidth for the voltage loop is chosen to be 1/10 of the rectified sine wave frequency. BW_{VLoop} is chosen to be 10-15 Hz.

By using Equation 10 and Equation 16, the following equation is derived.

EQUATION 17:

$$I_{ACREF} = G \cdot (V_{DCREF} - V_{DC}) \cdot |Sin\theta| \cdot (\pi/2)$$

where:

I_{ACREF} = Capacitor Current Reference
V_{DCREF} = DC Bus Reference Voltage
V_{DC} = DC Bus Voltage
G = PI Controller Transfer Function Gain

Digital Design Considerations

The following aspects are considered while implementing the solution in MATLAB:

- **PID Controller**

  The modelling is performed using the zero order hold function and a PID controller. The Zero order hold implies that the value of the diode duty cycle (Dd) is kept constant for one sampling period.

- **Continuous to Discrete Transformation (c2d MATLAB function):**

  A continuous system is converted to discrete system using the `c2d` function available in MATLAB. Equation 18 lists the continuous and discrete forms of the various terms implied in the system's model.

EQUATION 18:

Term in Continuous Time Domain	Terms in Discrete Time Domain
K_p	K_p
$\frac{K_i}{s}$	$\frac{K_i \cdot T_s(z^{-1})}{1 - z^{-1}}$
$K_d s$	$\frac{K_d \cdot T_s(z^{-1})}{1 - z^{-1}}$

Zero order hold with appropriate sampling time is added to the SIMULINK model to drive the system.

- **Quantizations**

  The ADC and PWM quantizers and saturation blocks are implemented in SIMULINK.

- **Bandwidth Selection**

  As a rule of thumb, the bandwidth should be at most 1/7th of the control loop frequency. The control loop frequency is also limited by the switching frequency.

- **Number Resolution**

  The product ($K_i.T_s$) may become very small due to the finite fixed point processor representation in the DSC. This will lead to steady state errors. It may be desirable to have a slower frequency for the outer loop control execution to counteract this effect. This will ensure that T_s is large enough to produce a finite number every cycle.

Design Constraints

The following are the design constraints:

1. Due to practical limits on the system parameters, such as the duty cycle (i.e., D > 10%), the flat regions exists in the current wave shape when the voltage is near zero. Therefore, when the maximum turn-on time for a MOSFET is clamped, and the input voltage (V_{AC}) is near zero, it is impossible to boost the output voltage to V_{DC} if the converter is operating in Continuous Conduction mode.

   For example, if $V_{in}(t)$ is 20V and V_o is 400V (i.e., gain is 20), the diode cannot be ON for more than 5% (1/20%) of time in Continuous Conduction mode. As the duty ratio is clamped to 10%, the result is the non-ideal wave shape in that region of operation.

2. As the bandwidth of V_{DC} is small, the correction and stabilization of the system requires a long time. To minimize the change in V_{DC} under changing loads, the large value of C is selected. If the load current can be measured using a separate current sensor, its effects could be decoupled. This is known as load feed-forward or disturbance decoupling. So, instead of the load causing a dip, and then the PI controller taking a corrective action, the controller takes this into account before the dip occurs. With this method, the output capacitor size can be reduced significantly.

3. A careful analysis yields that the voltage loop bandwidth is also a function of duty ratio and it is equal to ($BW_{VLoop} * Dd * 2$) Hz. Therefore, as the duty cycle changes, the bandwidth also changes. It is maximum at the peak of the sine wave and minimum near the zero crossings.

LABORATORY TEST RESULTS AND WAVEFORMS

Figure 10 to Figure 15 show the waveforms for the I_{AC}, V_{AC} and V_{DC} at 175W and 350W. This information aids in validating the digital implementation on a dsPIC DSC device.

FIGURE 10: I_{AC} AND V_{AC} AT 175W

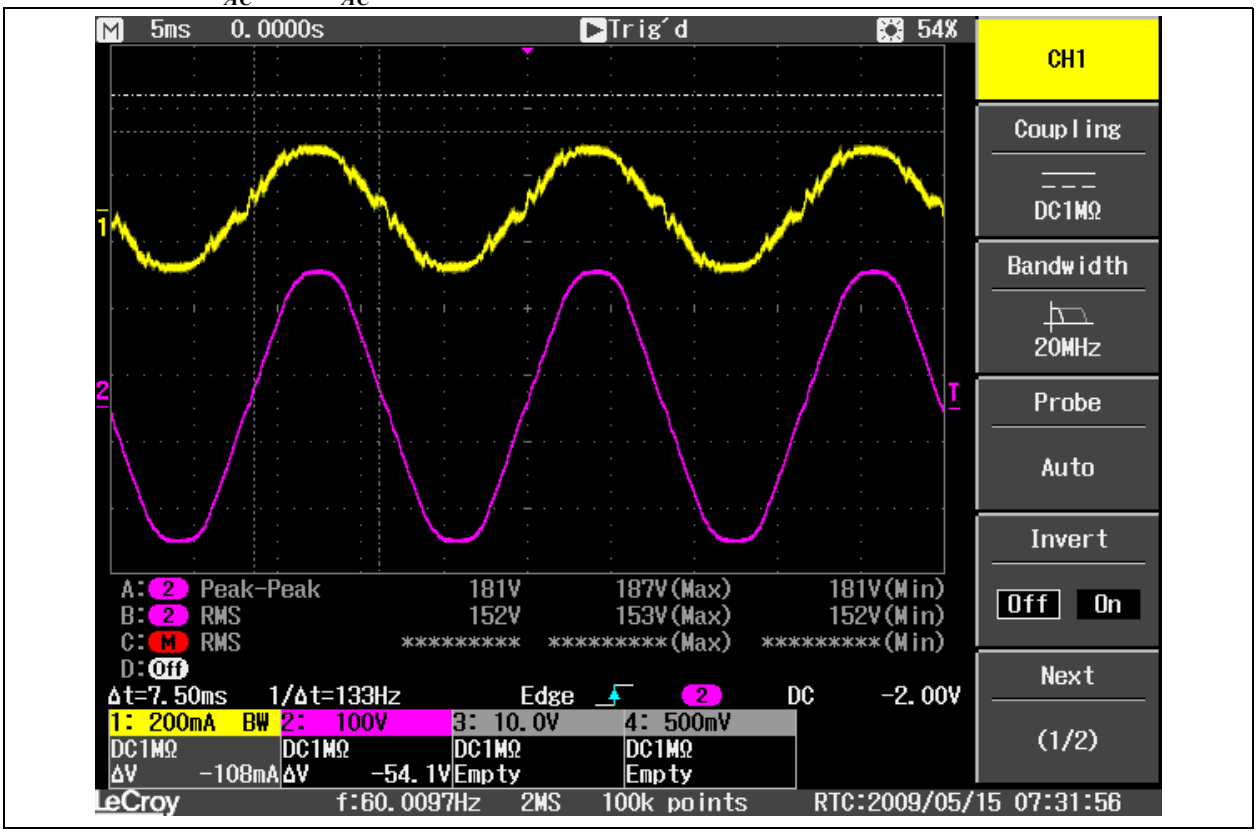


FIGURE 11: I_{AC} AND V_{AC} AT 350W

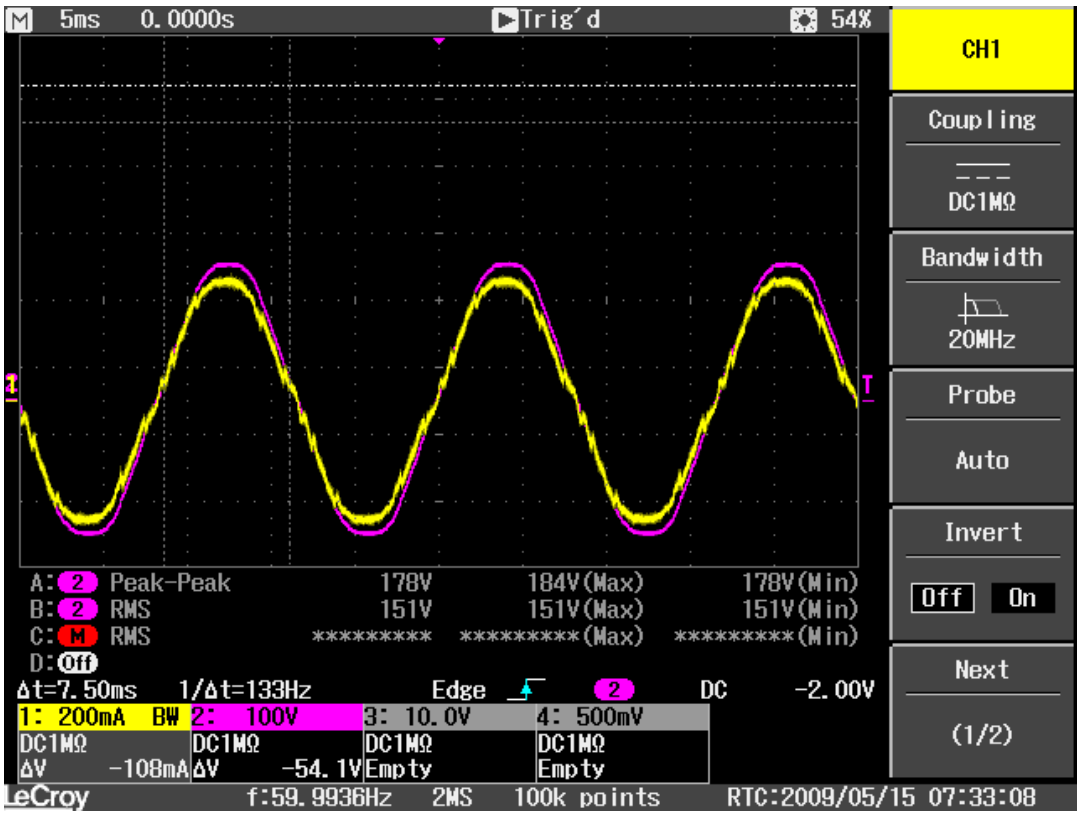


FIGURE 12: I_{AC} AND V_{AC} TRANSIENT FROM 175W TO 350W

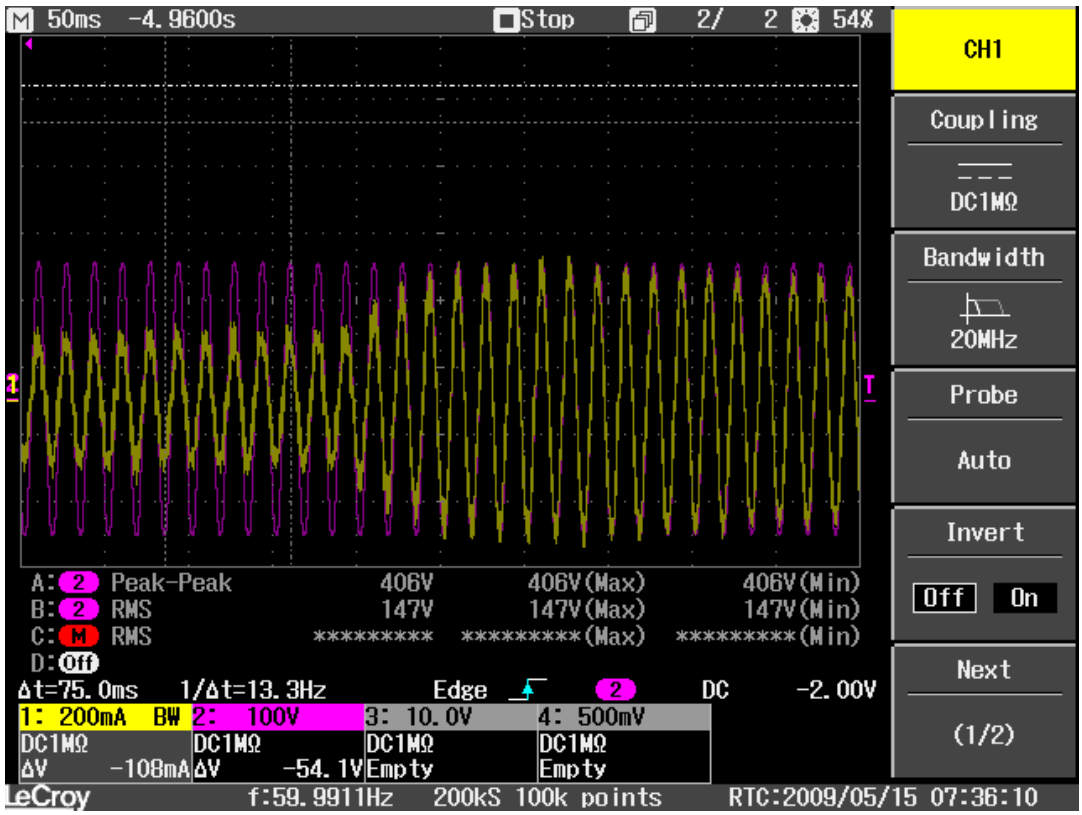


FIGURE 13: I_{AC} AND V_{AC} TRANSIENT FROM 350W TO 175W

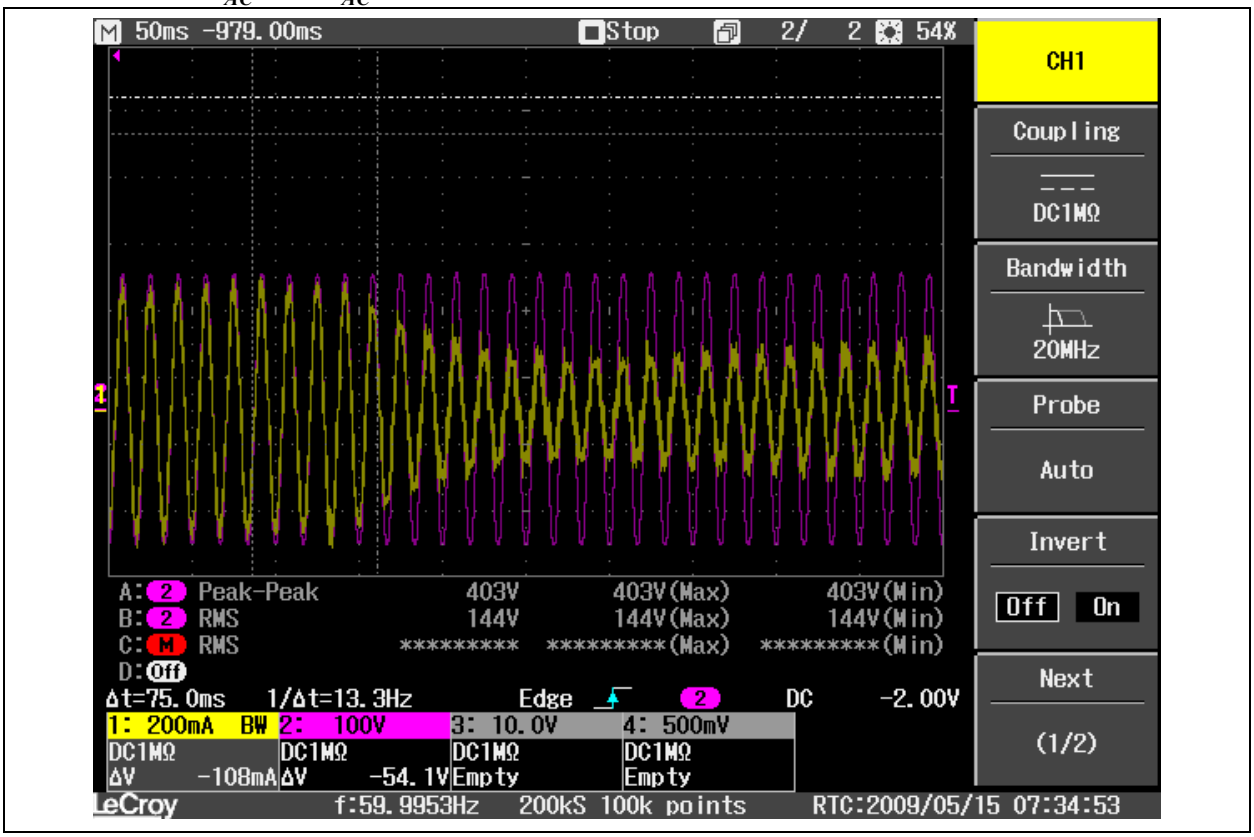


FIGURE 14: 175W TO 350W V_{DC} RESPONSE

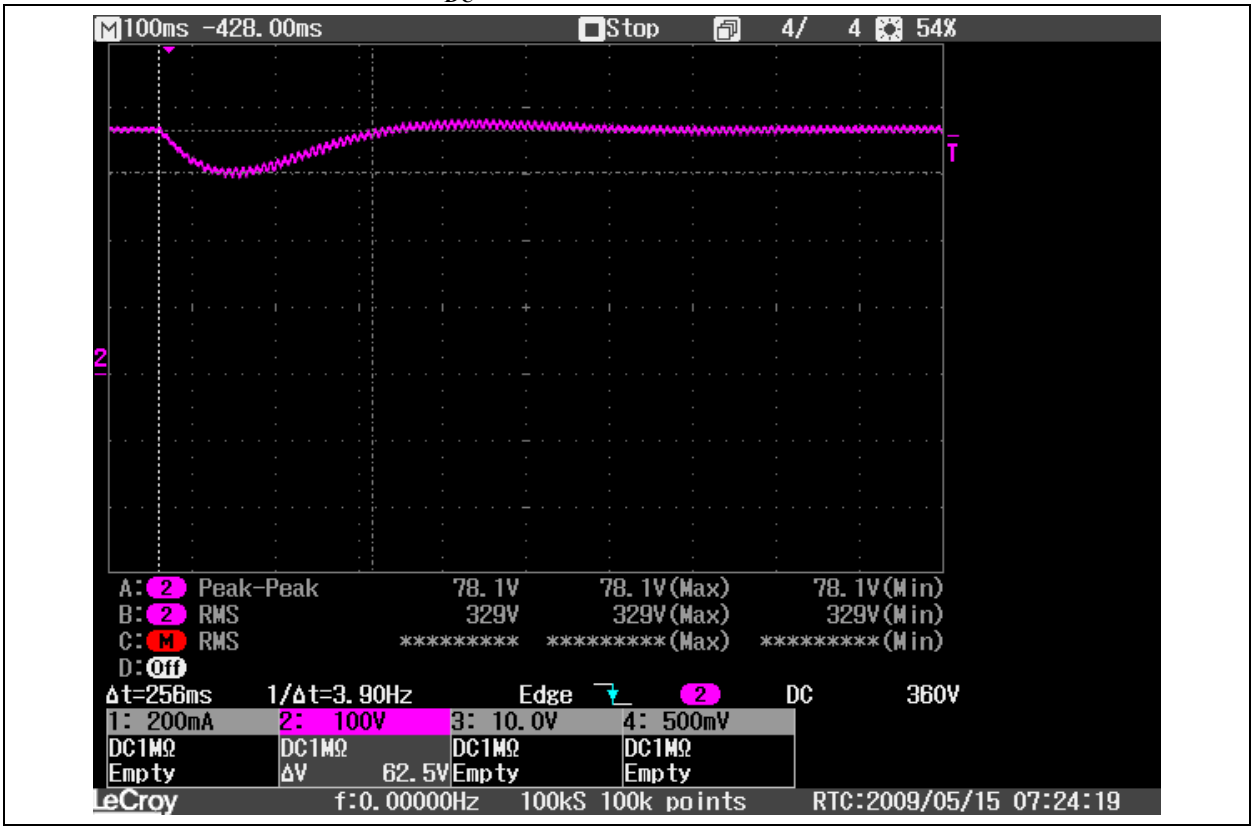
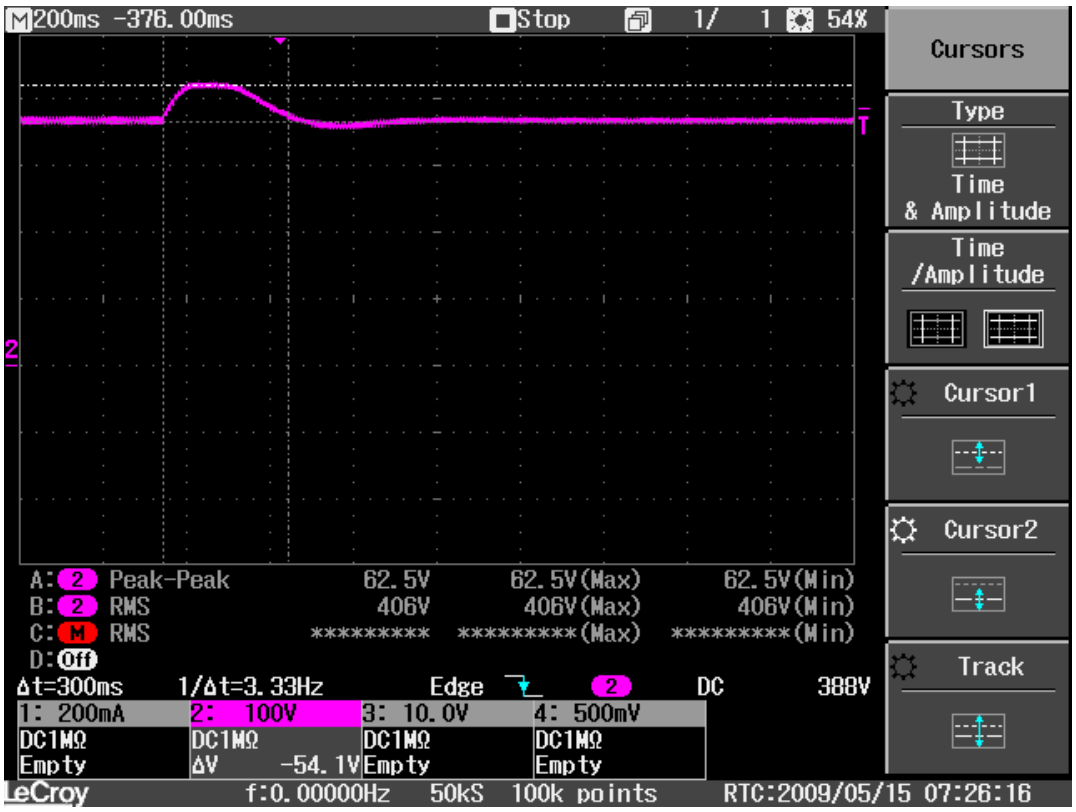


FIGURE 15: 350W TO 175W V_{DC} RESPONSE



IPFC HARDWARE DESIGN

Note: For more information about manufacturers' part numbers and data sheets, refer to the Bill of Materials (BOM), which is included in the reference design archive file (see **Appendix A: "Source Code"**).

This section provides the hardware details and design guidelines. Figure 16 shows the block diagram of the IPFC system. The major hardware building blocks, shown in Figure 16, are discussed in this section. The core part of the IPFC system is the boost converter stage. The boost converter and various components of the system are designed to ensure system robustness and versatility.

FIGURE 16: IPFC SYSTEM BLOCK DIAGRAM

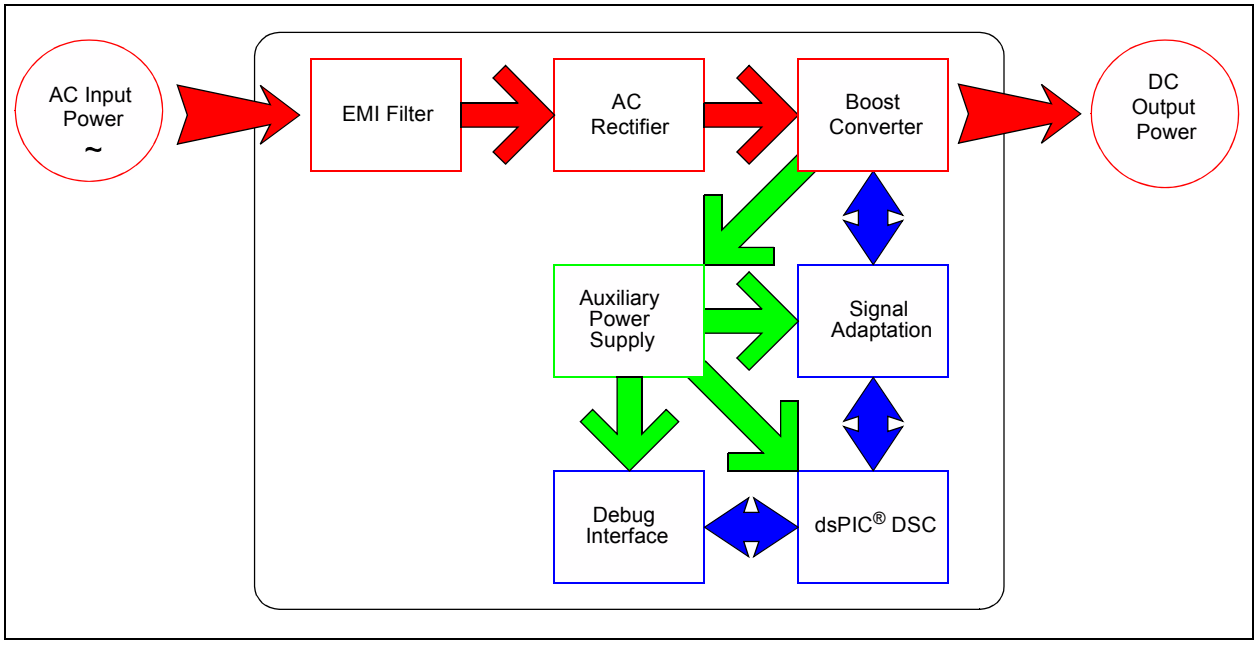
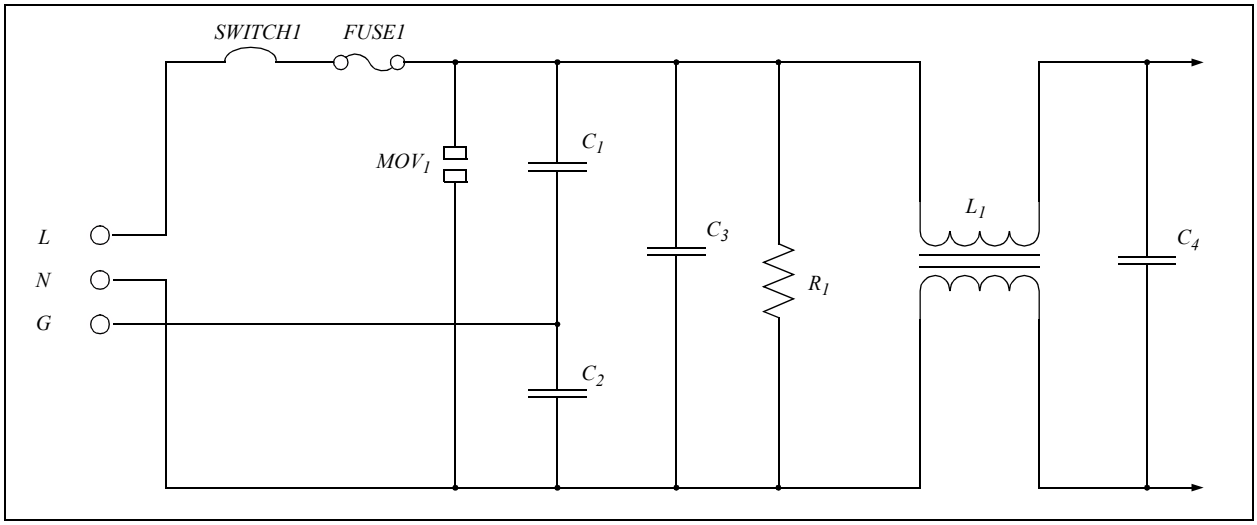


FIGURE 17: EMI FILTER CIRCUIT



EMI Filter Block

The EMI filter located between the input terminals of the main supply and the AC rectifier circuitry is a single stage π quadruple type filter, which is designed to meet the standards for conducted EMC. The input voltage range of the EMI filter is 85-265 V_{AC}. The output voltage of the EMI filter will be in the range of 85-265 V_{AC}.

The simplified schematic of the EMI filter circuit is shown in Figure 17. L_1 is a dual-wound toroidal inductor. C_1 and C_2, connected to the ground (G) are Y2 class compliant and meets the standards for the CATII overvoltage category. The choke (L_1) and the capacitors (C_1, C_2) filter the common mode noise.

The choke (L_1) offers a high impedance path to the in-phase component of the common mode noise, while C_1 and C_2 shunt the high-frequency component of the noise to the ground. The differential mode noise is filtered using C_3 and C_4. The discharge resistor is used when the circuit is plugged off. The varistor, MOV_1, and a fuse provides overvoltage/overcurrent protection.

Note:	The EMI/EMC filter value has been chosen based on switching frequencies and expected noise levels in the system. This value may be changed based on the final test results of EMI/EMC.

AC Rectifier Block

A diode bridge rectifies the input AC signal. It supports the rated AC input voltage (85-265 V_{AC}) and the specified power ratings. The rectifier block also provides overcurrent protection using a Negative Temperature Coefficient (NTC) thermistor.

Boost Converter Block

The boost converter contains IPFC stages and is fed from the rectifier's output. The simplified schematic of the boost converter circuit is shown in Figure 18. The regulated output voltage of the converter is 400 V_{DC}.

The converter contains two boost converter stages, which are parallel coupled and are 180º out of phase with respect to each other. This configuration enables power balancing between the two units. The dimensioning of the circuit components depends on the specified input/output voltages, power ratings, their accepted deviations and the available space on the board layout. The dimensioning per stage is based on the premise that at the maximum rated power, the sharing between the twin stages is equal.

INDUCTOR SELECTION (L_2 and L_3)

In addition to the parameters listed in the previous section, designing the boost inductors (L_2 and L_3) requires consideration of one more aspect: minimum peak voltage available at the AC input terminals. The boost converter also boosts the minimum peak voltage up to the required output voltage while meeting the load power requirements. The values of the inductor L_2 and L_3 are computed using Equation 19, which are considered as a first approximation of the inductance value.

EQUATION 19:

$$L_2 = L_3 = \frac{V_{in\_min}^{\ 2}\,\eta\,T}{I\%\frac{P_{out\_max}}{2}}\left(\frac{V_{out} - V_{in\_min}\sqrt{2}}{V_{out}}\right)$$

where:

V_{in_min} = Minimum input voltage

V_{out} = Output DC voltage

T = Time period of the PWM switching

P_{out_max} = Maximum output power

η = Efficiency

I% = Ratio of accepted peak to peak inductor current ripple (typical value 20-40%)

For IPFC circuit, I% is assumed to be 40% because ripple cancellation is possible when the two stages are 180º out of phase with respect to each other. For the minimum input voltage (85V), the required output power is 350W at 400 V_{DC}. Equation 18 uses these values and determines the value of L_2 and L_3.

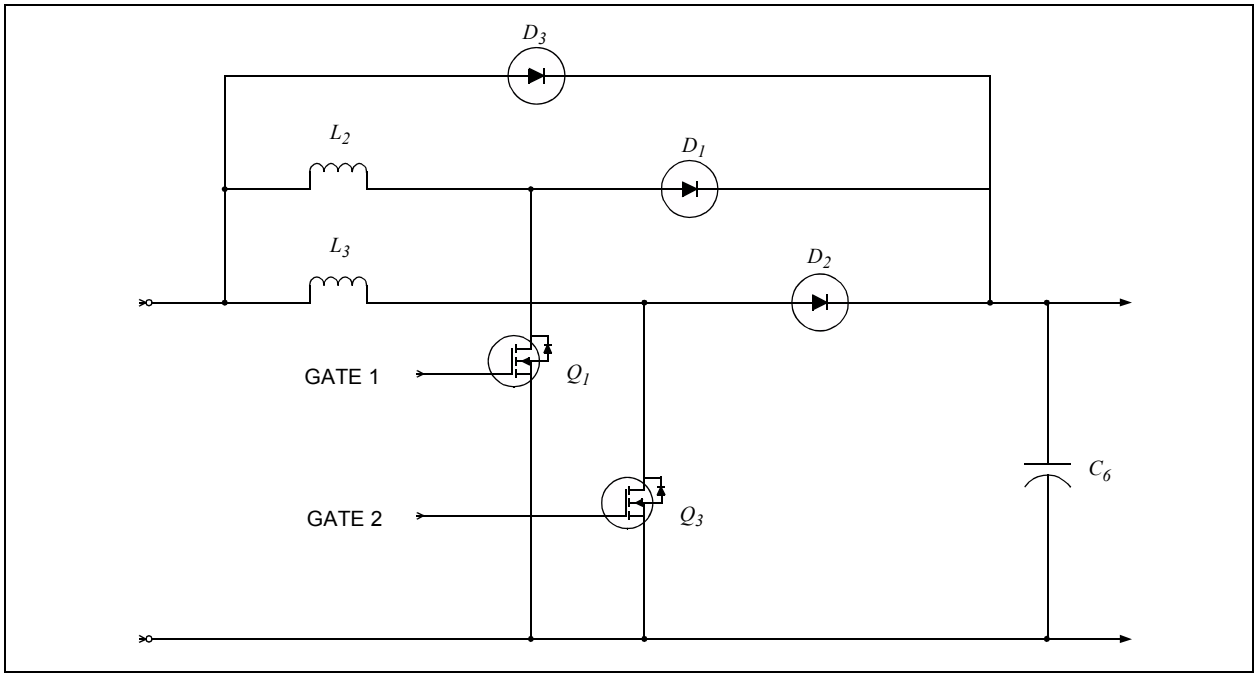
EQUATION 20: INDUCTANCE CALCULATION

$$L_2 = L_3 = \frac{(85)^2\,0.9\,(100\times10^3)^{-1}}{\frac{40}{100}\frac{350}{2}}\left(\frac{400 - 85\sqrt{2}}{400}\right)$$

$$L_2 = L_3 = 649.49\ mH$$

The choice of inductance often depends upon the trade-off between the inductor value and the output current – a low inductance value results in a higher output current and a higher inductance value results in lower output current. If the smallest available value for the inductor is chosen, the MOSFET and output capacitor will have to support a higher current and voltages. Based on the result provided by Equation 20, an inductance of 700 µH is chosen for each boost stage.

FIGURE 18: INTERLEAVED BOOST CONVERTER CIRCUIT



MOSFET SELECTION

The selection of the MOSFETs (Q1 and Q3) depends on the specified output voltage of the IPFC system and the maximum current that will pass through it (i.e., the inductor current). The output voltage (V_{out}) must be lower than V_{DS} rating of the MOSFET, while the inductor current (I_{L1} and I_{L2}) should be lower than the drain current (I_D) rating of the MOSFET. The inductor current can be computed using Equation 21.

EQUATION 21:

$$I_{L2} = I_{L3} = \frac{\sqrt{2}\frac{P_{out\_max}}{2}}{V_{in\_min}\eta}\left(1 + \frac{I\%}{2}\right)$$

where:

P_{out_max} = Maximum output power

V_{in_min} = Minimum input voltage

η = Efficiency

I_{L2}, I_{L3} = Inductance peak current

Equation 22 shows the inductance peak current calculation.

EQUATION 22: INDUCTANCE CURRENT CALCULATION

$$I_{L2} = I_{L3} = \frac{\sqrt{2}\,\frac{350}{2}}{85 \cdot 0.9}\left(1 + \frac{\frac{40}{100}}{2}\right)$$

$$I_{L2} = I_{L3} = 3.88\text{A}$$

DIODE SELECTION (D1 AND D2)

The selection of the diodes (D_1 and D_2) depends on the reverse recovery time (t_{rr}) and reverse voltage value (V_{RRM}). The reverse recovery time determines the switch losses, which become significant at higher commutation frequencies. Because the losses in commutation are proportional with the time spent for each commutation**,** the reverse recovery time should be as small as possible. The diodes D_1 and D_2, having minimum reverse recovery time, are selected. The reverse voltage rating of the selected diodes is higher than the output voltage of the IPFC.

The efficiency of the IPFC denotes the acceptable overall losses. Total power loss also includes losses due to the power semiconductors (i.e., losses in switching and conduction). Equation 23 computes the power loss for the given specifications.

EQUATION 23:

$$P_L = P_{out}\left(\frac{1-\eta}{\eta}\right)$$

where:

P_L = Power loss

η = Efficiency

P_{out} = Output Power

The selection of the power semiconductors, such as the diodes and MOSFETs, also depends on the basic characteristics of the semiconductor device (i.e., voltages and currents Characteristics) and the other features that indicates the losses in conduction or commutation (e.g., reverse recovery time of the diodes and the drain source resistance of MOSFETs).

Equation 22 expresses an approximation of the total semiconductor acceptable losses as being half of the total losses of the IPFC drive.

EQUATION 24:

$$P_{L\_Semi} = \frac{P_L}{2} = \frac{39}{2} = 19.5W$$

where:

P_{L_Semi} = Semiconductor power loss

P_L = Power loss

CAPACITOR SELECTION (C_6)

The selection of the output bulk capacitor (C_6) depends on the acceptable output voltage ripple and the minimum holdup time considered for brown-out conditions. The holdup time (t_{holdup}) is assumed to be 15 ms, which is equivalent of power mains' one semi-period power loss. The capacitance value can be computed using Equation 25.

EQUATION 25:

$$C6 = \frac{2 \cdot P_{out} \cdot t_{hold}}{V_{out} - (V_{out\_min})^2}$$

where:

V_{out_min} = Acceptable output voltage ripple during holdup conditions

t_{hold} = Holdup time

V_{out} = Output Voltage

The Effective Series Resistance (ESR) of the capacitor also affects the output voltage ripple. Therefore, the capacitor with the lowest possible ESR is recommended. The ESR of the capacitor can be lowered by coupling two capacitors in parallel if the board layout dimensions permits. The resultant capacitance of the parallel configuration should be equivalent to the capacitance, C_6. However, the paralleling of the capacitors also results in division of total current ripple. Therefore, it lowers the current ripple specification per capacitor. Equation 26 computes the power loss for the given specifications.

EQUATION 26: CAPACITOR CALCULATION

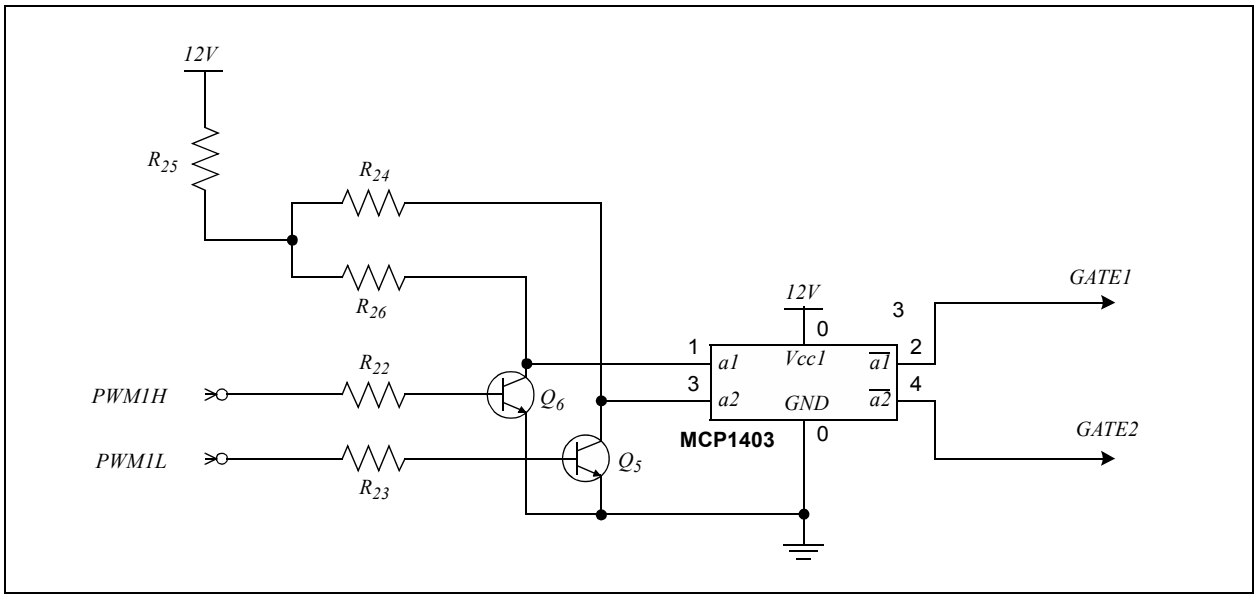
$$C_6 = \frac{2 \cdot 350 \cdot 15e^{-3}}{400 - (350)^2} = 280\ \mu F$$

For this reference design, two 180 µF capacitors were selected and are coupled in parallel.

DIODE SELECTION (D_3)

To limit the start-up inrush current, the diode D_3 should support the charging of the bulk capacitor current and the reverse voltage, which is equal to the output voltage (V_{out}).

FIGURE 19: MOSFET DRIVER CIRCUIT



Signal Adaptation Block

The signal adaptation block consists of all the electric circuitry (active and passive), which interfaces the dsPIC DSC to the power electronics circuitry, such as MOSFET gate signals, analog currents and voltages, filters, and voltage dividers.

MOSFET GATE SIGNAL

The Microchip driver, MCP1403, drives the MOSFET gate signals: GATE1 and GATE2 (see Figure). PWM1H and PWM1L are the output ports of the dsPIC DSC device. When the base of the bipolar transistor (Q6) connected to PWM1H is high, the a1 input of MCP1403 is low. Therefore, the output ($\overline{a1}$) is driven high (connected to GATE 1), and it opens the MOSFET transistor Q1 (see Figure 18). The GATE2 operation is similar to the GATE1 operation.

The signals acquisition includes the voltages and currents measurements. The IPFC system uses the following methods for signal measurement and scaling:

Current Measurement Techniques:

- Shunt Current Measurement
- Current Transformer Measurement

Voltage Measurement Techniques:

- Resistive Divisor Voltage Measurement

SHUNT CURRENT MEASUREMENT

This method measures the total current flowing into the system. In this method, the shunt (R_s) is connected between the two boost stages and the input voltage rectifier. The load current passes through it.

The voltage drop on the shunt resistance is very small. It is amplified by differential amplifier and fed to the analog channel of the ADC. The schematic is built around Microchip's MCP6022 rail-to-rail input/output Op amp, as shown in Figure 5, where I_{Load} designates the total current flowing to the load.

Equation 27 computes the cut-off frequency for the differential mode low-pass filter formed by the RC combination R_{43}, R_{44}, and C_{18}.

EQUATION 27:

$$f_{-3db} = \frac{1}{2 \cdot \pi \cdot (R_{43} + R_{44}) \cdot C_{18}}$$

For this circuit, R_{43} and R_{44} are chosen as 100 Ohms each and C_{18} is chosen as 330 pF. Equation 28 computes the cut-off frequency for the given component values.

EQUATION 28:

$$f_{-3db} = \frac{1}{2 \cdot \pi \cdot (100 + 100) \cdot 333 \times 10^{-12}}$$

$$f_{-3db} = 2.5\ MHz$$

The gain (k) of the circuit, shown in Figure 16, is computed using Equation 29.

EQUATION 29:

$$k = \frac{R_{40}}{R_{38}} = \frac{R_{42}}{R_{39}}$$

with the premise that:

$$\frac{R_{40}}{R_{38}} = \frac{R_{42}}{R_{39}}$$

The gain is chosen such that the output voltage on the analog pin of dsPIC DSC has sufficient tolerance under overcurrent condition and it is set in the range of 0V to 3.3V. Equation 30 can be used to compute the output voltage.

EQUATION 30:

$$V_{ADC\_peak} = k \cdot I_{Load\_max} \cdot R_s$$

Where,

$$I_{Load\_max} = \frac{P_{out\_max} \cdot \sqrt{2}}{P_{in\_max} \cdot \eta}\left(1 + \frac{I\%}{2}\right)$$

where:

V_{ADC_peak} = Maximum voltage on ADC pin

I_{Load_max} = Maximum load current

P_{out_max} = Maximum output power

P_{in_max} = Maximum input power

Equation 31 computes the cut-off frequency for the output low-pass filter formed by the RC combination R_{41} and C_{17}.

EQUATION 31:

$$f_{-3db} = \frac{1}{2 \cdot \pi \cdot R_{41} \cdot C_{17}}$$

The common mode resistors and capacitors should be matched as close as possible. The resistors should have a tolerance of 1% or better, while the capacitors should have a tolerance of 5% or better. For more information, refer to application note AN894 *"Motor Control Sensor Feedback Circuit"* (DS00894).

EQUATION 32:

$$I_{Load\_max} = \frac{350 \cdot \sqrt{2}}{85 \cdot (0.9)}\left(1 + \frac{\frac{40}{100}}{2}\right)$$

$$I_{Load\_max} = 7.76\text{A}$$

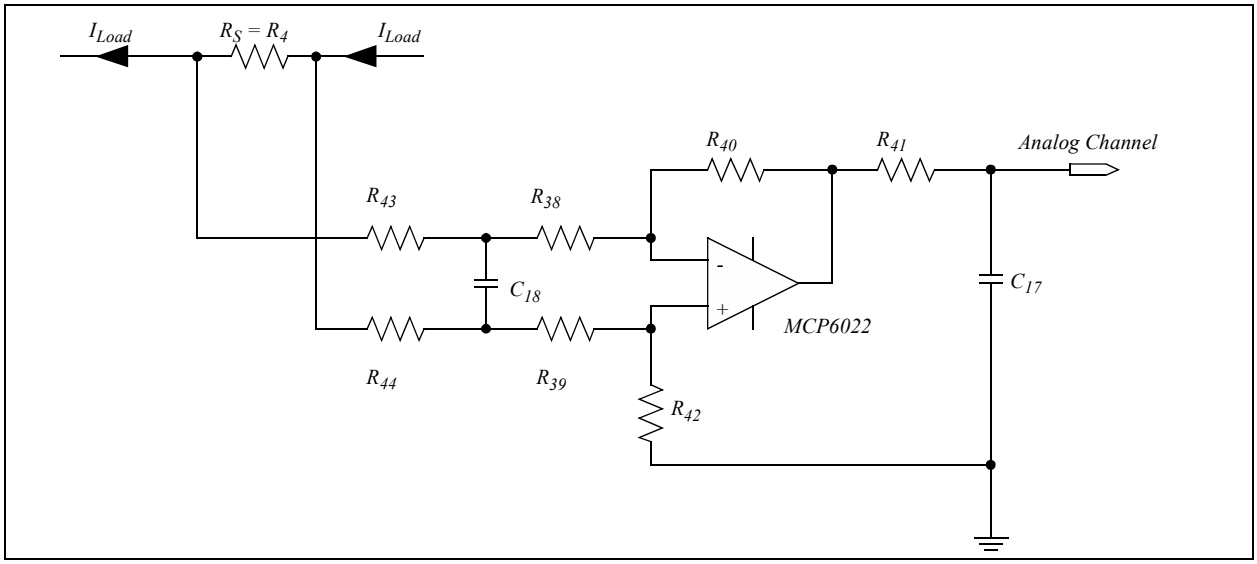
Considering the shunt resistance and amplifier circuit, the gain and the output voltage is computed using Equation 33.

EQUATION 33:

$$k = \frac{15e^{3}}{470} = 32$$

$$V_{ADC\_peak} = 32 \cdot 7.76 \cdot 10e^{-3} = 2.5V$$

FIGURE 20: SHUNT CURRENT MEASUREMENT CIRCUIT



CURRENT TRANSFORMER MEASUREMENT

This method uses a current transformer (CT) to measure the current. It is mounted at the lower side of the switching leg, between the MOSFET transistors and ground (see Figure 18).

This method does not require the amplifier circuitry and offers certain advantages, such as galvanic isolation and cost reduction.

Figure 21 shows the simplified schematic of the current measurement method. The current, I_{Q1}, denotes the current flowing through one of the boost converter legs.

The selection of the CT depends on the number of turns (N) of the secondary of the transformer and the external current sense resistor (R_T). The parameters N and R_T are chosen such that the resulting voltage at the analog pin of the dsPIC DSC has enough tolerance against the overcurrent condition and the voltage is set in the range of 0V to 3.3V. Equation 34 determines the resulting voltage. After the successive iterations, the appropriate values for N and R_T can be determined.

EQUATION 34:

$$V_{ADC\_peak} = \frac{I_{Q1\_max}}{N} \cdot R_T$$

$$I_{Q1\_max} = \frac{\frac{P_{out\_max}}{2} \cdot \sqrt{2}}{V_{in\_max} \cdot \eta}\left(1 + \frac{I\%}{2}\right) = I_{L1} = I_{L2}$$

where:

V_{ADC_peak} = Maximum voltage on ADC pin

I_{Q1_max} = Current through one of the boost converter leg

P_{out_max} = Maximum output power

Typically, the higher the number of turns (N), the better. An increase in the number of turns decreases the power loss due to R_T and increases the volt-time product value. The product, $V * t$ µs, represents the time integral of the series voltages drops on the CT secondary, including the voltage drop on the current sense resistor. Exceeding this product would lead to the CT core saturation, which eventually leads to wrong current measurements. This is overcome by using the reset circuit formed by R_1 and C_1 during the off-time of the MOSFET commutation. It counterbalances the on-time $V * t$ µs. Although, the balancing will not be perfect, it will ensure that the saturation does not occur.

Equation 35 computes the cut-off frequency for the CT output low-pass filter formed by the RC combination R_{13} and C_{10}. It filters any sudden spikes that may occur during switching.

EQUATION 35:

$$f_{-3db} = \frac{1}{2 \cdot \pi \cdot R_{13} \cdot C_{10}}$$

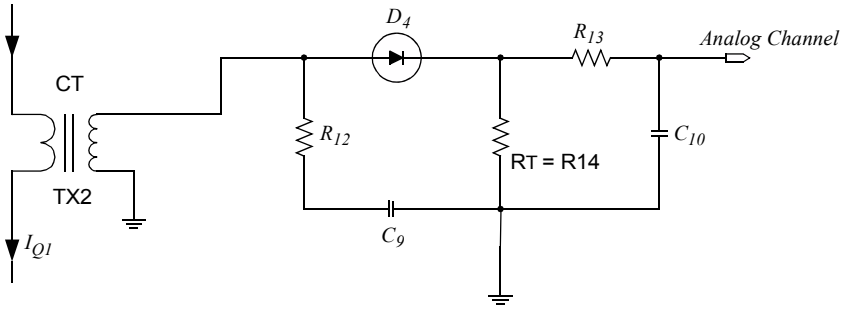
CT Output Voltage Calculation

Equation 36 computes the output voltage of the CT. The terminating resistance (R_T) is chosen as 27Ω and the number of turns (N) ratio is 125.

EQUATION 36:

$$V_{ADC\_peak} = \frac{3.88}{125} \cdot 27 = 0.83V$$

FIGURE 21: CT CURRENT MEASUREMENT



RESISTIVE DIVISOR VOLTAGE MEASUREMENT

The DC bus voltage and AC bus voltage required for the control algorithm are scaled using the voltage divisor shown in Figure 22.

In Figure 22, V_{ACH} and V_{ACL} are connected to the alternative input power lines, so that the peak input voltage is rectified using D_{10} and D_{11}. The resistive divisor formed by R_{35} and R_{37} scales down the power line peak voltage to the ADC input voltage level, which is in the range of 0V to 3.3V. Equation 37 computes the gain of the voltage division.

EQUATION 37:

$$k = \frac{R_{37}}{R_{35} + R_{37}}$$

$$V_{ADC\_peak} = k \cdot V_{in\_max}$$

The capacitor C is used for the signal filtering, but its presence in the circuit is not mandatory. Similarly, the presence of the diode D_3 is not mandatory. The diode D_3 provides protection if the voltage provided to an analog pin of the dsPIC DSC exceeds 3.3V.

At the maximum input voltage, V_{ADC_peak} is computed using Equation 38. For this circuit, R_{35} and R_{37} are chosen as 400 kΩ and 3 kΩ respectively.

EQUATION 38:

$$V_{in\_peak} = V_{in\_max} \cdot \sqrt{2} = 265 \cdot \sqrt{2} = 373.65$$

$$V_{ADC\_peak} = \frac{3}{3 + 400} \cdot 373.65 = 2.78V$$

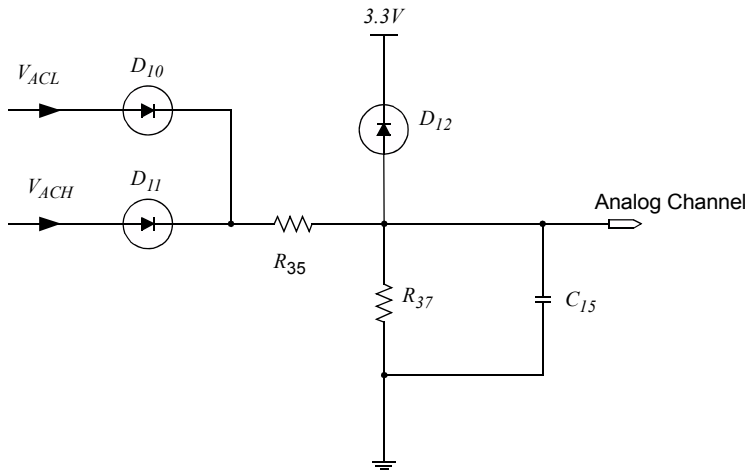
where:

V_{in_peak} = Peak input voltage

V_{ADC_peak} = Maximum voltage on ADC pin

V_{ADC_peak} = Peak voltage on ADC pin

FIGURE 22: VOLTAGE DIVISORS – AC VOLTAGE SENSE



Auxiliary Power Supply Block

The auxiliary power supply is used to drive two voltages:12V and 3.3V. It uses a TNY276P with Flyback topology and can handle input voltages in the universal range.

IPFC INSTALLATION AND CONFIGURATION

Overview of the IPFC Reference Design

The IPFC Reference Design is intended to aid the user in the rapid evaluation and development of Power Factor Correction (PFC) using the dsPIC DSC.

This flexible and cost-effective tool can be configured in different ways for use with Microchip's specialized Switching Mode Power Supply (SMPS) Digital Signal Controllers. The IPFC reference design supports the dsPIC33F motor control device family. It offers a mounting option to connect either a 28-pin SOIC device or a generic 100-pin Plug-In Module (PIM).

The system has two PFC boost circuits to control the power factor. The main components of the system are shown in Figure 1. The rated continuous output current from the system is 1A (rms). This allows up to approximately 350W output when running from an 85 V_{AC} to 265 V_{AC} single-phase input voltage at a maximum ambient temperature of 30ºC (85F).

For more details, refer to **Appendix C: "Electrical Specifications"**. Before using the IPFC system, carefully read the **"IPFC Hardware Design"** section.

KEY FEATURES

The key features of the IPFC Reference Design are:

- Devices Supported:
  - 44-pin to 100-pin dsPIC33FJXXXGSX04 PIM (MA330020) with a dsPIC33F Motor Control device (U9) socket
  - dsPIC33FJ06GS202 Motor Control device in 28-pin QFN-S package (U3) Footprint
- User Interfaces:
  - LED indicators to indicate the following Fault conditions
    - DC bus over-current fault (D14)
    - DC bus over-voltage fault (D17)
    - AC input over-voltage fault (D20)
    - AC input under-voltage fault (D22)
    - VDD Missing Fault (D24)
- LED indicators for Power Supply detection
  - 12V (D33)
  - DC bus (D13)
- Power ON/OFF switch (SW1)
- Minimum load ON/OFF switch (SW2)
- Push button (SW4)
- Push button (SW5)
- Push button (RESET)
- AC inlet connector (J1)
- Output connector (J2)
- Fan connector (FA1/JP11)
- Power supplies output connector (J12)
- Expansion connector (J5)
- RJ-11 connector for programming a dsPIC DSC device (J4), non-isolated
- ICSP™ connector for programming a dsPIC DSC device (J3), non-isolated
- Shunt jumper for internal/external power supply selection (J6)
- Shunt jumper for connecting/disconnecting the
  - DC bus over-current fault (J7)
  - DC bus over-voltage fault (J8)
  - AC input over-voltage fault (J9)
  - AC input under-voltage fault (J10)
  - VDD missing fault (J11)

Power Factor Corrector:

- Implemented using two boost circuits in parallel (interleaved)
- Maximum output power: 350W at 400 V_{DC}
- Maximum input voltage: 85-265 V_{AC}
- Current feedback circuitry
- V_{AC} input voltage sensing
- Zero-crossing detection
- DC bus sensing
- DC bus overcurrent protection
- DC bus overvoltage protection
- V_{AC} input undervoltage protection
- V_{AC} input overvoltage protection

Built-In power supplies

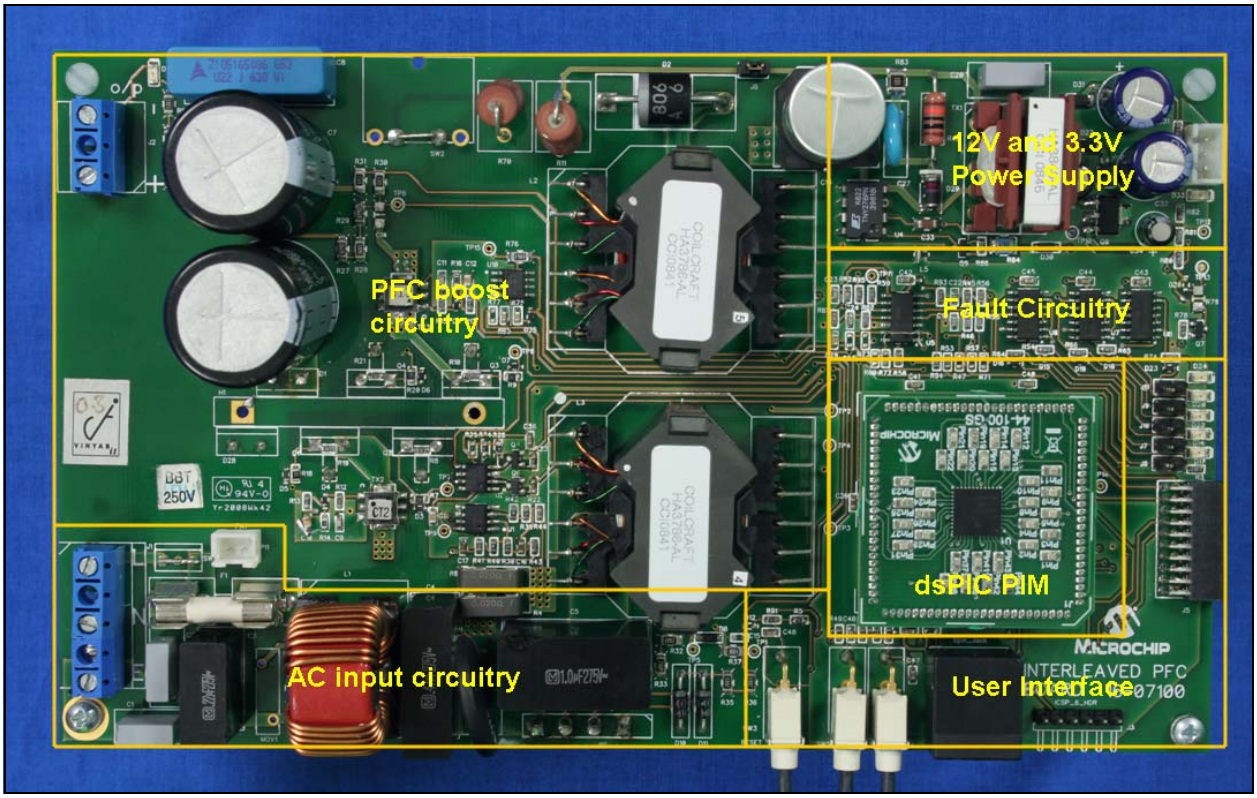
- 12V power supply
- 3.3V power supply

Additional Protection Circuitry

- 250 V_{AC}/10A fuse
- In-rush current limiter
- EMI filter

Figure 23 shows a photograph of the IPFC Reference Design Board with key areas highlighted.

FIGURE 23: IPFC REFERENCE DESIGN BOARD



Getting Started

CONNECTING THE SYSTEM

Caution 1:	When using the IPFC system, the user should be aware of the operating procedures outlined below and ensure that they are followed. Failure to do so may result in damage to the system. Microchip is *not* liable for any damage resulting from such procedures.
2:	Only suitably qualified persons should connect, operate, or service this unit.

It is recommended that cables used for the power connections be terminated with blue or red insulated crimp terminals. If crimp terminals are not used, care should be taken to ensure that stray strands of wire do not short to adjacent terminals or the enclosure. If possible, all wires should be stripped and tinned with solder before connecting to the IPFC reference design terminals.

For the AC mains supply input, standard double-insulated, 3-core flex cable should be used with a minimum current rating of 10A (1 mm^2 18 AWG). A computer power cable can also be used.

Note:	The system is designed for installation category II. Therefore, the incoming mains cable should be wired into a standard non-locking 2-pin + ground type plug.

The recommended output cable size is 1.0 to 1.5 mm^2 (18-16 AWG) and should have a 600V rating. This cable should also be double insulated or have a protective ground screen. Access to the terminal screws is provided via holes in the lid of the enclosure. A slotted screwdriver should be used.

Caution:	The user should only access the power terminals when the system is fully discharged.

The system connections are shown in Table 5 and Figure 24.

FIGURE 24: IPFC REFERENCE DESIGN BOARD CONNECTORS

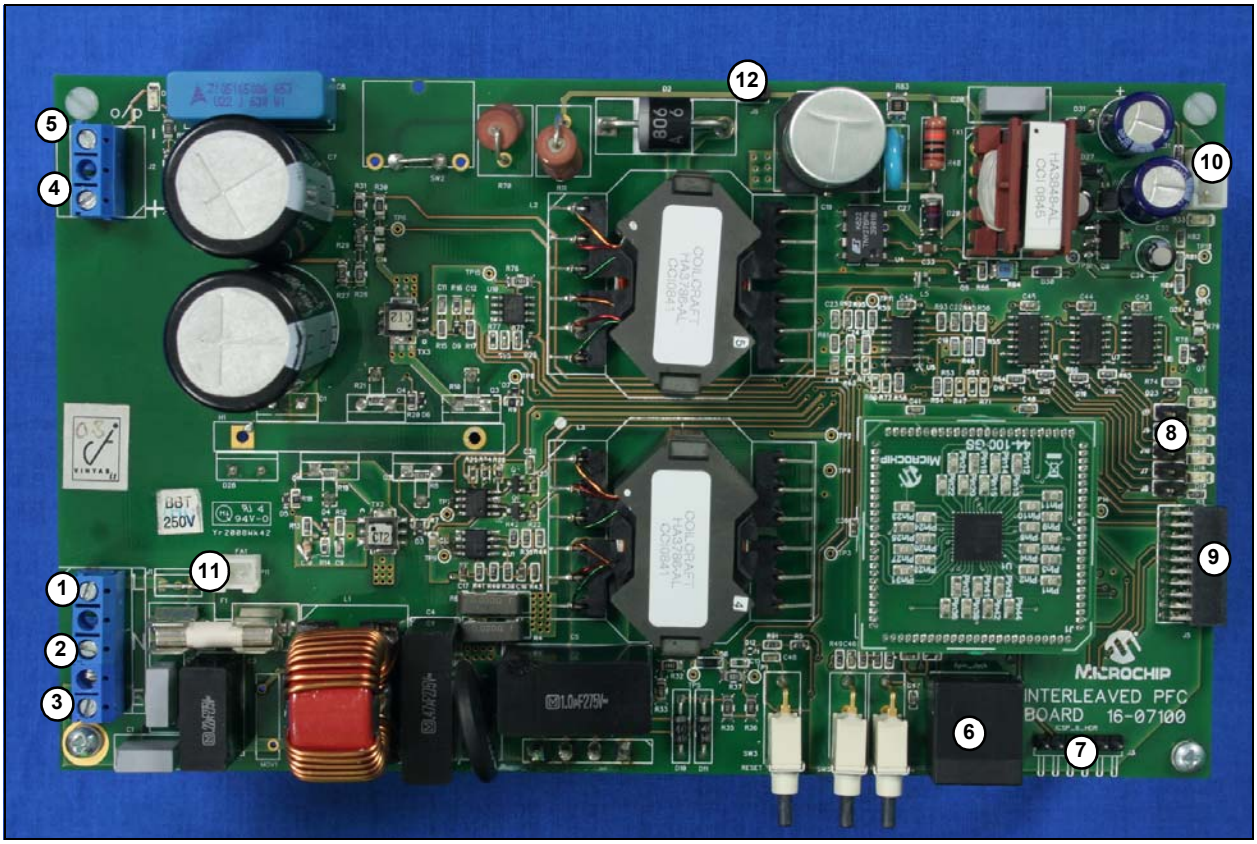


TABLE 5: IPFC REFERENCE DESIGN BOARD CONNECTORS

Number	Connection Name	Type
1	Live (Fused)	Input
2	Neutral	Input
3	Earth Ground	Input
4	DC BUS (+)	Output
5	DC BUS (-)	Output
6	RJ-11 connector for programming a dsPIC® DSC device, non-isolated	Output/Input
7	ICSP™ connector for programming a dsPIC DSC device, non-isolated	Output/Input
8	Fault Selection Headers	Faults
9	Expansion Connector	Output/Input
10	External Power Supplies Connector	Input/Power
11	Fan Connector	Output
12	Power Supply Selection Shunt Jumper	Power

INTERCONNECTING THE HARDWARE

The recommended connection sequence is listed below. The user should ensure that the following sequence is met before connecting the system to the mains.

Note:	Before making any connection verify that the system is not powered and is fully discharged. The system is completely discharged when the LED D13 is OFF.

To set up the system, complete the following steps:

1. Connect the load to the DC BUS (+) and DC BUS (-) output terminals.
2. Make sure that the power cord is disconnected from the AC mains before connecting it to the IPFC reference design AC input connector.
3. Connect the power cord to the Interleaved AC inlet.
4. Connect the power cord to the mains.

Power-up Sequence

To power-up the IPFC system, complete the following steps:

1. Connect the power cable to the AC mains.
2. Turn-on the incoming AC supply by sliding the switch SW1 to the ON position.
3. Check the status of the D13 and D33 LEDs. The unit is powered when these LEDs are ON.

Power-down Sequence

To disconnect the power supply to the IPFC system, complete the following steps:

1. Turn off the incoming AC supply by sliding the switch SW1 to the OFF position.
2. Wait until the red DC bus LED indicator (D13) turns OFF. This can take a maximum of 5 minutes.
3. Disconnect the power cord from mains.

PROGRAMMING/DEBUGGING AN APPLICATION CODE

The MPLAB® ICD 2, MPLAB IDC 3, PICkit™ 3 and MPLAB REAL ICE™ in-circuit emulator may be used along with MPLAB IDE to debug your software. MPLAB IDE is the free integrated development environment available from Microchip's web site. MPLAB IDE allows these two devices, which are supported on the IPFC Reference Design, to be used as an in-circuit debugger as well as a programmer:

- dsPIC33FJ06GS202
- dsPIC33FJ16GS504

In-circuit debugging allows you to run, examine, and modify your program for the device embedded in the IPFC system hardware. This greatly assists you in debugging your firmware and hardware together.

Special software interacts with the MPLAB IDE application to run, stop, and single-step through programs. Breakpoints can be set and the processor can be reset. Once the processor is stopped, the register's contents can be examined and modified.

For more information on how to use MPLAB IDE, refer to the following documentation:

- *"MPLAB® IDE User's Guide"* (DS51519)
- *"MPLAB® IDE Quick Start Guide"* (DS51281)
- MPLAB® IDE Help File

Note:	The programming connectors used for connecting the MPLAB programmers/ debuggers are not isolated. The user should use an isolation method, such as an isolated USB HUB.

SETTING UP AN APPLICATION FOR DEBUG

Complete the following steps to prepare the application for debug:

1. Launch MPLAB IDE, and then open the application project. The related workspace will be open. For information on projects and workspaces, see the MPLAB IDE documentation mentioned at the beginning of this section.
2. Select *Project>Build All* to build the application code. The build's progress will be visible in the **Build** tab of the Output window.
3. Select *Debugger>Select Tool>"Your Preferred Tool"*. MPLAB IDE will change to add your tool debug features.
4. Select *Debugger>Program* to program the application code into the dsPIC33F DSC device. The debug programming progress will be visible in the **Debugging tool** tab of the Output window.

PROGRAMMING AN APPLICATION

When the program is successfully debugged and running, the next step is to program the device for standalone operation in the finished design. When doing this, the resources reserved for debug are released for use by the application. To program the application, use the following steps:

1. Disable your tool as a debug tool by selecting *Debugger>Select Tool>None*.
2. Select your tool as the programmer by selecting *Programmer>Select Programmer menu*.
3. Select *Programmer>Program*.

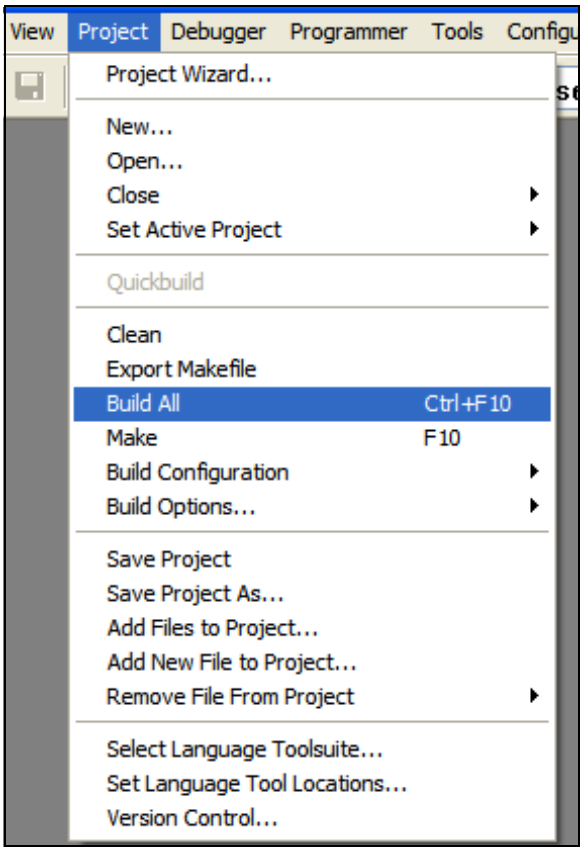
Now the application code will run independently.

Running the Demonstration Software

To run the demonstration, complete the following steps:

1. On the IPFC Reference Design Board, make sure that the shunt jumper J6 is mounted.
2. Make sure that the dsPIC33FJ16GS504 PIM (MA330020) is mounted on the IPFC Reference Design Board.
3. Connect the load to the DC BUS (+) and DC BUS (-). For details, refer to **"Connecting the System"**.
4. Power-on the IPFC reference design board, applying only 50V AC. For details, refer to **"Power-up Sequence"**.
5. Open the IPFC demonstration software by double-clicking the `.mcw` file.
6. After the MPLAB IDE work-bench is open, Compile the project. Build the project using the "Build All" option from the "Project" drop-down menu. (see Figure 25).

FIGURE 25: COMPILING CODE IN MPLAB® IDE



7. Select the programmer from the "Programmer" drop down menu. In this case select the MPLAB REAL ICE or any of the other shown options. (see Figure 26).

FIGURE 26: PROGRAMMER SECTION IN MPLAB® IDE

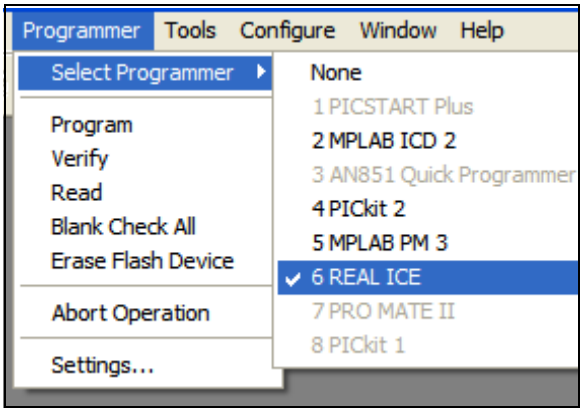
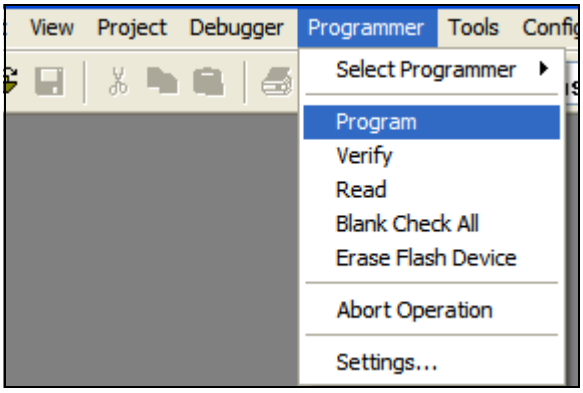


FIGURE 27: PROGRAMMING OPTIONS IN MPLAB® IDE



8. Connect the programming tool to the IPFC Reference Design Board using the RJ-11 connector, and then program the device using *Programmer>Program*. Next, disconnect the debugger from the board (see Figure 27).

Note: The programming connectors used for connecting the MPLAB programmers/debuggers are not isolated. User should use an isolation method, such as an isolated USB HUB.

9. Remove the programmer/debugger.
10. Increase the input voltage to the desired value within the input range of 85-265V AC.

The IPFC Reference Design Board should now be up and running.

CONCLUSION

This application note presents the novel method of Interleaved Power Factor Correction (IPFC) using the dsPIC DSC. It explains in detail the digital design and implementation of an IPFC converter including the hardware consideration and MATLAB simulations.

This unique approach can be used to design and integrate other downstream converters following the IPFC stage. The power control-related peripherals, such as ADC, PWM, and Analog Comparators can be used for the other converter stages as well.

The modular design of the software makes it easier to append other functions necessary to meet the needs of the specific application. The dsPIC DSC devices, with their high processing power and peripheral-rich platform, are well suited for development of such complex applications on a single chip. Multiple control loops running with different timing requirements can be executed using the variety of DSP instructions. In addition, the Data Monitor and Control Interface (DMCI) feature available in the MPLAB Integrated Development Environment (IDE) can be used to control and display the application variables while the application is running. This aids in observing various signals during the software development phase.

Microchip has various resources to assist you in developing this integrated application. For more details on the IPFC Reference Design, please contact your local Microchip Sales office.

REFERENCES

The following application notes have been published by Microchip Technology Inc., which describe the use of dsPIC DSC devices for power conversion applications:

- AN1106 *"Power Factor Correction in Power Conversion Applications Using the dsPIC® DSC"* (DS01106)
- AN1208 *"Integrated Power Factor Correction (PFC) and Sensorless Field Oriented Control (FOC) System"* (DS01208)

These documents are available for download from the Microchip web site (**www.microchip.com**).

APPENDIX A: SOURCE CODE

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All of the software covered in this application note is available as a single WinZip archive file. This archive can be downloaded from the Microchip corporate Web site at:

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APPENDIX B: SYMBOL GLOSSARY

TABLE B-1: SYMBOLS AND DESCRIPTIONS

Symbol	Description
V_{AC}	Rectified AC Voltage
I_{AC}	Rectified AC Current
V_{DC}	DC Bus Voltage
V_{DCREF}	DC Bus Reference Voltage
I_{ACREF}	Capacitor Current Reference
R_{max}	Maximum Resistance
V_{max}	Maximum Voltage
I_{max}	Maximum Current
σ_{max}	Maximum Conductance
Ga	Proportional Gain for Voltage Error Compensator
Gsa	Integral Gain for Voltage Error Compensator
BW_{VLoop}	Voltage Loop Bandwidth
IBW_{VLoop}	Integral Voltage Loop Bandwidth
f_{VLoop}	Voltage Control Loop Frequency
Ra	Proportional Gain for Current Error Compensator
Rsa	Integral Gain for Current Error Compensator
BW_{ILoop}	Current Loop Bandwidth
IBW_{ILoop}	Integral Current Loop Bandwidth
f_{ILoop}	Current Control Loop Frequency
Ka	Proportional Gain for Load Balance Error Compensator
Ksa	Integral Gain for Load Balance Error Compensator
BW_{LBLoop}	Load Balance Loop Bandwidth
IBW_{LBLoop}	Integral Load Balance Loop Bandwidth
f_{LBLoop}	Load Balance Control Loop Frequency
V_{AVG}	Average Value of the Rectified Input Voltage
V_L	Inductor Voltage obtained from the current error compensator
D	Main Duty cycle
$D1$	Duty Cycle of MOSFET1
$D2$	Duty Cycle of MOSFET2
Dd	Main Duty cycle
DD	Correction in Duty Cycle
$E_{Singlestage}$	Energy stored in a single stage PFC converter
$E_{Interleaved}$	Energy stored in a IPFC converter
K_i	Proportional Gain
K_v	Integral Gain
V_{in_min}	Minimum input voltage
V_{out}	Output DC voltage
T	Time period of the PWM switching
P_{out_max}	Maximum output power
h	Efficiency
$I\%$	Ratio of accepted peak to peak inductor current ripple (typical value 20-40%)

TABLE B-1: SYMBOLS AND DESCRIPTIONS (CONTINUED)

Symbol	Description
t_{hold}	Holdup time
t_{rr}	Reverse recovery time
V_{RRM}	Reverse voltage value
V_{out_min}	Minimum output voltage
ESR	Effective series resistance
V_{ADC_peak}	Maximum voltage on ADC pin
T	Time period of the PWM switching
P_{out_max}	Maximum output power
h	Efficiency
$I\%$	Ratio of accepted peak-to-peak inductor current ripple (typical value 20-40%)
t_{hold}	Holdup time
t_{rr}	Reverse recovery time
V_{RRM}	Reverse voltage value
V_{out_min}	Minimum output voltage
ESR	Effective series resistance
V_{ADC_peak}	Maximum voltage on ADC pin
V_{in_peak}	Input Peak Voltage
V_{in_max}	Maximum Input Voltage
I_{Q1max}	Current flowing through Boost Converter Leg
L	Effective Boost Inductance
C	Effective Boost Capacitance
I_{M1}	MOSFET1 current
I_{M2}	MOSFET2 current
V_{ERR}	Voltage Error
I_{CAPREF}	Capacitor Current Reference
I_{INDREF}	Inductor Current Reference
I_{ERR}	Current Error
V_{IND}	Inductor Current
V_L	Inductor Voltage obtained from the current error compensator
I_C	Current through Output Capacitor
I_D	Diode Current
t_{ON}	ON time of the MOSFET
t_{OFF}	OFF time of the MOSFET
V_{DCREF}	Reference DC Voltage
V_{DC}	Sensed DC Voltage
I_{Load}	Load Current
I_{Load_max}	Maximum Load Current
I_{ACREF}	Reference current signal
V_m	Peak voltage of half sine wave
V_{avg}	Average voltage
V_L	Inductor voltage

APPENDIX C: ELECTRICAL SPECIFICATIONS

The IPFC Reference Design was tested at a maximum power of 350W with resistive and a three-phase inverter type load.

TABLE C-1: ELECTRICAL SPECIFICATIONS

Parameter	Minimum	Typical Values at 120 V_{AC} Input 400 V_{DC} Output 350W Output	Typical Values at 230 V_{AC} Input 400 V_{DC} Output 350W Output	Maximum
Input Voltage	85 V_{AC}	120 V_{AC}	230 V_{AC}	265 V_{AC}
Input Current	—	3.17A	1.6A	8A
Input Power	—	380W	368W	400W
Output Voltage	—	400 V_{DC} ± 2%	400 V_{DC} ± 2%	420 V_{DC}
Output Current	—	0.87A	0.87A	2A
Output Power	—	350W	350W	350W
Heatsink at 25ºC Ambient Temperature	—	70ºC(1)	48ºC(1)	75ºC(2)
ITHD	—	3%	5%	—
Power Factor	—	0.998	0.992	—
Efficiency	—	92%	95%	—

Note 1: When using a heatsink with a thermal resistance of 6ºC/W, the heatsink temperature stabilizes at this value for continuous operation.

2: The temperature was measured on the heatsink after one hour of operation at a minimum input voltage of 85 V_{AC} and maximum output power of 350W at 400 V_{DC}. No fan was utilized. If the user requires full duty cycle operation under these conditions, an external fan is recommended to keep the heatsink temperature below 75ºC.

APPENDIX D: SCHEMATICS AND BOARD LAYOUT

FIGURE D-1: IPFC REFERENCE DESIGN SCHEMATIC (SHEET 1 OF 3)

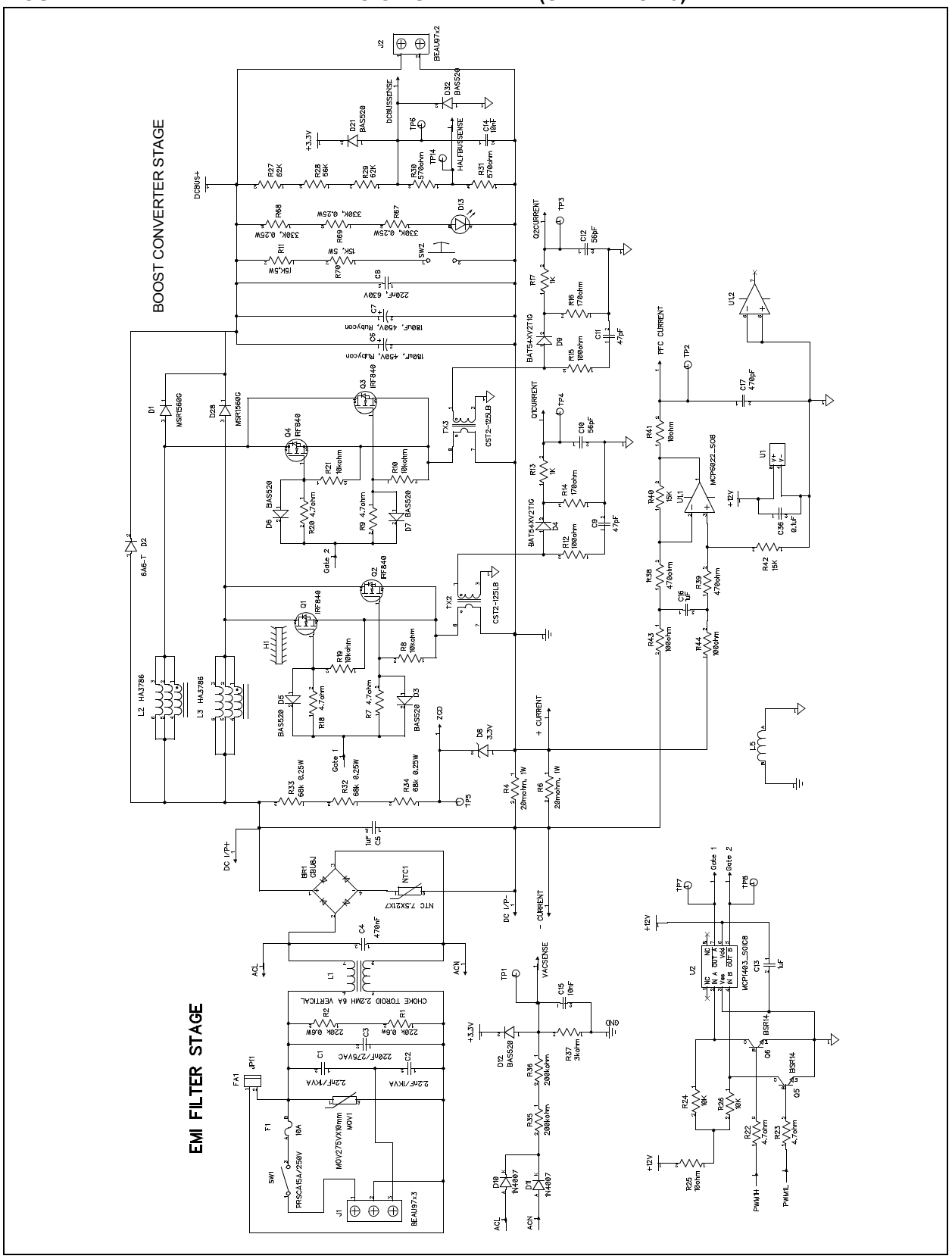


FIGURE D-2: IPFC REFERENCE DESIGN SCHEMATIC (SHEET 2 OF 3)

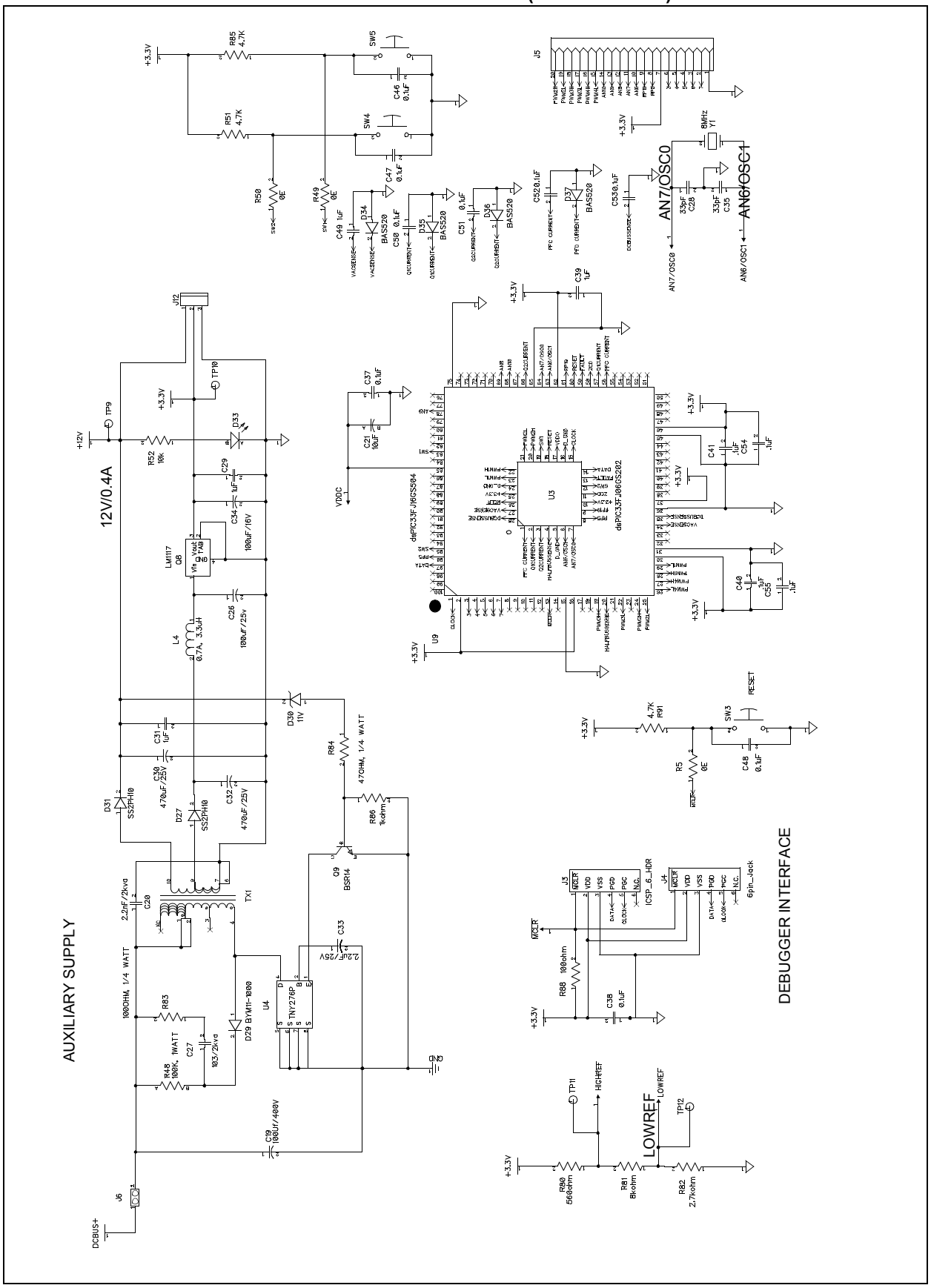


FIGURE D-3: IPFC REFERENCE DESIGN SCHEMATIC (SHEET 3 OF 3)

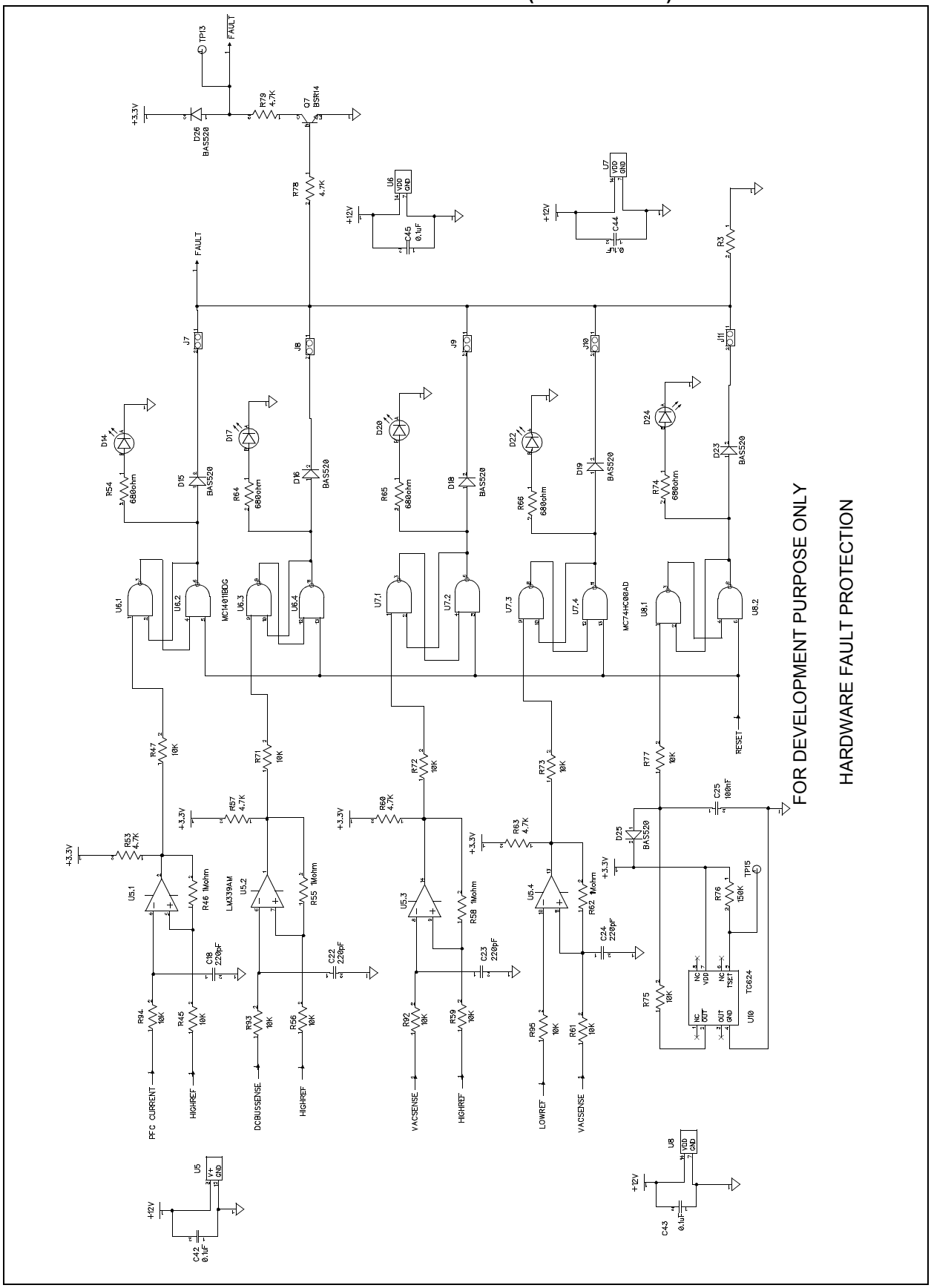
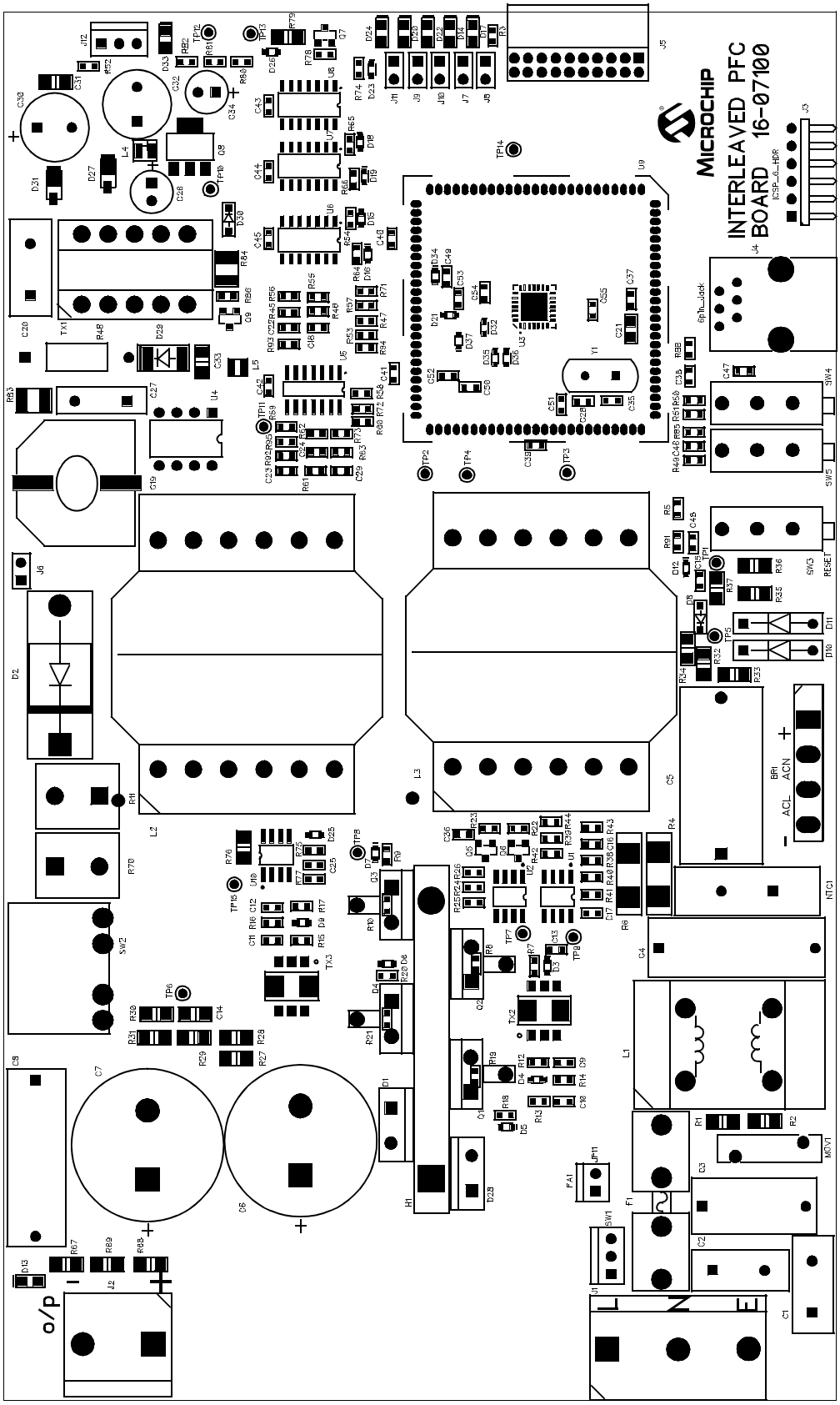


FIGURE D-4: IPFC REFERENCE DESIGN BOARD LAYOUT (TOP)



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Japan - Yokohama
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Korea - Seoul
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Malaysia - Kuala Lumpur
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Malaysia - Penang
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Philippines - Manila
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