
Power Factor Correction in Power Conversion Applications Using the dsPIC[®] DSC

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INTRODUCTION

Most of the power conversion applications consist of an AC-to-DC conversion stage immediately following the AC source. The DC output obtained after rectification is subsequently used for further stages.

Current pulses with high peak amplitude are drawn from a rectified voltage source with sine wave input and capacitive filtering. The current drawn is discontinuous and of short duration irrespective of the load connected to the system.

Since many applications demand a DC voltage source, a rectifier with a capacitive filter is necessary. However, this results in discontinuous and short duration current spikes. When this type of current is drawn from the mains supply, the resulting network losses, the total harmonic content, and the radiated emissions become significantly higher. At power levels of more than 500 watts, these problems become more pronounced.

Two factors that provide a quantitative measure of the power quality in an electrical system are Power Factor (PF) and Total Harmonic Distortion (THD). The amount of useful power being consumed by an electrical system is predominantly decided by the PF of the system.

Benefits from improvement of Power Factor include:

- Lower energy and distribution costs
- Reduced losses in the electrical system during distribution
- Better voltage regulation
- Increased capacity to serve power requirements

This application note focuses primarily on the study, design and implementation of Power Factor Correction (PFC) using a Digital Signal Controller (DSC). The software implementation of PFC using the 16-bit fixed point dsPIC[®] DSC is explained in detail. The discretization of the error compensators, along with a design example is covered as well. In conclusion, some laboratory test results and waveforms are presented to validate the digital implementation of the PFC converter.

The low cost and high performance capabilities of the DSC, combined with a wide variety of power electronic peripherals such as an Analog-to-Digital Converter (ADC) and a Pulse Width Modulator (PWM), enable the digital design and development of power related applications to be simpler and easier.

Some advantages of using a digital implementation for PFC are:

- Easy implementation of sophisticated control algorithms
- Flexible software modifications to meet specific customer needs
- Simpler integration with other applications

SIGNIFICANCE OF POWER FACTOR IN POWER AND CONTROL SYSTEMS

To understand PF, it is important to know that power has two components:

- Working, or Active Power
- Reactive Power

Working Power is the power that is actually consumed and registered on the electric meter at the consumer's location. It performs the actual work such as creating heat, light and motion. Working power is expressed in kilowatts (kW), which registers as kilowatt hour (kWh) on an electric meter.

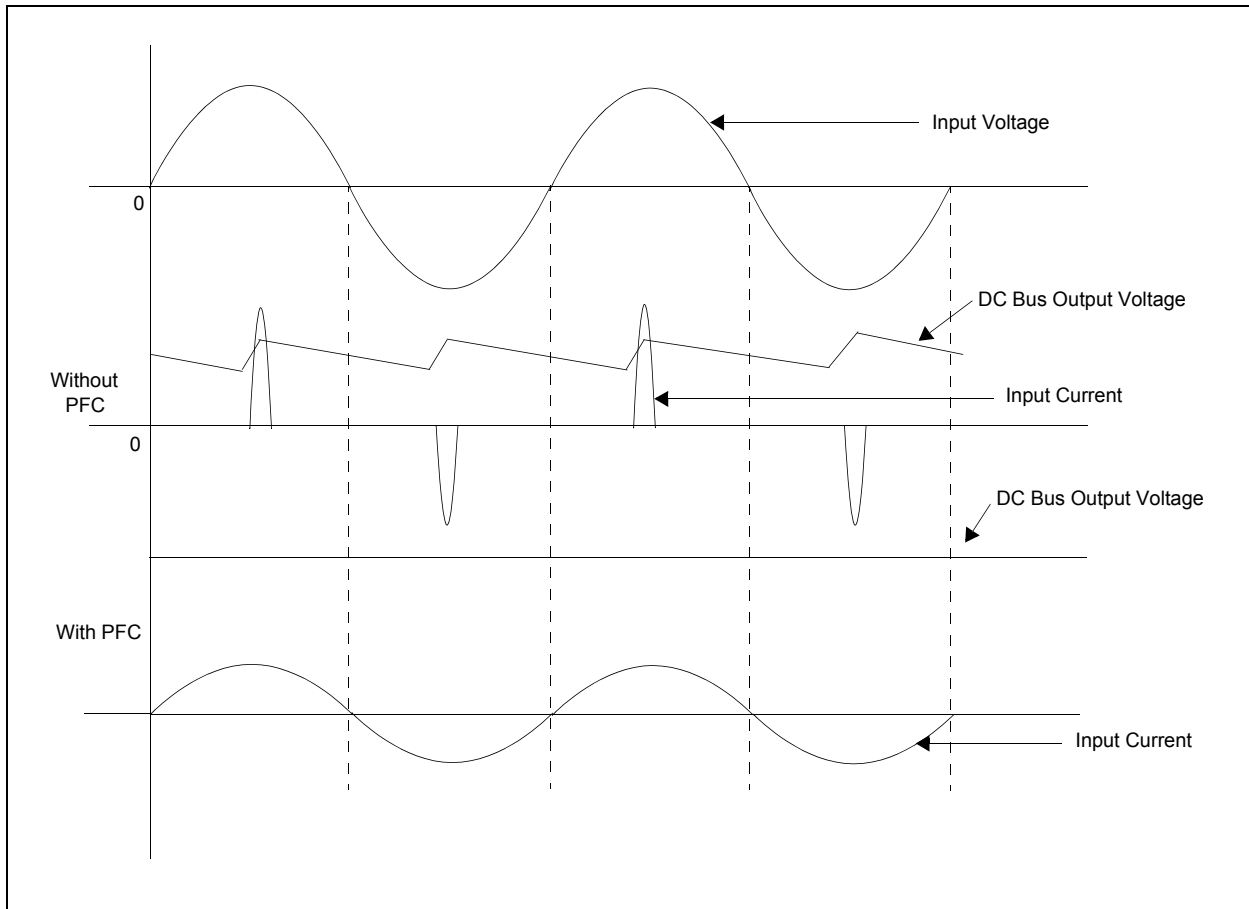
Reactive Power does no useful work, but is required to maintain and sustain the electromagnetic field associated with the industrial inductive loads such as induction motors driving pumps or fans, welding machines and many more. Reactive Power is measured in kilovolt ampere reactive (kVAR) units.

The total required power capacity, including Working Power and Reactive Power, is known as Apparent Power, expressed in kilovolt ampere (kVA) units.

Power Factor is a parameter that gives the amount of working power used by any system in terms of the total apparent power. Power Factor becomes an important measurable quantity because it often results in significant economic savings.

Typical waveforms of current with and without PFC are shown in Figure 1.

FIGURE 1: CURRENT WAVEFORMS WITH AND WITHOUT PFC



These waveforms illustrate that PFC can improve the input current drawn from the mains supply and reduce the DC bus voltage ripple.

The objective of PFC is to make the input to a power supply look like a simple resistor. This allows the power distribution system to operate more efficiently, reducing energy consumption.

The Power Factor is equal to Real Power divided by Apparent Power, as shown in Equation 1.

EQUATION 1: POWER FACTOR

$$\text{Power Factor} = \text{Real Power} / \text{Volt} \times \text{Ampere}$$

When the ratio deviates from a constant, the input contains phase displacement, harmonic distortion or both, and either one degrades the Power Factor.

The remaining power that is lost as Reactive Power in the system is due to two reasons:

- Phase shift of current with respect to voltage, resulting in displacement
- Harmonic content present in current, resulting in distortion

These two factors define Displacement Factor and Distortion Factor, which provide the Power Factor as shown in Equation 2. The amount of displacement between the voltage and current indicates the degree to which the load is reactive.

EQUATION 2: POWER FACTOR

Power Factor = Displacement Factor x Distortion Factor

$$\text{PowerFactor} = \underbrace{\cos\phi}_{\text{Displacement Factor}} \cdot \underbrace{\frac{1}{\sqrt{1 + (I_2/I_1)^2 + (I_3/I_1)^2 + \dots}}}_{\text{Distortion Factor}} = \frac{\cos\phi}{\sqrt{1 + THD^2}}$$

$$THD = \sqrt{1 + (I_2/I_1)^2 + (I_3/I_1)^2 + \dots}$$

where:

$\cos\phi$ = Displacement factor of the voltage and current

THD = Total Harmonic Distortion

I_1 = Current drawn from the supply at fundamental frequency

I_2 = Current drawn from the supply at double the fundamental frequency and so on

Harmonic Content

Current harmonics are sinusoidal waves that are integral multiples of the fundamental wave. They appear as continuous, steady-state disturbances on the electrical network. Harmonics are altogether different from line disturbances, which occur as transient distortions due to power surges.

SOURCES OF CURRENT HARMONICS

Some of the prominent sources that cause current harmonics distortion are:

- Power Electronic Equipment (rectifiers, UPS systems, variable frequency drives, state converters, thyristor systems, switch mode power supplies, SCR controlled systems, etc.)
- Auxiliary Equipment (welding machines, arc furnaces, mercury vapor lamps, etc.)
- Saturable Inductive Equipment (generators, motors, transformers, etc.)

PROBLEMS CREATED BY CURRENT HARMONICS

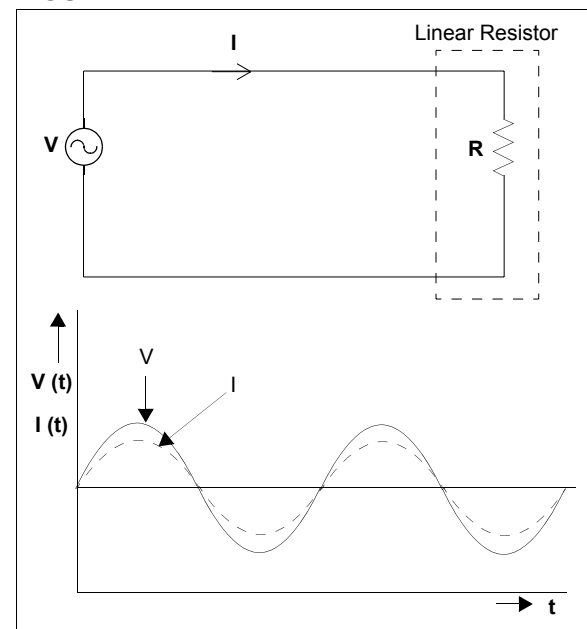
Problems created by current harmonics include, but are not limited to:

- Erroneous operation of control system components
- Damage to sensitive electronic equipment
- Nuisance tripping of circuit breakers and blowing fuses
- Excessive overheating of capacitors, transformers, motors, lighting ballasts and other electrical equipment
- Interference with neighboring electronic equipment

To reduce these problems of current harmonics, the current drawn from the input needs to be shaped similar to that of voltage wave profile. The Total Harmonic Distortion (THD) is shown in Equation 2.

PFC aims at improving the displacement and distortion factors to derive maximum Real Power from the supply. This is done by reducing the losses that occur in the system due to the presence of reactive elements, resulting in the improvement of power quality and overall efficiency of the system.

When the power converter is fed from a voltage source, and by making the power converter appear as a linear resistance to the supply voltage, the input current wave shape can be made to follow the input voltage wave shape. For example, if the input voltage (V) is in the form of a sine wave, input current (I) is the same as that shown in Figure 2.

FIGURE 2:

HOW TO MAKE THE POWER CONVERTER LOOK RESISTIVE

Despite having reactive passive elements like inductors, capacitors and active switching elements like MOSFETs and IGBTs, how can we make the converter appear to be resistive to the supply voltage?

The answer to this question lies in the fact that PFC is a low-frequency requirement. Therefore, the converter need not be resistive at all frequencies, provided a filtering mechanism exists to remove the high-frequency ripples.

The basic elements present in a converter are an inductor (L) and a capacitor (C), which are zero order elements. This means that these elements cannot store energy in a single switching cycle due to their fundamental properties:

- An inductor cannot take a sudden change in current. This makes it a cut set with an open switch and a periodic current source, as shown in Figure 3.
- A capacitor cannot take a sudden change in voltage. This makes it a closed circuit with a closed switch and a periodic voltage source, as shown in Figure 4.

FIGURE 3: SUDDEN CHANGE IN CURRENT

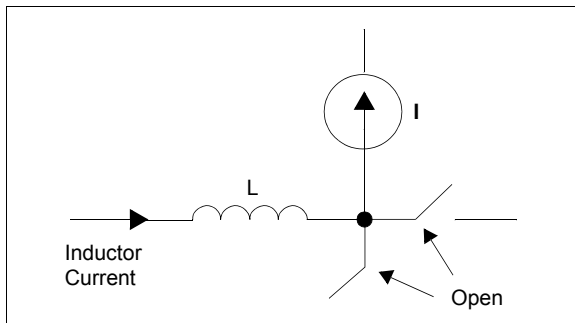
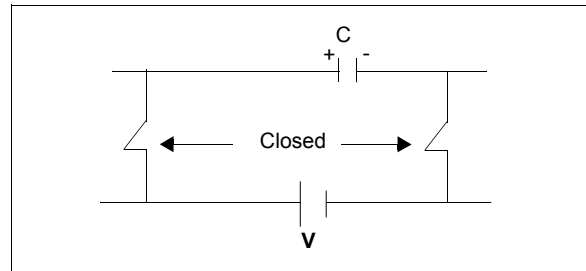


FIGURE 4: SUDDEN CHANGE IN VOLTAGE



Active PFC must control both the input current and the output voltage. The current is shaped by the rectified line voltage so that the input to the converter appears to be resistive. The output voltage is controlled by changing the average amplitude of the current programming signal.

Figure 3 and Figure 4 show the two fundamental properties that lead to the following conclusions:

- The two elements, inductor and capacitor, can be considered to be resistive in the low frequency range.
- The current through the inductor can be programmed in such a way that it follows the supply voltage and assumes the same wave shape as that of the voltage. To achieve this, different strategies are used for implementing PFC.

The effective resistance of the resistive load specified to the AC line varies slowly according to the power demands of the actual load. The line current remains proportional to the line voltage, but this proportionality constant varies slowly over a number of line cycles.

THEORETICAL BACKGROUND ON PFC STRATEGIES

In a DSC-based application, the relevant analog parameters and the control loops need to be redefined and discretized. This enables changeover from existing hardware to its digital counterpart easier and more logical.

The basic function of PFC is to make the input current drawn from the system sinusoidal and in-phase with the input voltage. Figure 5 shows the component blocks required for PFC and the PFC stage interfaced to a dsPIC device. This is an AC-to-DC converter stage, which converts the AC input voltage to a DC voltage and maintains sinusoidal input current at a high input Power Factor. As indicated in the block diagram, three input signals are required to implement the control algorithm.

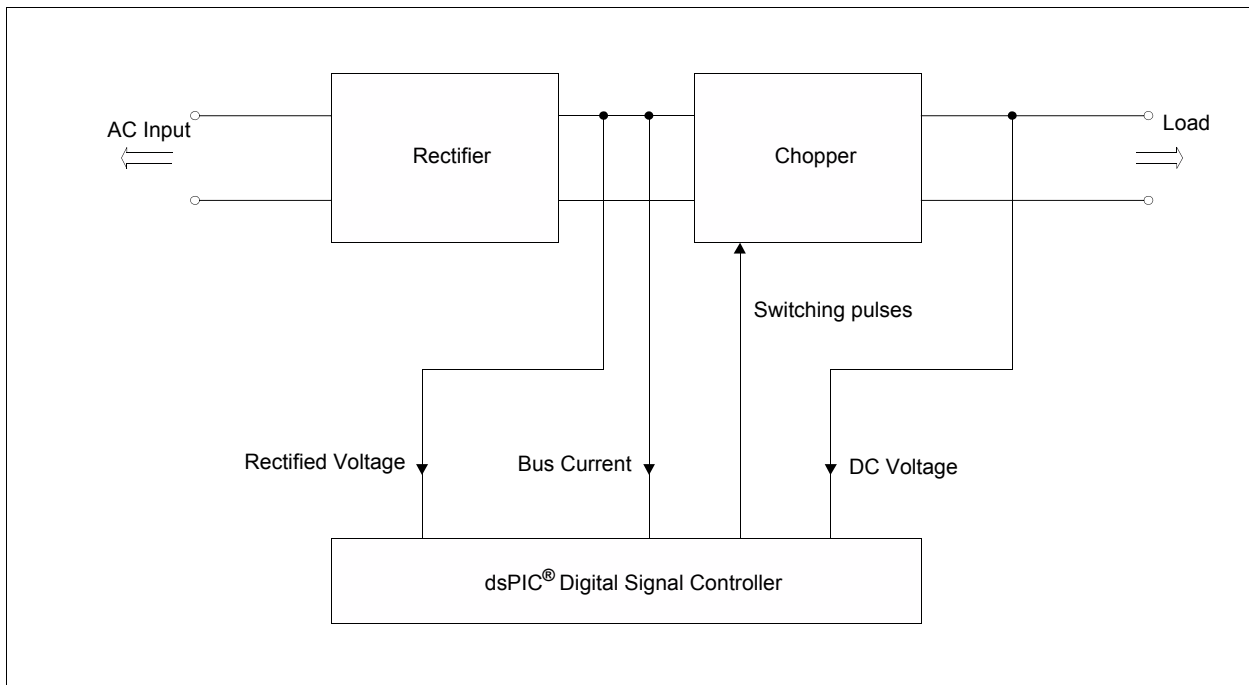
The input rectifier converts the alternating voltage at power frequency into unidirectional voltage. This rectified voltage is fed to the chopper circuit to produce a smooth and constant DC output voltage to the load.

The chopper circuit is controlled by the PWM switching pulses generated by the dsPIC device, based on three measured feedback signals:

- Rectified input voltage
- Rectified input current
- DC bus voltage

The various topologies for active PFC are based on the block diagram shown in Figure 5.

FIGURE 5: BLOCK DIAGRAM OF THE COMPONENTS FOR POWER FACTOR CORRECTION



POWER FACTOR CORRECTION TOPOLOGIES

Boost PFC Circuit

The boost converter produces a voltage higher than the input rectified voltage, thereby giving a switch (MOSFET) voltage rating of V_{OUT} . Figure 6 shows the circuit for the boost PFC stage. Figure 7 shows the boost PFC input current shape.

FIGURE 6: BOOST PFC

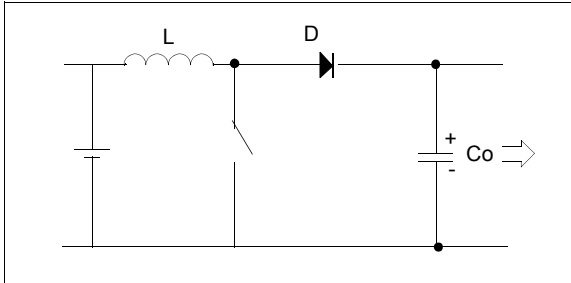
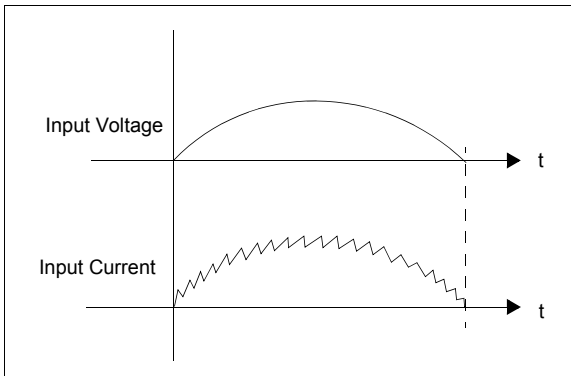


FIGURE 7: BOOST PFC INPUT CURRENT SHAPE



Buck PFC Circuit

In a buck PFC circuit, the output DC voltage is less than the input rectified voltage. Large filters are needed to suppress switching ripples and this circuit produces considerable Power Factor improvement. The switch (MOSFET) is rated to V_{IN} in this case. Figure 8 shows the circuit for the buck PFC stage. Figure 9 shows the buck PFC input current shape.

FIGURE 8: BUCK PFC

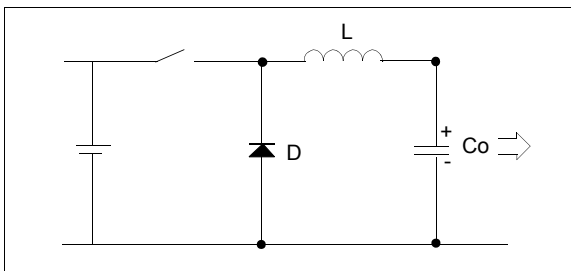
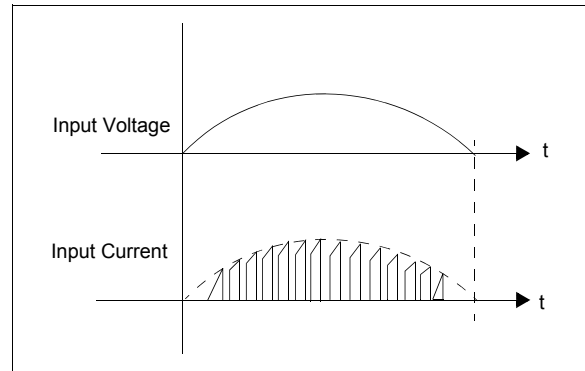


FIGURE 9: BUCK PFC INPUT CURRENT SHAPE



Buck/Boost PFC Circuit

In the buck/boost PFC circuit, the output DC voltage may be either less or greater than the input rectified voltage. High Power Factor can be achieved in this case. The switch (MOSFET) is rated to $(V_{IN} + V_{OUT})$. Figure 10 shows the circuit for the buck/boost PFC stage. Figure 11 shows the buck/boost PFC input current shape.

FIGURE 10: BUCK/BOOST PFC

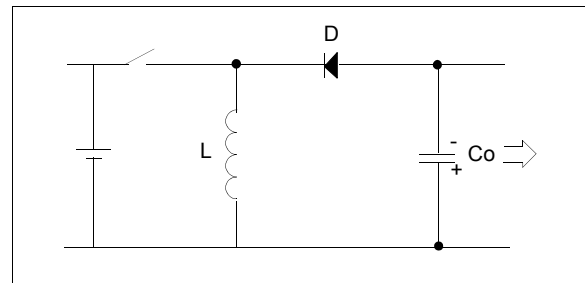
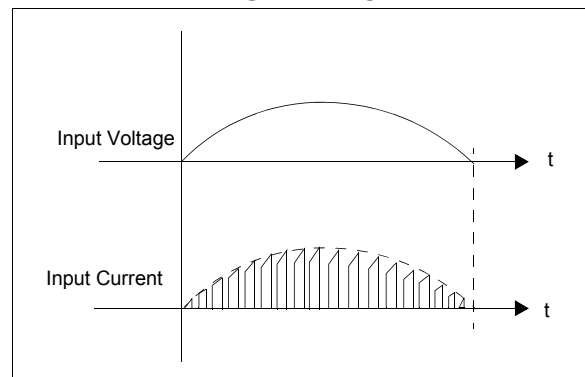


FIGURE 11: BUCK/BOOST PFC INPUT CURRENT SHAPE



Regardless of the input line voltage and output load variations, input current drawn by the buck converter and the buck boost converter is always discontinuous. However, in the case of a boost converter, input current drawn is always continuous if it is operating in Continuous Conduction Mode (CCM). This helps to reduce the input current harmonics.

PFC USING THE dsPIC30F6010A

The topology selected for the application described in this application note is the boost PFC circuit implemented digitally using the dsPIC30F6010A device. However, PFC software implementation can be done on any of the dsPIC device variants. Figure 12 illustrates the block diagram of PFC implementation using the dsPIC30F6010A.

The only output from the dsPIC device is firing pulses to the boost converter switch to control the nominal voltage on the DC bus in addition to presenting a resistive load to the AC line.

The output DC voltage of the boost converter and the input current through the inductor are the two parameters that are essentially controlled using active PFC. The technique used here for PFC is the Average Current Mode control.

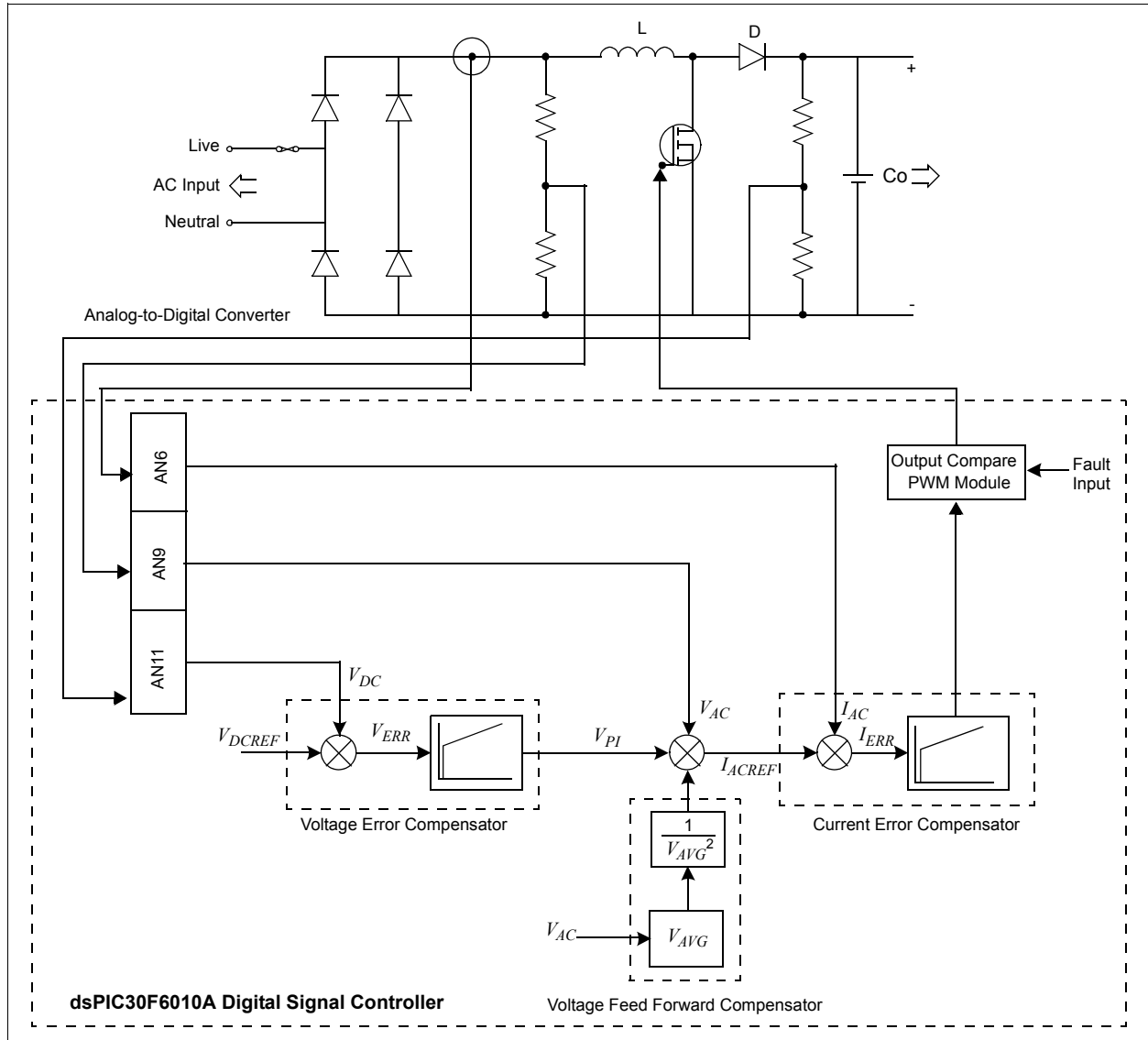
In Average Current Mode control, the output voltage is controlled by varying the average value of the current amplitude signal.

The current signal is calculated digitally by computing the product of the rectified input voltage, the voltage error compensator output and the voltage feed-forward compensator output.

The rectified input voltage is multiplied to enable the current signal to have the same shape as the rectified input voltage waveform. The current signal should match the rectified input voltage as closely as possible to have high Power Factor.

The voltage feed-forward compensator is essential for maintaining a constant output power because it compensates for the variations in input voltage from its nominal value.

FIGURE 12: BLOCK DIAGRAM FOR IMPLEMENTING PFC USING dsPIC30F6010A



PFC SOFTWARE IMPLEMENTATION

Three main blocks are integrated to achieve Power Factor Correction as shown in Figure 13 and Figure 14.

FIGURE 13: PFC HARDWARE INTERFACE

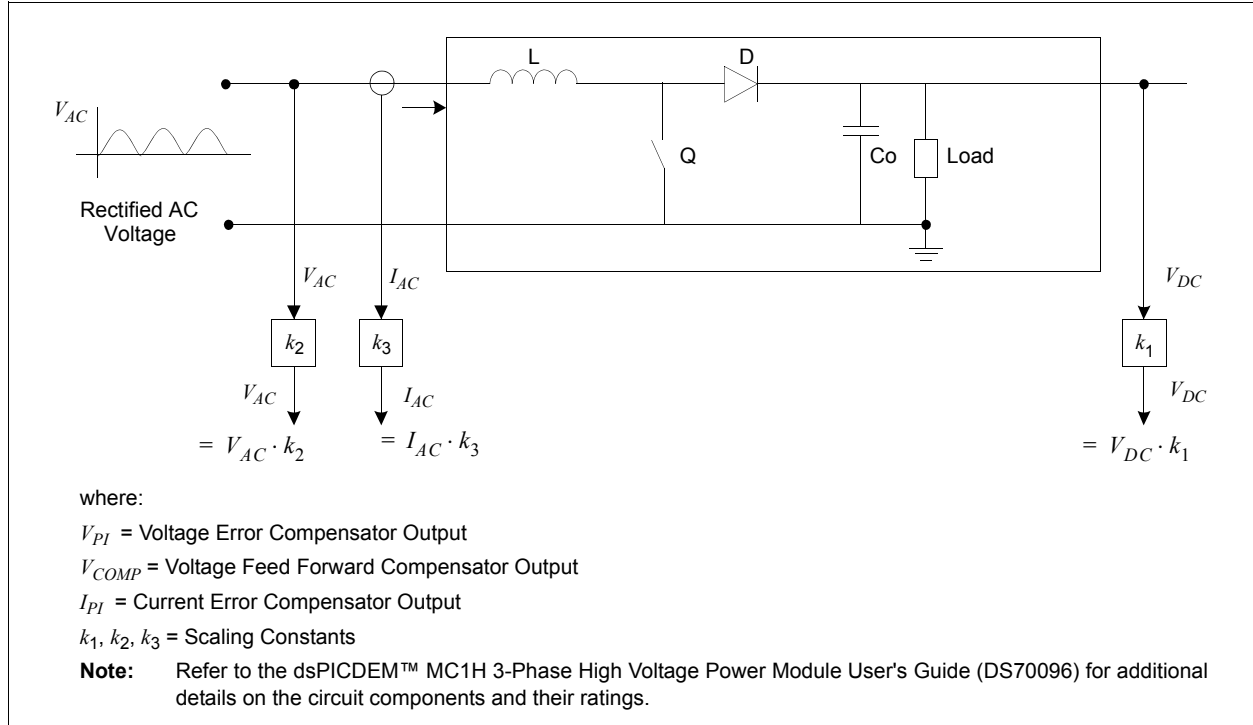
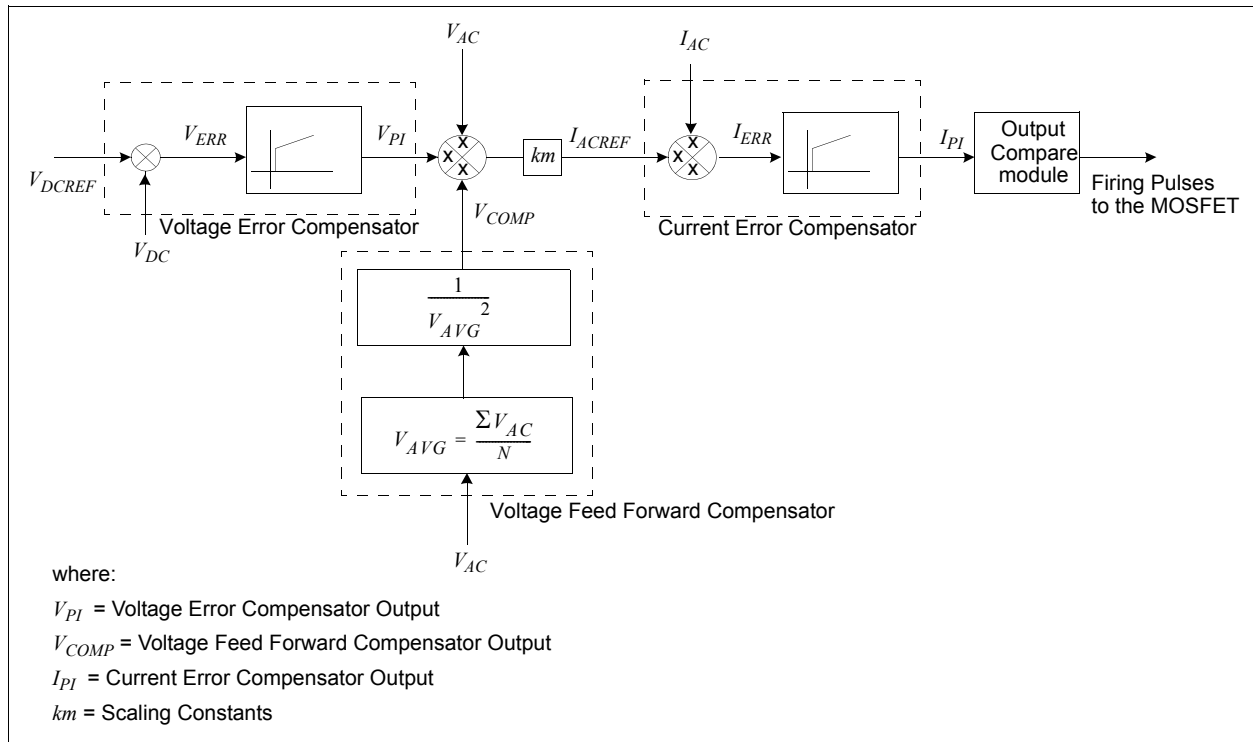


FIGURE 14: PFC SOFTWARE IMPLEMENTATION



Current Error Compensator

The inner loop in the control block forms the current loop. The input to the current loop is the reference current signal IACREF and the actual inductor current IAC. The current error compensator is designed to produce a control output such that the inductor current IAC follows the reference current IACREF.

The current loop should run at a much faster rate when compared to the voltage loop. The bandwidth of the current compensator should be higher for correctly tracking the semi-sinusoidal waveform at twice the input frequency. Usually, the bandwidth of the current compensator is between 5 kHz to 10 kHz for a switching frequency of around 100 kHz. The current loop bandwidth selected here is 8 kHz for a switching frequency of 80 kHz. A switching frequency of 80 kHz is chosen to keep the component size small.

The current controller Gi produces a duty cycle value after appropriate scaling to drive the gate of the PFC MOSFET.

Voltage Error Compensator

The outer loop in the control block forms the voltage loop. The input to the voltage loop is the reference DC voltage VDCREF and the actual sensed output DC voltage VDC. The voltage error compensator is designed to produce a control output such that the DC bus voltage VDC remains constant at the reference value Vdcref regardless of variations in the load current IO and the supply voltage VAC. The voltage controller Gv produces a control signal, which determines the reference current IACREF for the inner current loop.

The output voltage is controlled by the voltage error compensator. When the input voltage increases, the product of VAC and VPI increases, and thereby increasing the programming signal. When this signal is divided by the square of the average voltage signal, it results in the current reference signal being reduced proportionally.

The outcome is that the current is reduced proportional to the increase in voltage, thereby keeping the input power constant. This ensures that the reference control output IACREF from the voltage compensator is maximum such that the rated output power is delivered at minimum input voltage.

Voltage Feed-Forward Compensator

If the voltage decreases, the product ($V_{AC} \cdot V_{PI}$), which determines IACREF, also proportionally decreases. However, to maintain a constant output power at reduced input voltage, the term IACREF should proportionally increase. The purpose of having an input voltage feed-forward, is to maintain the output power constant as determined by the load regardless of variations in the input line voltage. This compensator implemented digitally by calculating the average value

of the input line voltage, squaring this average value and using the result as a divider for the input reference current, which is fed to the current error compensator.

If VAC is the rectified input voltage to the PFC circuit, the input voltage feed forward term is calculated as shown in Equation 3.

EQUATION 3: AVERAGE VOLTAGE COMPUTATION

In the analog domain, the continuous form of the average voltage is:

$$V_{AVG} = \frac{1}{T} \cdot \int_t^{(t+T)} (V_{AC} \cdot dt)$$

where:

V_{AC} = the instantaneous AC input voltage.

T = the time period depending on the frequency of the AC i/p voltage

In the digital domain, the discrete form of this equation is:

$$i = n + \frac{T}{T_S}$$

$$\Rightarrow V_{AVG} = \frac{1}{T} \cdot \sum_{i=n} V_{AC}^{(i)} \cdot T_S$$

$$\Rightarrow V_{AVG} = \sum_{i=n} V_{AC}^{(i)} \cdot \frac{1}{T/T_S}$$

$$\Rightarrow V_{AVG} = \frac{\sum V_{AC}^{(i)}}{N}$$

where:

V_{AC} = Input voltage at the i^{th} sample.

N = Number of samples taken

To calculate "N", which is given by $N = T/T_S$, the input line frequency, $f = 1/T$, has to be computed with the control loop frequency $f_s = 1/T_S$.

The PFC is implemented with a control loop frequency of 40 kHz running inside the ADC Interrupt Service Routine (ISR). A control loop frequency of 40 kHz is chosen to track the input voltage precisely and to shape the inductor current accurately. Based on this, the sampling time is as shown in Equation 4.

EQUATION 4: SAMPLING TIME

$$T_S = \frac{1}{40kHz} = \frac{1}{40000} = 25\mu s$$

The PFC software is designed for a line frequency range of 40 Hz to 66 Hz, as shown in Equation 5.

EQUATION 5: INPUT FREQUENCY

$$\Rightarrow f_{MIN} = 40Hz \Rightarrow T_{MAX} = 25ms$$

$$\Rightarrow f_{MAX} = 66Hz \Rightarrow T_{MIN} = 15.15ms$$

Given the previous calculations, the value of “N” has the range shown in Equation 6.

EQUATION 6: SAMPLE COUNT

$$N_{MAX} = \frac{T_{MIN}}{T_S} = \frac{25ms}{25\mu s} = 1000$$

to

$$N_{MIN} = \frac{T_{MAX}}{T_S} = \frac{15.15ms}{25\mu s} = 600$$

However, since the rectified AC input voltage is at twice the line frequency, the sample count may be anywhere between 300 and 500 with the nominal value being 333.33, corresponding to a line frequency of 60 Hz.

Figure 15 shows how to compute the number of samples “N” in the rectified AC input voltage (the zero crossing points need to be monitored).

Monitoring of zero crossing points demands more complexity in analog circuitry. Instead, the method used is to fix a minimum reference point for the input voltage, as shown in Figure 16. A counter starts when the sampled value of input AC voltage from ADC rises above V_{MINREF} , and stops when the voltage falls below V_{MINREF} in the next cycle. The count value at that point would give the value of sample count “N”.

FIGURE 15: RECTIFIED AC VOLTAGE

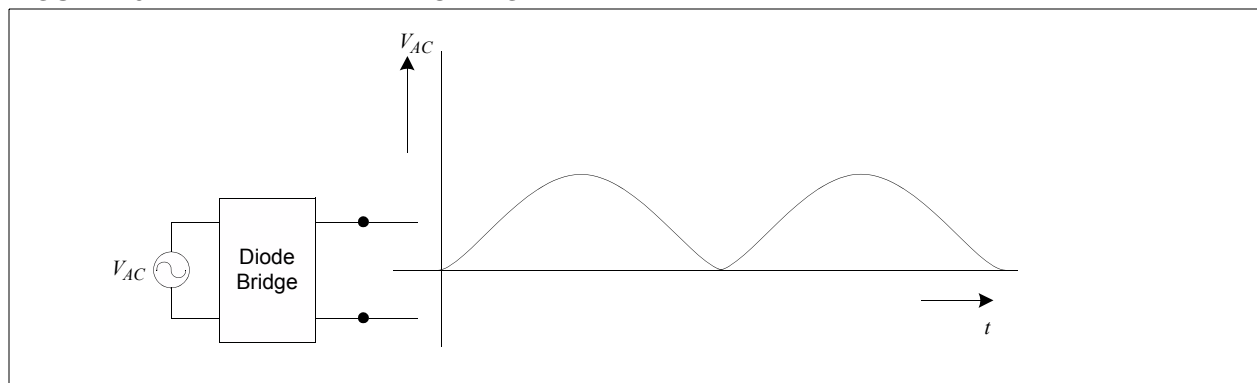
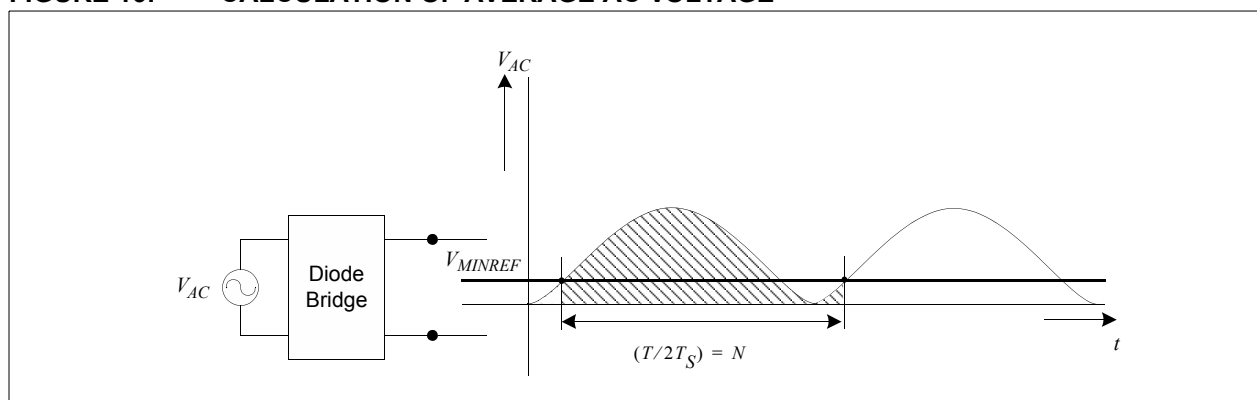


FIGURE 16: CALCULATION OF AVERAGE AC VOLTAGE



PFC DIGITAL DESIGN

The voltages V_{AC} and V_{DC} are measured using potential divider circuitry and are fed to the ADC module.

The current I_{AC} is measured using a shunt resistor (or a Hall Effect sensor) and the output voltage is fed to the ADC module, as shown in Figure 12.

This section describes the detailed design for the Power Factor Correction. The block diagram in Figure 14 is redrawn in terms of its transfer functions, as shown in Figure 17.

FIGURE 17: PFC DIGITAL DESIGN

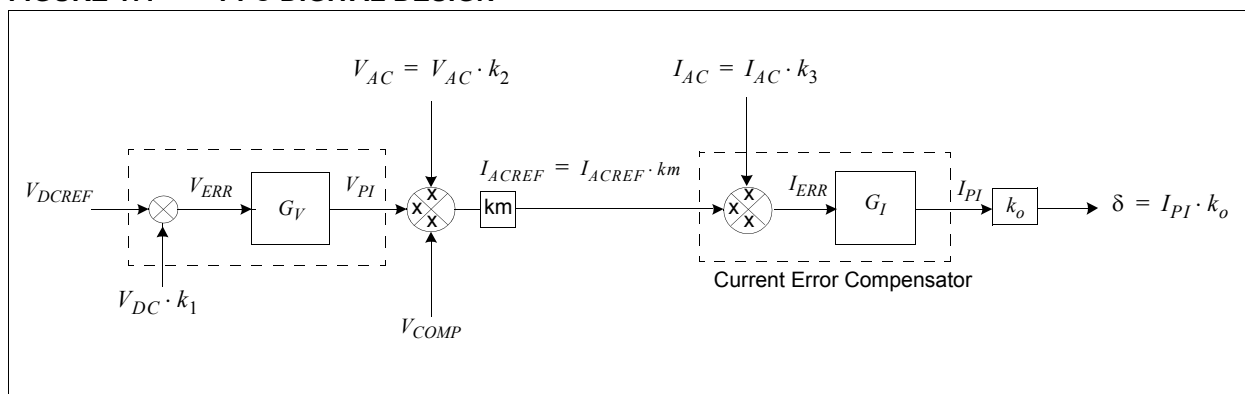


Table 1 lists the system parameters used for the PFC digital design.

TABLE 1: SYSTEM DESIGN PARAMETERS

Parameters	Values
Output power	$P = 400$ Watt
Input voltage range (peak)	$V_{ACMIN} = 100V, V_{ACMAX} = 410V$
Input frequency range	$f_{MIN} = 40$ Hz, $f_{MAX} = 66$ Hz
Output voltage	$V_{DC} = 410V$
Switching frequency	$f_{SW} = 80kHz$
Digital loop sampling frequency	$f_S = 40kHz$
Inductance	$L = 1.2mH$
Output capacitance	$C_O = 1000 \mu F$ ($330 \mu F \cdot 3$)
Voltage loop bandwidth	$f_{BWV} = 10$ Hz
Current loop bandwidth	$f_{BWI} = 8$ kHz

Note: The design calculations that follow need to be recalculated for any change in the system design parameters listed above. For a higher power requirement, the compensator constants need to be approximately calculated using the procedures described in future sections.

EQUATION 7: CALCULATION OF CONSTANTS

The maximum inductor current is:

$$I_{ACMAX} = \frac{2 \cdot P}{V_{MIN}} = \frac{2 \cdot 400}{100} = 8A$$

The gain constants k_1 , k_2 , k_3 , and km are selected as:

$$k_1 = \frac{1}{V_{DC}} = \frac{1}{410} = 0.00244$$

$$k_2 = \frac{1}{V_{ACMAX}} = \frac{1}{410} = 0.00244$$

$$k_3 = \frac{1}{I_{ACMAX}} = \frac{1}{8} = 0.125$$

$$km = \frac{V_{ACMAX}}{V_{ACMIN}} = \frac{410}{100} = 4.1$$

Note: All the number representations in the software are done in a fixed point 1.15 (Q15) format. When the constants exceed the range of 0x7FFF, they are converted to an appropriate number format for processing and later the resulting output is brought back to Q15 format.

Table 2, Table 3 and Table 4 show the numerical range along with the base value for the various inputs.

TABLE 2: AC INPUT VOLTAGE NUMERICAL REPRESENTATION

	V_{AC} (RMS)	V_{AC} (Peak)	ADC (Input)	Q15 Format
Maximum	290 volt	410 volt	5.0 volt	0x7FFF
Minimum	70 volt	100 volt	1.2069 volt	0x1EE0
Nominal	230 volt	325 volt	3.965 volt	0x6560

TABLE 3: AC INPUT FREQUENCY NUMERICAL REPRESENTATION

	f	f_{RECT}	Sample Count (N)
Maximum	66 Hz	132 Hz	300
Minimum	40 Hz	80 Hz	500
Nominal	50 Hz	100 Hz	400

TABLE 4: DC OUTPUT VOLTAGE NUMERICAL REPRESENTATION

	V_{DC}	ADC Input	Q15 Format
Nominal	410 volt	4.5 volt	0x7300

Current Error Compensator Design

EQUATION 8: CURRENT ERROR COMPENSATOR

The transfer function for the current error compensator is given by:

$$G_I(s) = k_{pi} + \frac{k_{Ii}}{s} = k_{pi} \cdot \left(\frac{1 + T_{co} \cdot s}{T_{co} \cdot s} \right)$$

where: $f_z = 800\text{Hz}$, which is the location of zero for the current PI controller and,

$$T_{co} = \frac{1}{2\pi f_z}$$

$$G_I(s) = \left(\frac{2\pi f_{BWI} \cdot L}{k_3 \cdot V_{DC}} \right) \cdot \left(\frac{1 + T_{co} \cdot s}{T_{co} \cdot s} \right)$$

$$G_I(s) = \left(\frac{2\pi \cdot 8\text{kHz} \cdot 1.2\text{mH}}{0.125 \cdot 410} \right) \cdot \left(\frac{1 + 198.94 \cdot 10^{-6}s}{198.94 \cdot 10^{-6}s} \right)$$

$$G_I(s) = 1.177 \cdot \left(\frac{1 + 198.94 \cdot 10^{-6}s}{198.94 \cdot 10^{-6}s} \right)$$

$$G_I(s) = 1.177 + \frac{5916 \cdot 356}{s}$$

$$= k_{pi} + \frac{k_{Ii}}{s}$$

$$k_{pi} = 1.177$$

$$k_{Ii} = \frac{5916 \cdot 356}{40\text{kHz}} = 0.1479$$

The correction term k_{ci} is given by:

$$k_{ci} = \frac{k_{Ii}}{k_{pi}} = 0.12566$$

Therefore, for the current error compensator:

Proportional Constant	$k_{pi} = 1.177$	->	2410	(Q 11 Format)
Integral Constant	$k_{Ii} = 0.1479$	->	4846	(Q 15 Format)
Correction Constant	$k_{ci} = 0.12566$	->	4117	(Q 15 Format)

Note: The current loop bandwidth is chosen to be 8 kHz. This is selected such that the current faithfully tracks the semi-sinusoidal input voltage at 100 Hz or 120 Hz. The current compensator 'zero' is placed by taking the digital delays into consideration. Therefore, for a phase crossover frequency of 8 kHz, the 'zero' placement is done well below this frequency. A frequency of 800 Hz is chosen in this application for placing the current PI compensator 'zero'.

Voltage Error Compensator Design

EQUATION 9: VOLTAGE ERROR COMPENSATOR

The transfer function for the voltage error compensator is given by:

$$G_V(s) = k_{pV} + \frac{k_{Iv}}{s}$$

$$G_V(s) = k_{pV} \left(\frac{1 + T_{co} \cdot s}{T_{co} \cdot s} \right) = \frac{2k_2k_3(V_{ACMAX})^2}{k_1k_m(V_{ACMIN})} \frac{V_{DC}}{Z_{fcv}} \left(\frac{1 + T_{co} \cdot s}{T_{co} \cdot s} \right)$$

where: $f_z = 10$ Hz, which is the location of 'zero' for the voltage P_I controller

$$T_{co} = \frac{1}{2\pi f_z}$$

Computing for $G_V(s)$:

$$G_V(s) = \frac{420.25}{Z_{fcv}} \left(\frac{1 + 15.9155 \cdot 10^{-3}s}{15.9155 \cdot 10^{-3}s} \right) \quad \text{_____ (1)}$$

Here, Z_{fcv} is the equivalent impedance considering the parallel combination of output capacitance, PFC stage output impedance and load impedance:

$$Z_{fcv} = Z_o \left| \frac{1}{Cs} \right| Z_L = \frac{1}{\frac{1}{Z_o} + \frac{1}{Z_L} + Cs}$$

To supply a constant power load with maximum efficiency:

$$Z_{fcv} = \frac{1}{Cs} = \frac{1}{2\pi \cdot 10 \cdot 1000\mu F \cdot s}$$

$$Z_{fcv} = 15.91545 \quad \text{_____ (2)}$$

Using equation (2) in equation (1)

$$G_V(s) = 27 \cdot \left(\frac{1 + 15.9155 \cdot 10^{-3}}{15.9155 \cdot 10^{-3}} \right) = 27 + \frac{1696}{s}$$

$$k_{pV} = 27$$

$$k_{Iv} = \frac{1696.46}{40kHz} = 0.042411$$

$$\text{Correction factor, } k_{cv} = \frac{k_{Iv}}{k_{pV}} = 0.00157$$

Therefore, for the current error compensator:

Proportional Constant	$k_{pV} = 27$	->	27648	(Q 10 Format)
Integral Constant	$k_{Iv} = 0.042411$	->	1390	(Q 15 Format)
Correction Constant	$k_{cv} = 0.00157$	->	51.47	(Q 15 Format)

Note: The voltage loop bandwidth is chosen to be 10 Hz. This is selected to be well below the input frequency of 100 Hz or 120 Hz, so that the second harmonic ripple on the DC bus voltage is eliminated. The voltage compensator, 'zero', is the same as the voltage loop bandwidth, because at 10 Hz, the digital delays are insignificant.

TIMING LOGIC FOR THE SOFTWARE IMPLEMENTATION

Timer3 runs at a frequency of 80 kHz while supplying a trigger to the ADC every period (80 kHz). An ADC interrupt occurs every 2 timer periods (40 kHz).

The ADC module is used in Channel Scanning mode. The two voltages, VDC and VAC are sampled and converted on alternate triggers, while the current IAC is sampled and converted on every trigger.

The following analog channels and buffers are used on the dsPIC30F6010A device:

- The first ADC interrupt is generated after converting channels:
 - AN9 - VDC, DC Bus voltage (ADCBUF0)
 - AN6 - IAC, inductor current (ADCBUF3)

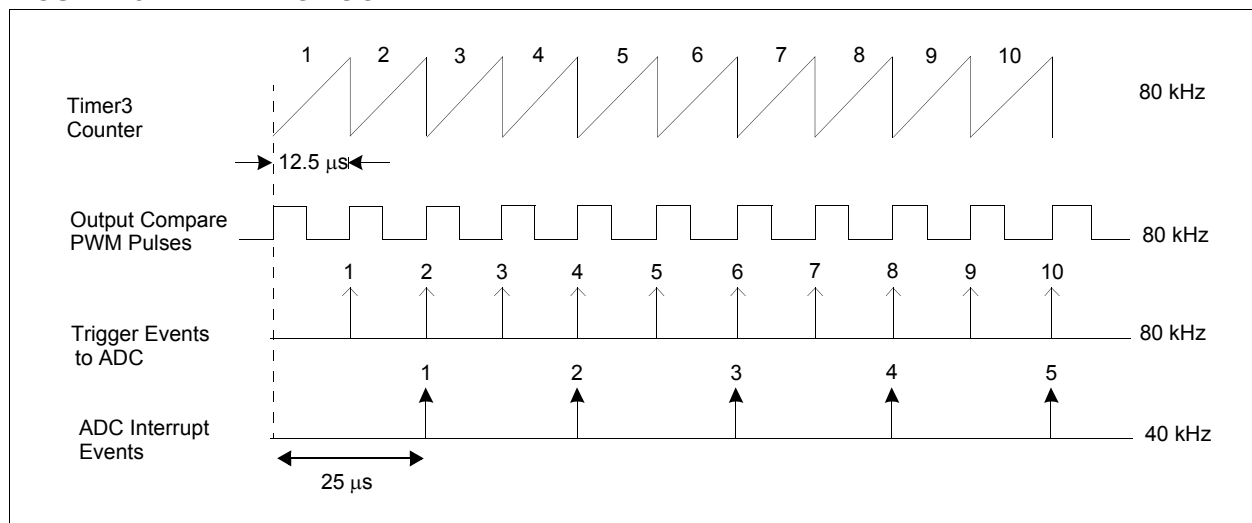
- The second ADC interrupt is generated after converting channels:
 - AN11 - VAC, rectified voltage (ADCBUF4)
 - AN6 - IAC, inductor current (ADCBUF7)

Analog inputs AN9 and AN11 are in channel scanning alternately.
- At any point in the control loop reading from:
 - ADCBUF0 gives the DC bus voltage
 - ADCBUF3 and ADCBUF7 give the inductor current
 - ADCBUF4 gives the AC voltage

The Output Compare module OC6 is in PWM mode to generate the PWM pulses to drive the gate of the PFC MOSFET. The time base for the Output Compare module is given by the Timer3 module running at 80 kHz.

These events, along with the A/D interrupt generation sequence, are shown in the timing logic in Figure 18.

FIGURE 18: TIMING LOGIC



SOFTWARE FLOW

The main software flow is shown in Figure 19. After a Reset, when the program is executed, all the variables are initialized and peripherals are configured. The PI parameter values are defined for the control loop compensators. The Timer3 module is switched ON to operate at a frequency of 80 kHz, and all the interrupts are enabled.

The ADC module waits for a Timer3 special event interrupt. On every period match, the timer generates a trigger to the ADC to start sampling the signals and converting them. On a timer trigger, the ADC samples and converts the voltages and currents and later generates an ADC interrupt.

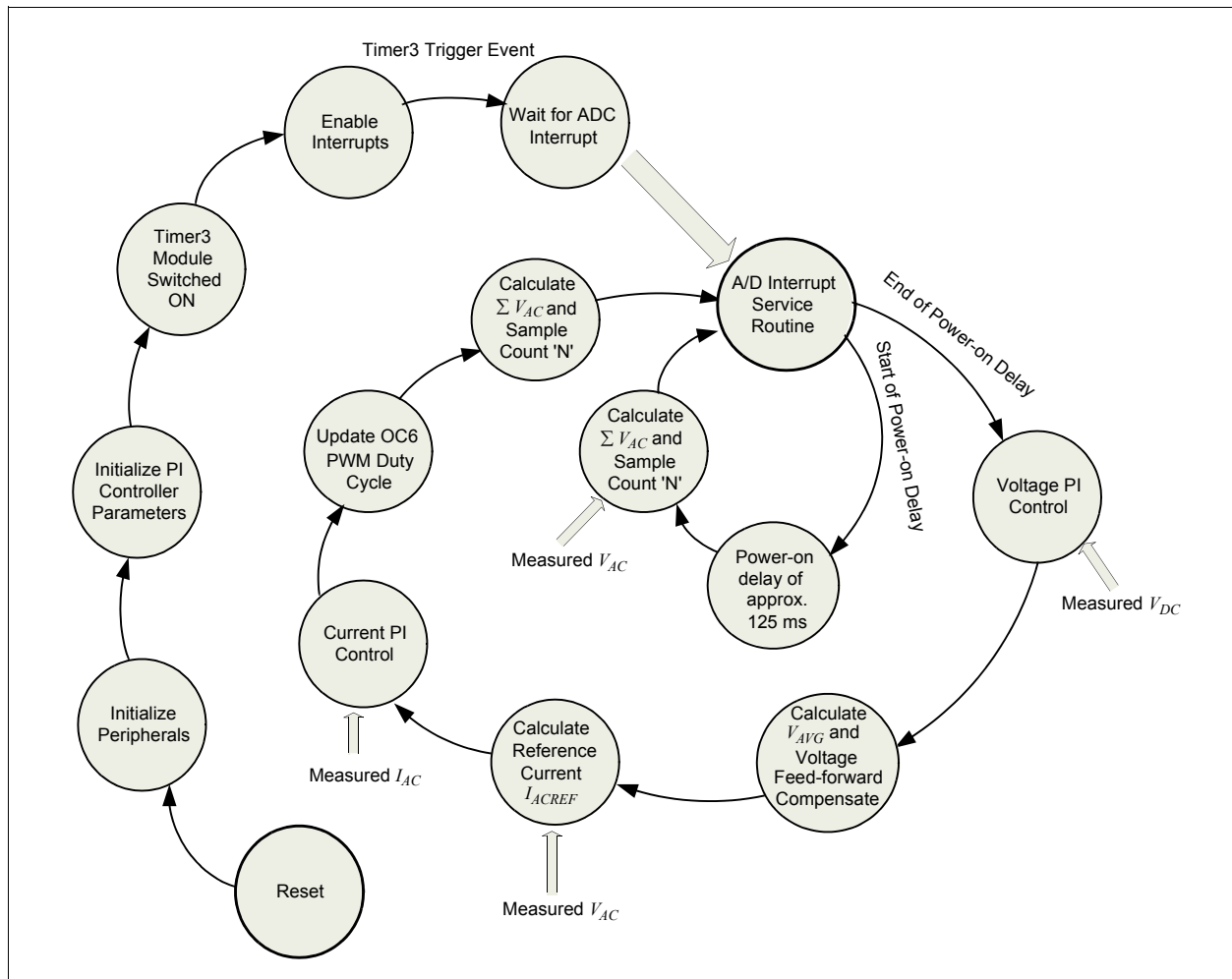
The PFC routines run inside the ADC Interrupt Service Routine (ISR). A power-on delay is allowed for the capacitors to charge to the DC bus voltage. After the power-on delay time (approximately 125 ms) completion, the control loops begin to execute. During

the process of power-on delay, the voltage samples are accumulated and frequency is calculated. This enables the average voltage calculation to be done in the first iteration of the control loop itself, as the average voltage is already available for a period corresponding to one line voltage cycle.

The voltage error compensators execute the voltage PI controllers having the measured value of DC bus voltage V_{DC}. The average value of input voltage, squaring and dividing routines, execute in sequence from the measured value of input AC voltage thereby giving the voltage feed-forward compensator output. This output is used in conjunction with the voltage error compensator output to calculate the reference value I_{ACREF}. Having I_{ACREF} and the measured value of the inductor current, the current error compensator executes the current PI controllers to produce the new duty cycle for the Output Compare module.

In the process, voltage samples accumulate and EV_{AC} is calculated in every iteration.

FIGURE 19: SOFTWARE FLOW



FUNCTION USAGE IN SOFTWARE

The functions listed in the Table 5 are used in software for implementing the various stages of PFC.

TABLE 5: PFC FUNCTIONS

Function Name	Description
<code>calcVsumAndFreq()</code>	Routine to compute V _{SUM} and frequency
<code>VoltagePIControl()</code>	Routine for voltage error compensator
<code>calcIacRef()</code>	Routine to calculate reference current
<code>CurrentPIControl()</code>	Routine for current error compensator

The functions listed in Table 6 are implemented for other auxiliary functions such as initializing the high voltage board, setting up the GPIO ports, configuring the interrupt priority and initialization of peripherals.

TABLE 6: AUXILIARY FUNCTIONS

Function Name	Description
<code>SetupBoard()</code>	Routine to clear and reset faults
<code>SetupPorts()</code>	Routine to initialize the GPIO ports
<code>InitOutputCompare6()</code>	Routine to configure Output Compare and Timer modules
<code>configADC()</code>	Routine to configure the ADC module

Note: The functions are implemented in assembly language and are callable from C routines.

PFC CONTROL INTEGRATION

The software for PFC has been developed to be used in conjunction with any other application where the first stage remains an AC-to-DC conversion demanding a constant DC voltage and a sinusoidal current wave shape.

With higher load demand and larger power levels, the application parameters may have to be modified to take this into consideration. The compensator gains and constants may require retuning and better protection levels incorporated in the system hardware with higher-rated components to cope with higher loads.

Applications in which the PFC stage can be used as an integral part are:

- Motor control applications
- Uninterruptible power supply applications
- Switched mode power supply applications

The PFC software uses some device peripherals and resources that cannot be shared with any other application. This excludes the ADC module, which can be used with the analog channels that are not used for PFC implementation.

The peripherals that cannot be shared for other applications are:

- Output Compare – 6 Module

This module is used in PWM mode to operate on its own time base rather than using the Motor Control (MC) PWM module, which can drive other applications like switching inverters in motor control and power supply related applications.

- Timer3 Module

This module is used to provide the time base to run the Output Compare module in addition to acting as a trigger source for the ADC module.

- Analog to Digital Converter

This module uses analog channels AN6, AN9 and AN11 for converting analog signals IAC, VAC and VDC, respectively. The remaining 13 channels can be used for any other application in conjunction with the PFC software.

The resources used for the PFC application are:

- Program Memory (ROM): 2013 bytes
- Data Memory (RAM): 142 bytes
- Processor Speed: 30 MIPS running from a 7.37 MHz external crystal
- MIPS: Approximately 10 MIPS utilized when the dsPIC is running at 30 MHz

LABORATORY TEST RESULTS AND WAVE FORMS

The following figures show the various waveforms including inductor current, DC bus voltage, input current and the test results, which include PF improvement and current harmonic reduction. This information aids in validating the PFC implementation, in addition to providing a comparison to a system without PFC.

FIGURE 20: INDUCTOR CURRENT WAVE FORM WITHOUT PFC

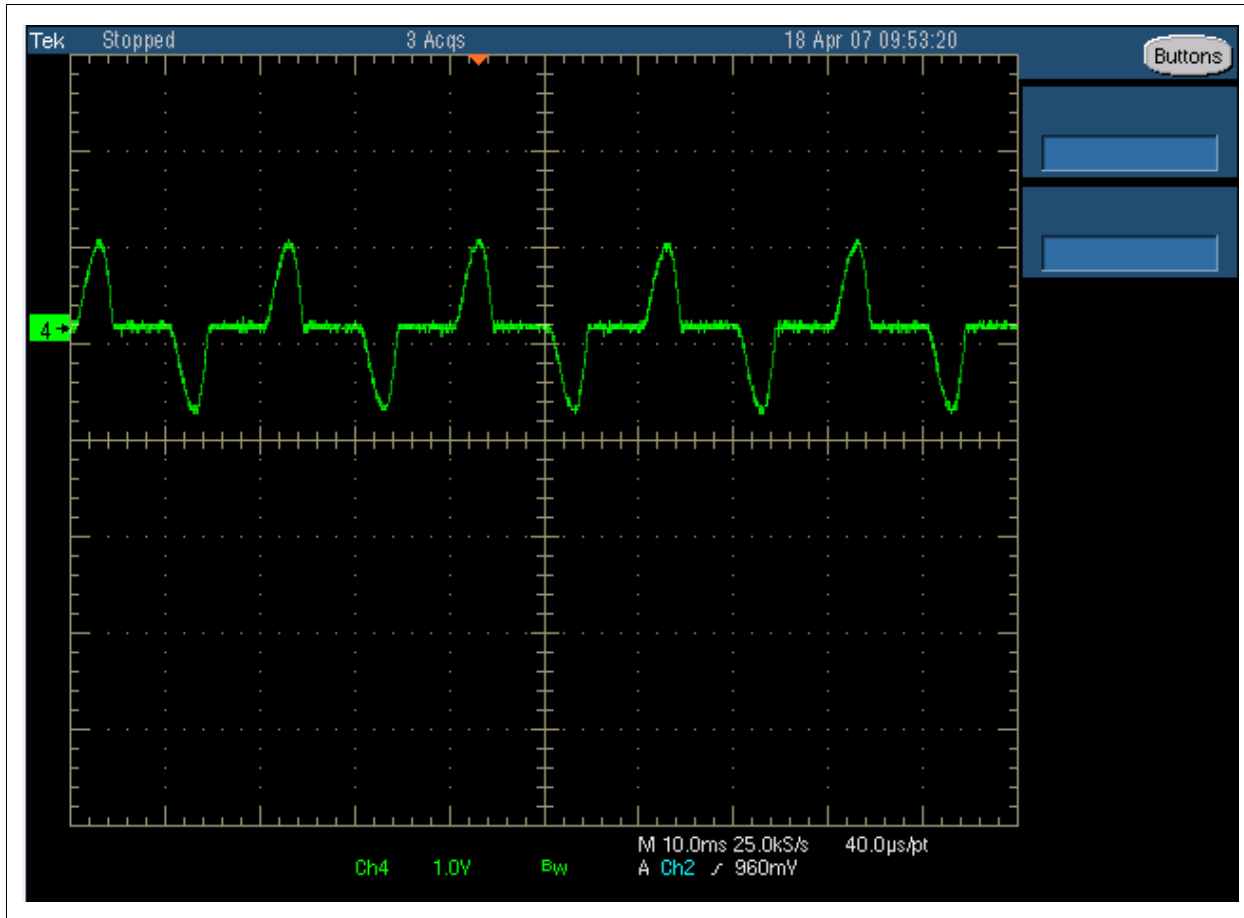


FIGURE 21: PFC START-UP CHARACTERISTICS

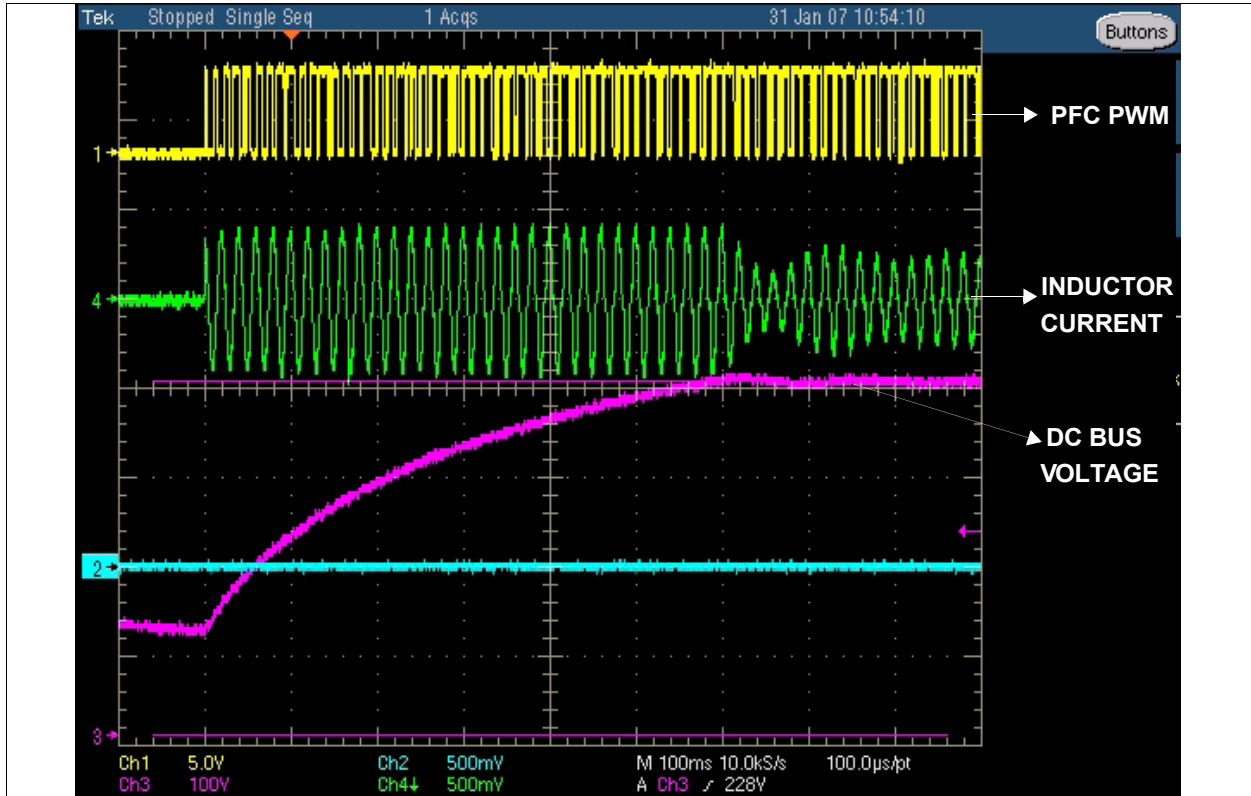


FIGURE 22: WAVE FORMS WITH PFC

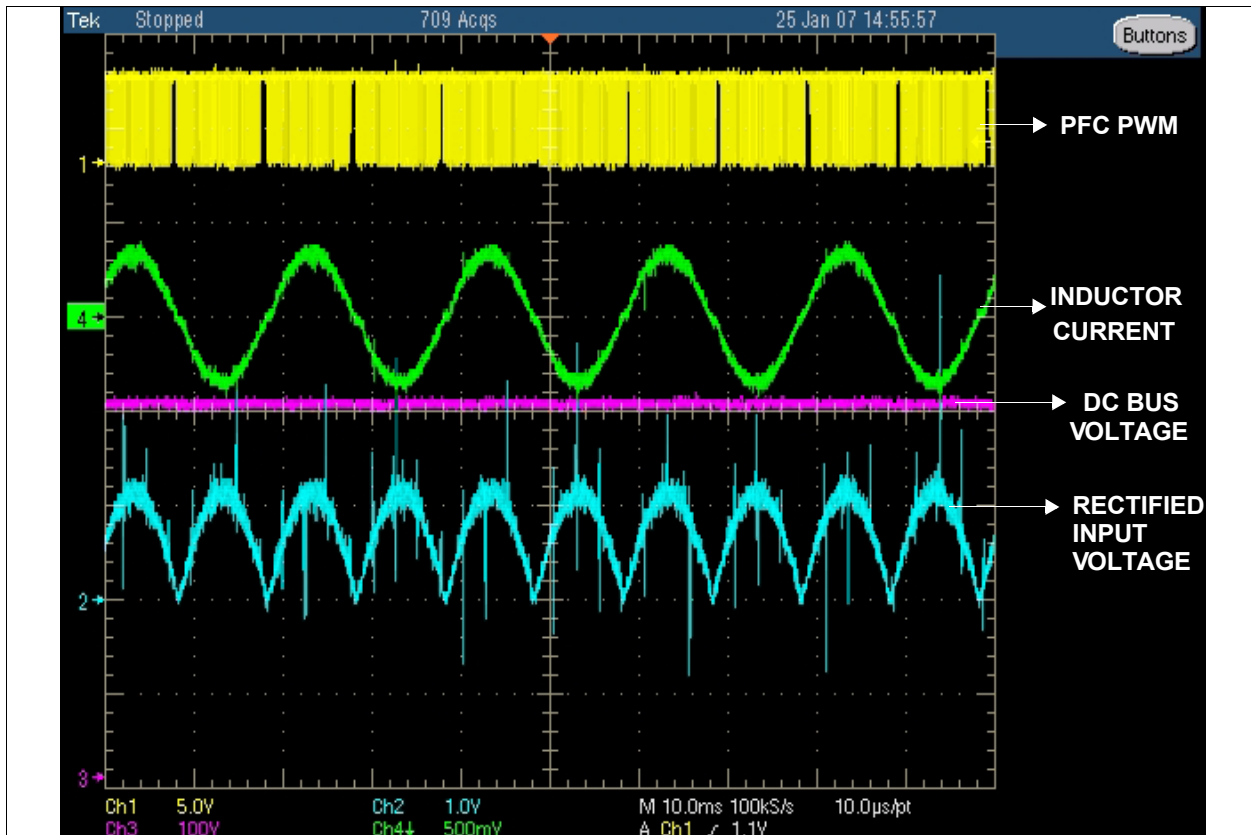


FIGURE 23: RESULTING POWER FACTOR WITH PFC

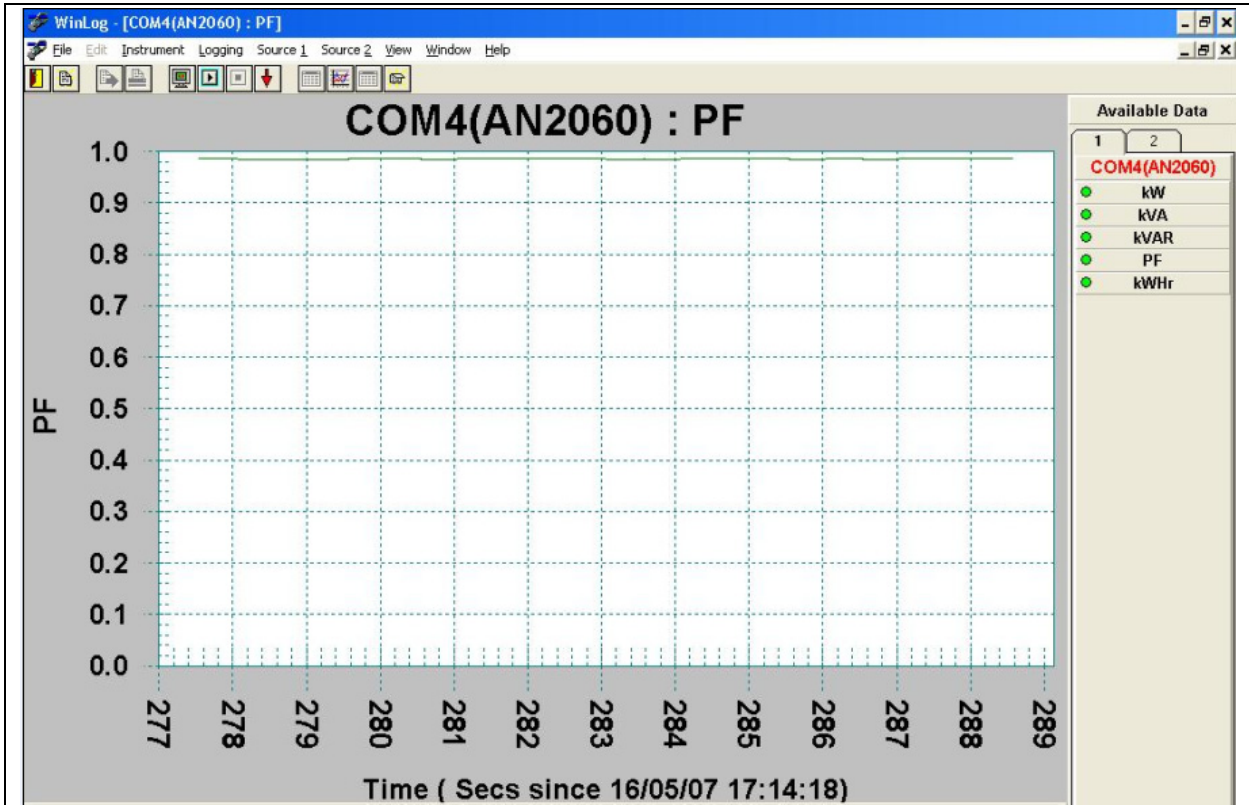
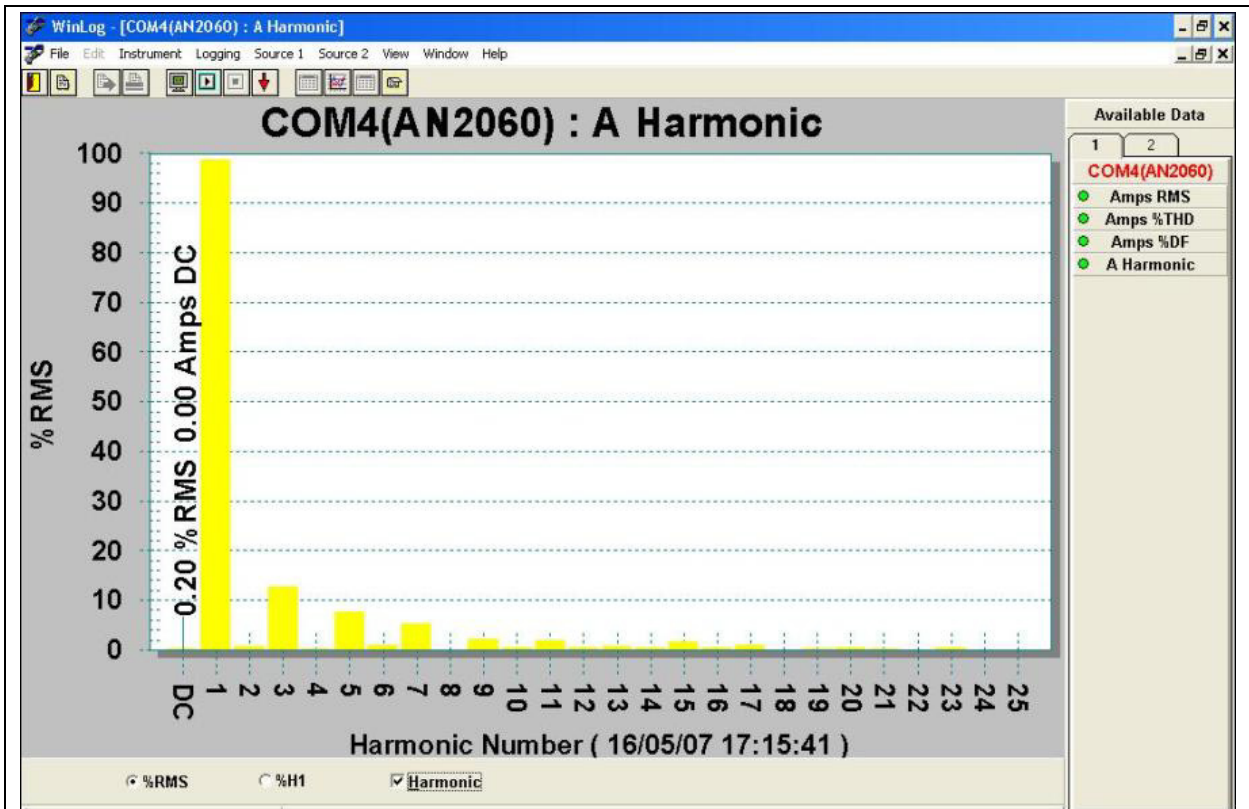


FIGURE 24: RESULTING HARMONIC REDUCTION WITH PFC



SUMMARY

This application note shows how to implement Power Factor Correction (PFC) through average current mode control using a dsPIC device.

The dsPIC device provides a wide variety of peripherals and memory to integrate this application with other related applications using the dsPICDEM™ MC1H 3-Phase High Voltage Power Module (P/N DM300021) and the dsPICDEM™ MC1 Motor Control Development Board (P/N DM300020).

The firmware used in this application (see **Appendix A: "Source Code"**) is written in assembly language to effectively make use of the special DSP operations.

For further development, the MPLAB® IDE and the development tools provide a flexible platform to develop code and debug programs.

REFERENCES

- *Digital Control For Power Factor Correction*, Manjing Xie. Virginia Polytechnic Institute and State University, June 2003.
- *Topological Issues in Single Phase Power Factor Correction*, Vlad Grigore, Helsinki University of Technology. Institute of Intelligent Power Electronics, November 2001 - <http://lib.tkk.fi/Diss/2001/isbn9512257351/>
- *dsPICDEM™ MC1H 3-Phase High Voltage Power Module User's Guide* (DS70096)
- *dsPICDEM™ MC1 Motor Control Development Board User's Guide* (DS70098)
- *dsPIC30F Family Reference Manual* (DS70046)

Note: When using a dsPIC33F device for implementing the PFC algorithm, these variations must be followed:

- dsPIC33F devices operate at 40 MIPS (40 MHz):
All timing considerations should be verified to suit this operating frequency. The Output Compare module's period and duty cycle should be recalculated for this frequency. The ADC triggering event from the timer should also be recalculated.
- Some of the dsPIC33F devices may use DMA with the ADC module:
All ADC results are stored in buffers configured in the DMA RAM. Therefore, the DMA controller needs to be configured for the ADC module to receive and transfer the results to the appropriate buffers.
- The GPIO ports must be checked for compatibility with each device variant.

APPENDIX A: SOURCE CODE

Any libraries and source files associated with this application note are available for download as a single archive file from the Microchip corporate Web site (www.microchip.com).

APPENDIX B: HARDWARE COMPONENT SELECTION FOR THE PFC BOOST CIRCUIT

The essential components for a PFC Boost Circuit are:

- Inductor
- MOSFET
- Diode
- Capacitor

For this application, the dsPICDEM™ MC1H 3-Phase High Voltage Power Module (part number DM300021) and its hardware components were used for development. Please refer to the user's guide for complete details on the hardware components and their values (see "**References**").

A PFC component calculator in the form of an Excel® spreadsheet, can be used for properly selecting the hardware components for any desired power rating. This file, `PFC_component_calculator.xls`, can be obtained from the Microchip Web site (www.microchip.com).

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