LX7720 and SAMRH71F20 PMSM FOC Motor Demo

Description

These instructions cover a reference design controlling a Hurst DMA0204024B101 3-phase permanent magnet synchronous motor (PMSM) with built-in quadrature encoder and 120° Hall-effect sensors with demonstration firmware running on a radiation hardened SAMRH71F20 MCU.

The reference design landing page is here: High-End Radiation Hardened PMSM Motor Control Demonstration Application. The MPLAB Harmony repository on Github is here: PMSM FOC using Quadrature Encoder with SAMRH71-EK and LX7720 boards.

The LX7720 drives 3 MOSFET half-bridges for the 3 motor phases, senses motor phase currents, and monitors the motor's two-channel quadrature optical encoder via the BLI1 and BLI2 comparator inputs. The SAMRH71F20 (200 DMIPS Cortex M7 with 100krad TID capability) operates as the PI loop controller using field oriented control (FOC). A useful application note on FOC is here: AN2757 - Sensored (Encoder-Based) Field Oriented Control of a Three Phase Permanent Magnet Synchronous Motor (PMSM).

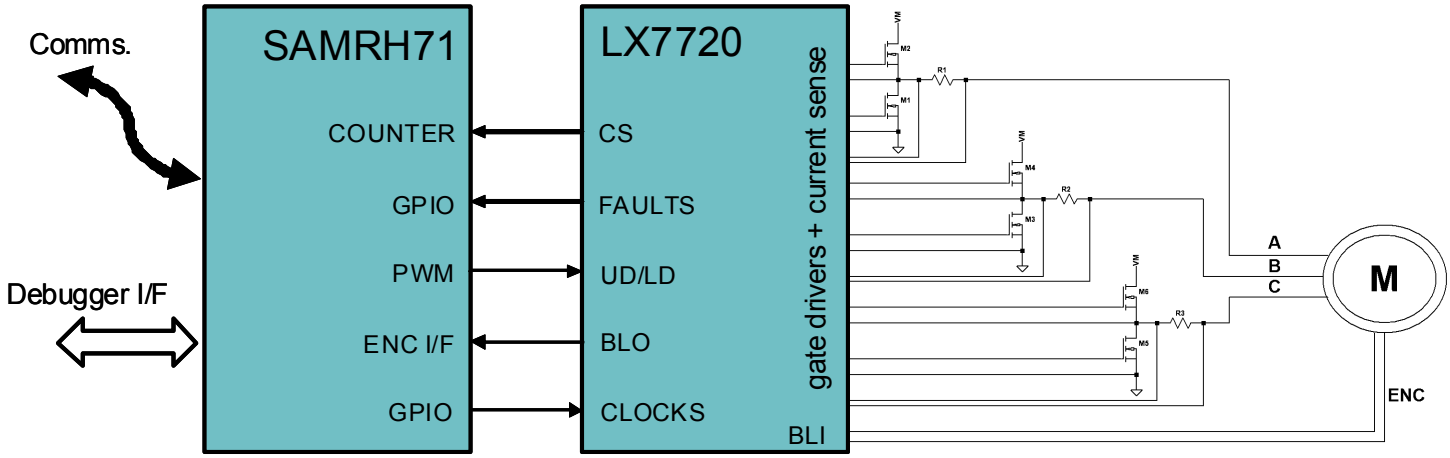

Figure 1. LX7720 and SAMRH71F20 Motor Driver Demo Top Level Block Diagram

1 Hardware and Setup

1.1 Hardware Requirements

- Either a SAMRH71F20-EK evaluation kit or a SAMRH71-TFBGA-EK evaluation kit for the SAMRH71F20 MCU
- An LX7720-DB daughter board
- Linker board between SAMRH71 board and LX7720-DB
- A Hurst DMA0204024B101 24V, 10 pole, 3-phase BLDC with built-in quadrature encoder

1.2 Linker Boards

The SAMRH71-EK linker (Figure 2 on page 2) interconnects a SAMRH71F20-EK evaluation kit and an LX7720-DB.

The SAMRH71-TFBGA-EK linker (Figure 3 on page 2) interconnects a SAMRH71-TFBGA-EK evaluation kit and an LX7720-DB.

An additional small board provides pushbutton switches and LEDs for control and status.

Table 2 on page 4 shows the MCU resource mapping used by the reference design.

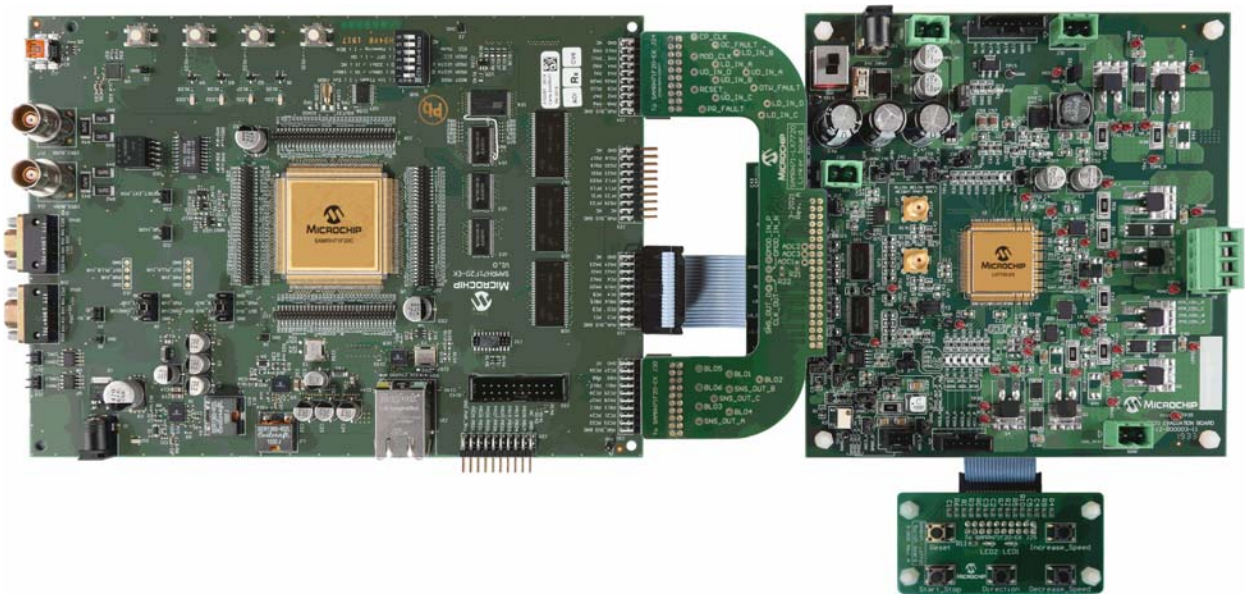

Figure 2. LX7720 Daughter Board Connected to SAMRH71F20-EK Evaluation Kit Using Linker Board

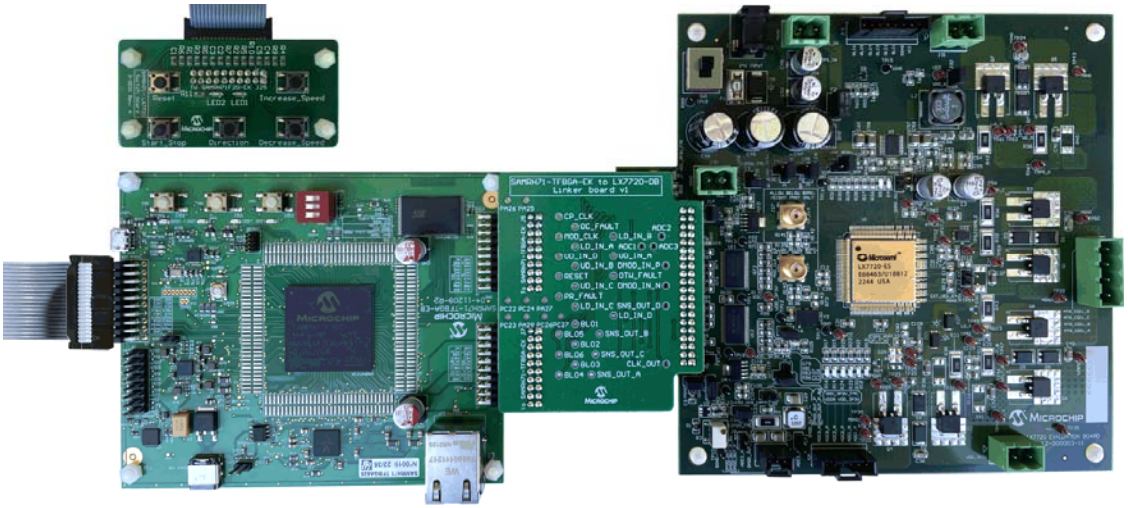

Figure 3. LX7720 Daughter Board Connected to SAMRH71-TFBGA-EK Evaluation Kit Using Linker Board

1.3 Motor Connections

Connect the Hurst DMA0204024B101 BLDC motor windings to connector J9, and its built-in quadrature encoder to connector J15 on the LX7720 board as shown in Table 1 below.

Table 1. Motor Connections

Hurst Motor Connection	Wire Color	LX7720-DB Connector	LX7720-DB Signal
Motor winding phase A	white	J9 pin 1	Phase A
Motor winding phase B	black	J9 pin 2	Phase B
Motor winding phase C	red	J9 pin 3	Phase C
Encoder VDD	red	J15 pin 1	VCC (+3.3V)
Encoder GND	black	J15 pin 2	GND
Encoder Output A	white	J15 pin 3	BLI1
Encoder Output B	blue	J15 pin 4	BLI2

1.4 SAMRH71 Firmware Implementation

The demo firmware implements an FOC algorithm using two D/Q space current PI loops, and a speed regulation loop using the two-channel quadrature optical encoder built into the motor. The current sense processing and the FOC algorithm sustaining a 20kHz PWM (fast) loop and 4kHz torque (slow) loop bring the SAMRH71 CPU to < 55% loading.

The control algorithm is from the Harmony 3 Motor Control module. An additional algorithm is used to filter the currents on phase A and B from the LX7720, which are second order sigma delta modulated streams.

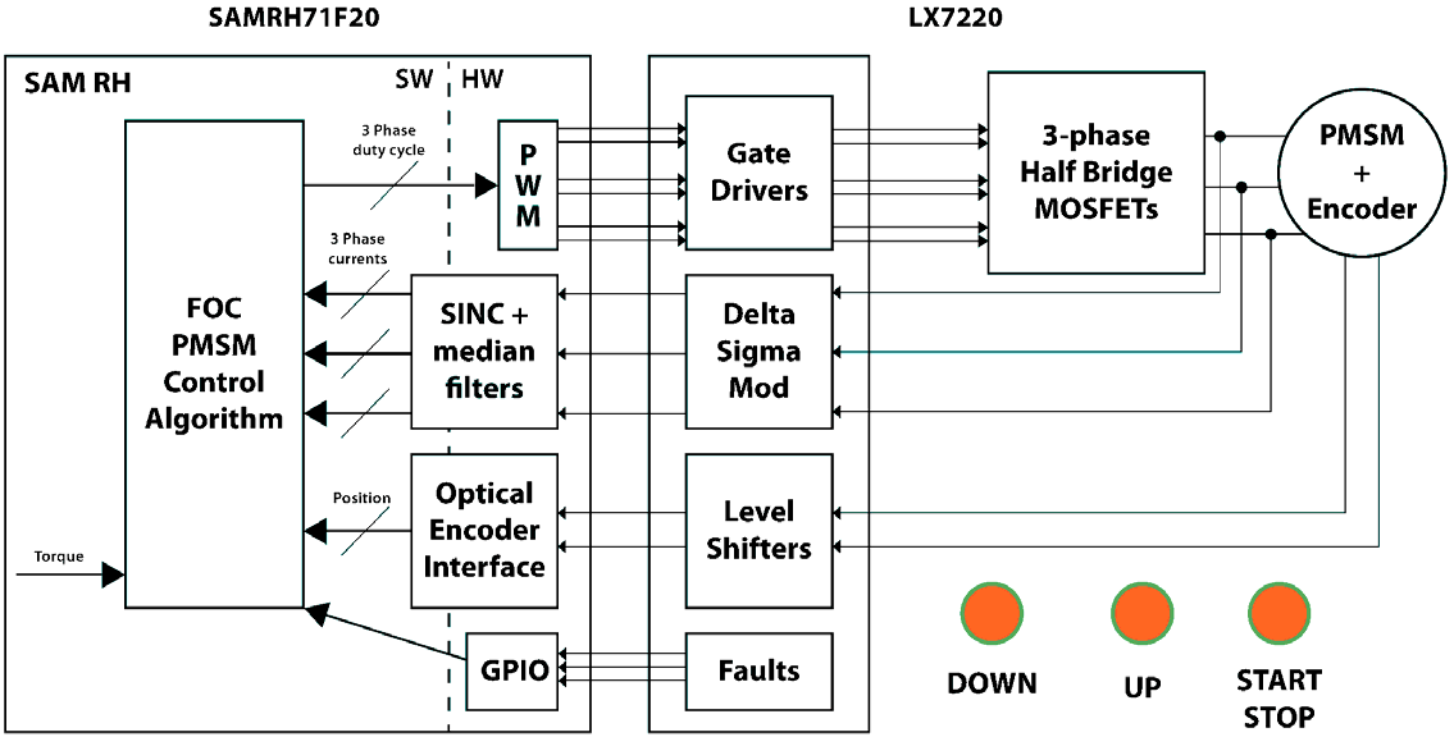

Figure 4. LX7720MLF EVB to SAMRH71F20-EK Demo Detailed Block Diagram

The SAMRH71 functions are summarized as follows:

- Generates six 20kHz PWM waveforms for the LX7720's half-bridges (independent high and low drives to incorporate dead-time)
- Generates the LX7720's 25MHz ΔΣ modulator clock using PCK0, and the 150kHz charge pump clock using PCK2
- Senses rotor position using the motor's two-channel quadrature optical encoder connected to the LX7720's BLI1 and BLI2 comparator inputs. SAMRH71 TIOs monitor the LX7720's corresponding BLO1 and BLO2 comparator outputs
- Calculates motor currents using digital filters on the LX7720's SNS_OUT_A and SNS_OUT_B current sense ΔΣ modulator output streams:
  - Integrator using a timer/counter
  - SINC³ decimation filter
  - Median filter
  - Motor phase C current calculated as sum of motor phase A and B currents, to avoid the processing overhead of filtering the phase C current's ΔΣ serial stream
- Monitors LX7720 fault outputs via GPIO

The motor phases A and B current stream sampling is done with a timer-counter each. The timer counters are clocked at 50MHz, and count the number of high periods of the 25MHz ΔΣ modulator streams for a 4µs interval to form a SINC¹ filter with over-sample ratio OSR1=50. The maximum counter value for full scale (all ones on a SNS_OUT_x output) is 50MHz x 4µs = 200.

A digital third order cascaded integrator-comb (CIC) aka SINC³ filter performs anti-aliasing filtering and decimation with over-sample ratio OSR2=5. This filter is applied to the SINC1 sample stream, and produces filtered output data every 20µs. This corresponds to 2.5 current measurement results per 50µs (at f_{PWM}=20kHz) PWM periods (Figure 5 on page 4).

The final calculation for phases A and B currents is performed in the FOC control interrupt routine. The currents are calculated with a weighted average on the last 4 samples.

The FOC control loop is executed in an interrupt routine generated by a timer counter. This counter starts when the PWM event signal is raised. Then the interrupt is triggered after 20µs using the timer compare mode. This ensures that there is at least one current SINC³ sample calculated before the weight average calculation.

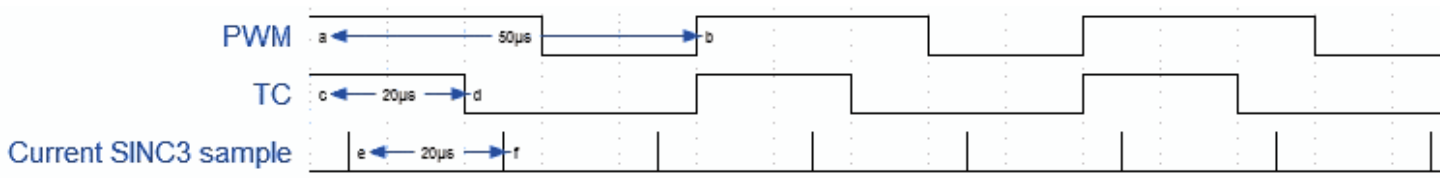

Figure 5. PWM and Filter Timing

The final filtered output has a full scale of 200 x 5^3 = 25000. The LX7720 current sense input has a differential full scale of ±350mV. Therefore:

- 25000 corresponds to +350mV across the phase's current sense resistor
- 12500 corresponds to 0mV across the phase's current sense resistor
- 0 corresponds to -350mV across the phase's current sense resistor

The 4µs sampling period for the counter and decimation by 5 at the SINC³ filter is a compromise, mostly driven by the capacity of the SAMRH71 to process the high sampling rate part of the SINC³ at 4µs intervals. The radiation tolerant SAMV71Q21RT offers more CPU capability, and SNR can be optionally improved for this MCU by reducing the decimation performed by the SINC¹ counter and increasing the decimation performed by the SINC³ digital filter.

Table 2. SAMRH71F20 Resource Mapping and LX7720 Functionality

LX7720 Signal	LX7720 Function	SAMRH71 Function	Pin	Timer
Motor Phase Waveform Generation				
LD_IN_A	Motor phase A lower FET PWM	PWMC0_PWML0	PA4	TC0
UD_IN_A	Motor phase A upper FET PWM	PWMC0_PWMH0	PA0	TC0
LD_IN_B	Motor phase B lower FET PWM	PWMC0_PWML1	PA5	TC0
UD_IN_B	Motor phase B upper FET PWM	PWMC0_PWMH1	PA1	TC0
LD_IN_C	Motor phase C lower FET PWM	PWMC0_PWML2	PA6	TC0
UD_IN_C	Motor phase C upper FET PWM	PWMC0_PWMH2	PA2	TC0
Motor Phase Current Acquisition				
SNS_OUT_A	Motor phase A current ΔΣ serial stream	TCLK9	PC21	TC3
SNS_OUT_B	Motor phase B current ΔΣ serial stream	TCLK10	PC28	TC3
SNS_OUT_C	Motor phase C current ΔΣ serial stream	TCLK11	PC25	TC3
Motor Quadrature Encoder Acquisition				
BLO1	Bi-level (comparator) output 1. Quadrature encoder output A is connected to BLI1	TIOA3 using QDEC module	PB9	TC1
BLO2	Bi-level (comparator) output 2. Quadrature encoder output B is connected to BLI2	TIOB3 using QDEC module	PB10	TC1
LX7720 Clock Generation				
CP_CLK	150kHz charge pump clock	Programmable clock PCK2	PA10	-
MOD_CLK	25MHz ΔΣ modulator clock	Programmable clock PCK0	PA11	-
LED Drive Signals				
-	-	GPIO output - LED drive 1	PB15	-
-	-	GPIO output - LED drive 2	PB16	-
LX7720 Status Outputs and RESET Input				
PR_FAULT	Power rail fault logic output	GPIO input	PA8	-
OC_FAULT	Over current fault logic output	GPIO input	PA9	-
OTW_FAULT	Over temperature fault logic output	GPIO input	PC9	-
RESET	Fault reset logic input	GPIO output	PC10	
LX7720 Switch Inputs				
RESET	Reset push switch, active low	GPIO input	PA20	-
DIRECTION	Direction push switch, active low	GPIO input	PA21	-
START/STOP	Start/Stop push switch, active low	GPIO input	PA22	-
INCREASE SPEED	Increase Speed push switch, active low	GPIO input	PA23	-
DECREASE SPEED	Decrease Speed push switch, active low	GPIO input	PA24	-

2 Revision History

2.1 Revision 1 - May 2023

First release.

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