

## Introduction

The SDRAM controller module on the SAM E70/S70/V70/V71 microcontroller unit (MCU) family was intended to enable interfacing external memory devices to address higher memory requirements for handling code or data (graphics, audio, and so on) in large and feature-rich embedded applications.

The SDRAM usage on the SAM E70/S70/V70/V71 MCUs is not suggested in new designs as the SDRAM Controller is not functional. The SDRAM support has been removed from all versions of SAM E70/S70/V70/V71 devices. Microchip does not guarantee the functionality of the SDRAM Controller, and the SDRAM Controller could cause issues with the functionality of the parts.

This document describes alternative solutions for applications with larger memory requirements.

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## 1. Alternatives to the SDRAM Interface

The following sections describe the microcontroller, memory, and microprocessor (MPU) alternatives to address the requirement of external SDRAM.

### 1.1 MCU Alternatives

The superset of devices in the MCU families, provided in the following table, have comparable or compatible features that can be considered as alternatives to the SDRAM interface on the SAM E70/S70/V70/V71 family of devices.

**Table 1-1.** MCU Family Devices

SI No	MCU Family	Core	SRAM	Flash	Processor Speed	Additional Memory Options	Suggested Parts	Parametric Search Link/ Keyword	MPLAB Harmony v3 Usage Example(s)
1.	SAM E70/S70/V70/V71	Cortex®-M7	384 KB	2048 KB	300 MHz	QSPI (2), EBI(1)	<a href="#">ATSAME70Q21</a> <a href="#">ATSAMS70Q21</a> <a href="#">ATSAMV70Q20</a> <a href="#">ATSAMV71Q21</a>	<a href="#">SAME70</a> <a href="#">SAMS70</a> <a href="#">SAMV70</a> <a href="#">SAMV71</a>	QSPI Memory usage example(s)
2.	PIC32MZ DA	MIPS32 microAptiv™	640 KB	2048 KB	200 MHz	DRAM (DDR2) (3), EBI(1)	<a href="#">PIC32MZ2064DAS176</a> <a href="#">PIC32MZ2064DAR176</a>	<a href="#">PIC32MZ DA</a>	DDR Memory usage example(s)
3.	PIC32MZ EF	MIPS32 microAptiv	512 KB	2048 KB	200 MHz	SQI (4), EBI(1)	<a href="#">PIC32MZ2048EFM144</a> <a href="#">PIC32MZ2048EFH144</a>	<a href="#">PIC32MZ EF</a>	SQI Memory usage example(s)
4.	PIC32CZ CA	Cortex®-M7	1MB/512KB	8MB/2 MB	300MHz	SQI(5), EBI(1)	<a href="#">PIC32CZ8110CA90208</a> <a href="#">PIC32CZ8110CA80208</a> <a href="#">EA60E74A</a>	<a href="#">PIC32CZ</a>	SQI memory example

**Notes:**

- Static Memory Controller (SMC) is part of the External Bus Interface (EBI) peripheral, providing a 16-bit interface with support for SRAM, PSRAM, PROM, EPROM, EEPROM, LCD module, NOR Flash, and NAND Flash.
- Quad I/O Serial Peripheral Interface (QSPI) enables interfacing up to 256 MB Flash with an eExecute-In-Place feature and RAM.
- Extended memory through the internal 32 MB DRAM (DDR2) or externally connected DRAM (DDR2) of 128 MB.
- The Serial Quad Interface (SQI) helps to communicate with memory devices, such as serial EEPROMs, serial Flash devices, and SPI RAM devices at 50 MHz rates.
- The SQI helps to communicate with memory devices, such as serial EEPROMs, serial Flash devices, and SPI RAM devices with interfacing upto 256MB/512MB.

## 1.2 MPU Alternatives

Microchip 32-bit MPUs are a natural extension to 32-bit MCUs and suitable for applications with large external memory requirements. They support multiple memory types, such as DDR2, DDR3, LPDDR2, LPDDR3, QSPI, and eMMC Flash.

The devices in the MPU family, as provided in the figure below, have comparable or compatible features that can be considered as an alternative to the SDRAM interface on the SAME70/S70/V70/V71 family of devices.

**Table 1-2.** MPU Family Devices

SI No	MPU Family	Core	SRAM	Flash	Processor Speed	Additional Memory Options	Packages	Suggested Parts	Parametric Search Link	MPLAB Harmony v3 Usage Example(s)
1.	<b>SAMA5D2</b>	Cortex-A5	N/A	N/A	500 MHz	DDR2 DDR3L LPDDR2 LPDDR3 QSPI eMMC	289-ball LFBGA, 14x14 mm <sup>2</sup> , 1.4 mm thickness, 0.8 mm pitch 256-ball TFBGA, 8x8 mm <sup>2</sup> , 1.05 mm thickness, 0.4 mm pitch 196-ball TFBGA, 11x11 mm <sup>2</sup> , 0.75 mm thickness, 0.75 mm pitch	<a href="#">ATSAMA5D21</a>	<a href="#">SAMA5D2</a>	<a href="#">DDR2 usage example(s) (1,2,3)</a>
2.	<b>SAM9X60</b>	<a href="#">ARM926</a>	64 KB	N/A	600 MHz	LPDDR DDR2 SDRAM LPSDR QSPI eMMC	228-ball TFBGA, 11x11 mm <sup>2</sup> , 0.65mm pitch	<a href="#">SAM9X60</a>	<a href="#">SAM9X60</a>	<a href="#">DDR2 usage example(s)<sup>(3)</sup></a>

**Notes:**

1. The example link is for the SAM9X60 MPU. It can be easily adapted to the SAMA5D2 MPU family as MPLAB Harmony v3 supports the RAM FS (file system) for the SAMA5D2 family.
2. SAMA5D2 Boot Process: [microchipdeveloper.com/32mpu:boot-sama5d2-series](http://microchipdeveloper.com/32mpu:boot-sama5d2-series).
3. The above two families support Internal SDRAM. For additional information about MPUs that support other memory interfaces, refer to the [www.microchip.com/en-us/products/microprocessors/32-bit-mpus](http://www.microchip.com/en-us/products/microprocessors/32-bit-mpus).

## 2. References

For additional information regarding Microchip products and services, visit the Microchip [Website](#), or contact a local Microchip sales representative.

- The MPLAB Harmony v3 Quick Docs repository provides standalone help pages for users to get started developing applications on Microchip's 32-bit SAM and PIC32 MCUs. Start from the `index.html` present in the docs folder.  
The online version is available at: [microchip-mplab-harmony.github.io/quick\\_docs/](https://microchip-mplab-harmony.github.io/quick_docs/)
- [MPLAB Harmony Landing page](#)
- [Getting Started with MPLAB Harmony v3 Peripheral Libraries on SAM E70/S70/V70/V71 MCUs](#)
- [Getting Started with MPLAB Harmony v3 Drivers and System Services on SAM E70/S70/V70/V71 MCUs](#)
- [Getting Started with MPLAB Harmony v3 Drivers on SAM E70/S70/V70/V71 MCUs using FreeRTOS](#)
- [Getting Started with MPLAB Harmony v3 Peripheral Libraries on PIC32MZ EF MCUs](#)
- [Getting Started with MPLAB Harmony v3 Drivers and Middleware on PIC32MZ EF MCUs using FreeRTOS](#)
- [MPLAB Harmony v3 Developer Help page](#)

### 3. Revision History

#### Revision B - 09/2024

The following updates were performed for this revision:

- Updated the [MCU Family Devices](#) table in [MCU Alternatives](#) to reflect new packages and new MCU lines
- Updated the [MPU Family Devices](#) table in [MPU Alternatives](#) with a new note
- Removed an erroneous reference from [References](#)

#### Revision A - 08/2022

This is the initial release of this document.

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