Section 58. Data EEPROM

HIGHLIGHTS

This section of the manual contains the following major topics:

Note: This family reference manual section is meant to serve as a complement to device data sheets. Depending on the device variant, this manual section may not apply to all PIC32 devices.

Please consult the note at the beginning of the **"Data EEPROM"** chapter in the current device data sheet to check whether this document supports the device you are using.

Device data sheets and family reference manual sections are available for download from the Microchip Worldwide Web site at: http://www.microchip.com

58.1 INTRODUCTION

This family reference manual describes the Data EEPROM module in the PIC32 family of devices.

Data EEPROM memory is accessed through a Special Function Register (SFR) interface. The size of Data EEPROM memory may vary by device.

58.2 CONTROL REGISTERS

Data EEPROM read and write operations are controlled using the following Special Function Registers (SFRs):

- **EECON: EEPROM Control Register**

  This is the primary register for all Data EEPROM access. This register provides both command and status functionality.

- **EEKEY: EEPROM Key Register**

  This write-only register is used to implement an unlock sequence to prevent accidental writes or erasure of EEPROM memory.

- **EEADDR: EEPROM Address Register**

  The address of each Data EEPROM command is selected by writing to the EEADDR register.

- **EEDATA: EEPROM Data Register**

  This register will contain the data being read from the Data EEPROM after a read cycle. Prior to a Data EEPROM write cycle, data is written to the EEDATA register.
- **DEVEE0: EEPROM Packed Calibration Value 1 and Value 0 Register**

  This register contains calibration values that are written to the Data EEPROM module prior to its use.
- **DEVEE1: EEPROM Packed Calibration Value 3 and Value 2 Register**

  This register contains calibration values that are written to the Data EEPROM module prior to its use.
- **DEVEE2: EEPROM Packed Calibration Value 5 and Value 4 Register**

  This register contains calibration values that are written to the Data EEPROM module prior to its use.
- **DEVEE3: EEPROM Packed Calibration Value 7 and Value 6 Register**

  This register contains calibration values that are written to the Data EEPROM module prior to its use.

Table 58-1 provides a brief summary of the related Data EEPROM module registers. Corresponding registers appear after the summary, followed by a detailed description of each bit.

Table 58-1: Data EEPROM SFR Summary

Name		Bit 31/15	Bit 30/14	Bit 29/13	Bit 28/12	Bit 27/11	Bit 26/10	Bit 25/9	Bit 24/8	Bit 23/7	Bit 22/6	Bit 21/5	Bit 20/4	Bit 19/3	Bit 118/2	Bit 17/1	Bit 16/0
EECON[(1)]	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
	15:0	ON	RDY	SIDL	ABORT	—	—	—	—	RW	WREN	ERR<1:0>		ILW	CMD<2:0>		
EEKEY[(2)]	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
	15:0	EEKEY<15:0>															
EEADDR[(1,3)]	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
	15:0	—	—	—	—	EEADDR<11:0>											
EEDATA	31:16	EEDATA<31:16>															
	15:0	EEDATA<15:0>															
DEVEE0[(4)]	31:16	EEPCAL1<15:0>															
	15:0	EEPCAL0<15:0>															
DEVEE1[(4)]	31:16	EEPCAL3<15:0>															
	15:0	EEPCAL2<15:0>															
DEVEE2[(4)]	31:16	EEPCAL5<15:0>															
	15:0	EEPCAL4<15:0>															
DEVEE3[(4)]	31:16	EEPCAL7<15:0>															
	15:0	EEPCAL6<15:0>															

Legend: — = unimplemented, read as ‘0’.

Note 1: This register has an associated Clear, Set, and Invert register at an offset of 0x4, 0x8, and 0xC bytes, respectively. These registers have the same name, with CLR, SET, or INV appended to the end of the register name (e.g., EECONCLR). Writing a ‘1’ to any bit position in these registers will clear, set, or invert valid bits in the associated register. Reads from the these registers should be ignored.

2: This register is a write-only register. Reads always result in ‘0’.

3: Because the EEPROM word size is 32 bits, for reads and writes the last two bits (EEADDR<1:0>) must always be ‘0’.

4: This register is not available on all devices. Refer to the **“Data EEPROM”** chapter in the specific device data sheet to determine availability.

Register 58-1: EECON: EEPROM Control Register

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0, HC	R-0	R/W-0	R/W-0, HC	U-0	U-0	U-0	U-0
	ON	RDY	SIDL	ABORT	—	—	—	—
7:0	R/W-0, HC	R/W-0	R/W-0, HS, HC	R/W-0, HS, HC	R/W-0, HS	R/W-0	R/W-0	R/W-0
	RW	WREN(1)	ERR<1:0>		ILW	CMD<2:0>(1)		

Legend:	HS = Hardware settable	HC = Hardware clearable
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared

bit 31-16 **Unimplemented:** Read as ‘0’

bit 15 **ON:** Data EEPROM Power Control bit

1 = Data EEPROM is enabled
0 = Data EEPROM is disabled

Attempting to clear this bit will have no effect if the RW bit is set. In addition, this bit is not cleared during Sleep if the FSLEEP bit in the DEVCFG register is set.

bit 14 **RDY:** Data EEPROM Ready bit

1 = Data EEPROM is ready for access
0 = Data EEPROM is not ready for access

RDY is cleared by hardware whenever a POR or BOR event occurs. It is set by hardware when the ON bit = 1 and the power-up timer has expired.

bit 13 **SIDL:** Stop in Idle Mode bit

1 = Discontinue operation when CPU enters in Idle mode
0 = Continue operation in Idle mode

bit 12 **ABORT:** Data EEPROM Abort Operation Control bit

1 = Set by software to abort the on-going write command as soon as possible
0 = Data EEPROM panel is ready/Normal operation

bit 11-8 **Unimplemented:** Read as ‘0’

bit 7 **RW:** Start Command Execution Control bit

When WREN = 1:

1 = Start memory word program or erase command
0 = Cleared by hardware to indicate program or erase operation has completed

When WREN = 0:

1 = Start memory word read command
0 = Cleared by hardware to indicate read operation has completed

This bit cannot be set if the ON bit = 0, or if the ON bit = 1 and the power-up timer has not yet expired. A BOR reset will indirectly clear this bit by forcing any executing command to terminate and to clear RW afterwards.

bit 6 **WREN:** Data EEPROM Write Enable Control bit(1)

1 = Enables program or erase operations
0 = Disables program or erase of memory elements, and enables read operations

Note 1: This bit cannot be modified when the RW bit = 1.

Register 58-1: EECON: EEPROM Control Register (Continued)

bit 5-4 **ERR<1:0>:** Data EEPROM Sequence Error Status bits

11 = A BOR event has occurred
10 = An attempted execution of a read or write operation with an invalid write OR command with a misaligned address (EEADDR<1:0> ≠ 00)
01 = A Bulk or Page Erase or a Word Program verify error has occurred
00 = No error condition

These bits can be cleared by software, or as the result of the successful execution of the next operation, or when the ON bit = 0. These bits may also be set by software (when the RW bit = 0) without affecting the operation of the module.

bit 3 **ILW:** Data EEPROM Imminent Long Write Status bit

1 = The next write to the EEPROM address (held in the EEADDR register) will require more time (~ 20 ms) than usual
0 = The next write to the EEPROM address (held in the EEADDR register) will be a normal write cycle

This bit can be cleared by software, or as the result of a write to the EEADDR register. This bit is set by hardware after a write command.

bit 2-0 **CMD<2:0>:** Data EEPROM Command Selection bits(1)

111 = Reserved
•
•
•
100 = Configuration register Write command (WREN bit must be set)
011 = Data EEPROM memory Bulk Erase command (WREN bit must be set)
010 = Data EEPROM memory Page Erase command (WREN bit must be set)
001 = Word Write command (WREN bit must be set)
000 = Word Read command (WREN bit must be clear)

Note 1: This bit cannot be modified when the RW bit = 1.

Register 58-2: EEKEY: EEPROM Key Register

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0
	EEKEY<15:8>							
7:0	W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0
	EEKEY<7:0>							

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared

bit 31-16 **Unimplemented:** Read as ‘0’

bit 15-0 **EEKEY<15:0>:** Data EEPROM Key bits

Writing the value 0xEDB7 followed by writing the value 0x1248 to this register will unlock the EECON register for write or erase operations. Reads have no effect on this register and return ‘0’.

Writing any other value will lock the EECON register.

Register 58-3: EEADDR: EEPROM Address Register

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	EEADDR<11:8>(1)			
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	EEADDR<7:0>(1)							

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared

bit 31-12 **Unimplemented:** Read as ‘0’

bit 11-0 **EEADR<11:0>:** Data EEPROM Address bits(1)

This register holds the address in the EEPROM memory upon which to operate. EEADDR<1:0> must always be ‘00’ when the RW bit (EECON<7>) is set or an error will occur.

Note 1: The bits in this register cannot be modified when the RW bit (EECON<7>) = 1.

Register 58-4: EEDATA: EEPROM Data Register

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	EEDATA<31:24>(1)							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	EEDATA<23:16>(1)							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	EEDATA<15:8>(1)							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	EEDATA<7:0>(1)							

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared

bit 31-0 **EEDATA<31:0>:** Data EEPROM Data bits(1)

This register holds the data in the EEPROM memory to store during write operations, or the data from memory after a read operation.

Note 1: These bits cannot be modified when the RW bit (EECON<7>) = `1`. In addition, reading this register, when the RW bit = `1` may not return valid data, as the read operation may not have completed.

Register 58-5: DEVEE0: EEPROM Packed Calibration Value 1 and Value 0 Register

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R	R	R	R	R	R	R	R
	EEPCAL1<15:8>							
23:16	R	R	R	R	R	R	R	R
	EEPCAL1<7:0>							
15:8	R	R	R	R	R	R	R	R
	EEPCAL0<15:8>							
7:0	R	R	R	R	R	R	R	R
	EEPCAL0<7:0>							

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared

bit 31-8 **EEPCAL1<15:0>:** Data EEPROM Packed Calibration Value 1 bits

These bits contain calibration values that are written to the Data EEPROM module prior to its use.

bit 7-0 **EEPCAL0<15:0>:** Data EEPROM Packed Calibration Value 0 bits

These bits contain calibration values that are written to the Data EEPROM module prior to its use.

Note 1: The values in this register must be written to the Data EEPROM module through the Configuration Write command (see **58.3.1 “Data EEPROM Initialization”**).

2: This register is not available on all devices. Refer to the **“Data EEPROM”** chapter in the specific device data sheet to determine availability of this register.

Register 58-6: DEVEE1: EEPROM Packed Calibration Value 3 and Value 2 Register

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R	R	R	R	R	R	R	R
	EEPCAL3<15:8>							
23:16	R	R	R	R	R	R	R	R
	EEPCAL3<7:0>							
15:8	R	R	R	R	R	R	R	R
	EEPCAL2<15:8>							
7:0	R	R	R	R	R	R	R	R
	EEPCAL2<7:0>							

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared

bit 31-8 **EEPCAL3<15:0>:** Data EEPROM Packed Calibration Value 3 bits
These bits contain calibration values that are written to the Data EEPROM module prior to its use.

bit 7-0 **EEPCAL2<15:0>:** Data EEPROM Packed Calibration Value 2 bits
These bits contain calibration values that are written to the Data EEPROM module prior to its use.

Note 1: The values in this register must be written to the Data EEPROM module through the Configuration Write command (see **58.3.1 “Data EEPROM Initialization”**).

2: This register is not available on all devices. Refer to the **“Data EEPROM”** chapter in the specific device data sheet to determine availability of this register.

Register 58-7: DEVEE2: EEPROM Packed Calibration Value 5 and Value 4 Register

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R	R	R	R	R	R	R	R
	EEPCAL5<15:8>							
23:16	R	R	R	R	R	R	R	R
	EEPCAL5<7:0>							
15:8	R	R	R	R	R	R	R	R
	EEPCAL4<15:8>							
7:0	R	R	R	R	R	R	R	R
	EEPCAL4<7:0>							

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared

bit 31-8 **EEPCAL5<15:0>:** Data EEPROM Packed Calibration Value 5 bits
These bits contain calibration values that are written to the Data EEPROM module prior to its use.

bit 7-0 **EEPCAL4<15:0>:** Data EEPROM Packed Calibration Value 4 bits
These bits contain calibration values that are written to the Data EEPROM module prior to its use.

Note 1: The values in this register must be written to the Data EEPROM module through the Configuration Write command (see **58.3.1 “Data EEPROM Initialization”**).

2: This register is not available on all devices. Refer to the **“Data EEPROM”** chapter in the specific device data sheet to determine availability of this register.

Register 58-8: DEVEE3: EEPROM Packed Calibration Value 7 and Value 6 Register

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R	R	R	R	R	R	R	R
	EEPCAL7<15:8>							
23:16	R	R	R	R	R	R	R	R
	EEPCAL7<7:0>							
15:8	R	R	R	R	R	R	R	R
	EEPCAL6<15:8>							
7:0	R	R	R	R	R	R	R	R
	EEPCAL6<7:0>							

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared

bit 31-8 **EEPCAL7<15:0>:** Data EEPROM Packed Calibration Value 7 bits

These bits contain calibration values that are written to the Data EEPROM module prior to its use.

bit 7-0 **EEPCAL6<15:0>:** Data EEPROM Packed Calibration Value 6 bits

These bits contain calibration values that are written to the Data EEPROM module prior to its use.

Note 1: The values in this register must be written to the Data EEPROM module through the Configuration Write command (see **58.3.1 “Data EEPROM Initialization”**).

2: This register is not available on all devices. Refer to the **“Data EEPROM”** chapter in the specific device data sheet to determine availability of this register.

58.3 DATA EEPROM OPERATION

On device power-up, the ON bit (EECON<15>) will be clear. Power is disconnected from the Data EEPROM and the Data EEPROM is in its lowest power mode.

When the ON bit is set, power is applied to the Data EEPROM. After a power-up timer delay has expired, the RDY bit (EECON<14>) is set by hardware, and the Data EEPROM is ready to be accessed.

Once ready for access (RDY = 1), all read and write operations are executed using the Data EEPROM registers. In all cases, the Data EEPROM is ready to read or write data only when RDY = 1 and there is no ongoing command (RW bit (EECON<7>) = 0).

Access to the Data EEPROM may be disabled by its associated Peripheral Module Disable (PMD) bit or by clearing the ON bit. Please refer to the **"Power-Saving Features"** chapter in the specific device data sheet to determine which PMD register and bit controls the power to the EEPROM.

58.3.1 Data EEPROM Initialization

58.3.1.1 DATA EEPROM INITIALIZATION AFTER A POR EVENT

After a POR event, the ON bit is clear, and the Data EEPROM is powered down. To enable the Data EEPROM, set the ON bit = 1, and wait for the RDY bit to be set by hardware.

Before accessing the EEPROM at full speed, it is necessary to program configuration values into the Data EEPROM module after enabling it. This is done through the Configuration Write command (CMD<2:0> bits (EECON<2:0>) = 100).

The configuration values to be written to the Data EEPROM module are stored in the DEVEE0, DEVEE1, DEVEE2 and DEVEE3 registers.

When writing the configuration values, the WREN bit (EECON<6>) must be set. Therefore, an unlock sequence must be used. Example 58-1 Data EEPROM Initialization Code provides a code example of unlocking the Data EEPROM and writing the configuration values after powering on the Data EEPROM.

58.3.1.2 DATA EEPROM INITIALIZATION AFTER A BOR EVENT

After a BOR event, the Data EEPROM remains powered-up (ON = 1) if it was powered-up prior to the BOR event. The ERR<1:0> bits (EECON<5:4>) will contain '11', which indicates a BOR event has occurred. The RDY bit will be clear. Wait for the RDY bit to be set by hardware before accessing the Data EEPROM.

58.3.1.3 DATA EEPROM INITIALIZATION AFTER NON-POR, NON-BOR EVENTS

After a non-POR or non-BOR event, the Data EEPROM will remain powered-up (ON = 1) if it was powered-up prior to the event. The RDY bit will remain set if it was previously set. For non-POR or non-BOR events, the EEPROM will complete its last command. User software need only wait for the completion of any ongoing command before proceeding.

Example 58-1: Data EEPROM Initialization Code

```
void EEWriteExecute(int waitForDone)
{
/* Disable interrupts prior to unlock sequence */
EEKEY = 0xEDB7; // Unlock the EEPROM to enable writing
EEKEY = 0x1248;
EECONbits.RW = 1; // Execute the write
/* Re-enable interrupts */
if (waitForDone) // Wait for the write to finish if
while (EECONbits.RW); // desired
}

void EEInitialize(void) // Basic EEPROM enable and initialization
{
EECONbits.ON = 1;// Turn on the EEPROM
while (EECONbits.RDY == 0);// Wait until EEPROM is ready (~125 us)
EECONbits.WREN = 1;// Enable writing to the EEPROM
EECONbits.CMD = 0b100;// Set the command to Configuration Write
EEADDR = 0x00;// Addr 0x00 = DEVEE0;
EEDATA = DEVEE0;
EEWriteExecute(1); // Execute write and wait for finish
EEADDR = 0x04;// Addr 0x04 = DEVEE1;
EEDATA = DEVEE1;
EEWriteExecute(1); // Execute write and wait for finish
EEADDR = 0x08;// Addr 0x08 = DEVEE2;
EEDATA = DEVEE2;
EEWriteExecute(1); // Execute write and wait for finish
EEADDR = 0x0C;// Addr 0x0C = DEVEE3;
EEDATA = DEVEE3;
EEWriteExecute(1); // Execute write and wait for finish
EECONbits.WREN = 0; // Turn off writes.
}
```

58.3.2 Data EEPROM Read Command

Prior to reading the Data EEPROM, the Data EEPROM must be enabled and the RDY status bit (EECON<14>) must be set by hardware. There can be no ongoing command (RW bit (EECON<7>) = 0) when a new command is issued to the Data EEPROM.

Do the following to execute a Data EEPROM read command:

1. Load the Data EEPROM address to be read (i.e., EEADDR = 0x100). The address must be on a 32-bit boundary so that the last two bits (EEADDR<1:0>) must be ‘00’.
2. Load the read command into the CMD<2:0> bits (i.e., EECONbits.CMD = 0x0).
3. Clear the WREN bit to enable for read access (i.e., EECONbits.WREN = 0).
4. Set the RW bit to begin the read (i.e., EECONbits.RW = 1).
5. Wait until the read cycle is complete and hardware clears the RW bit (i.e., while (EECONbits.RW = 1)).
6. Read the data from the EEDATA register (i.e., variable = EEDATA).
7. If an error occurred, ERR<1:0> will contain the error code.

Example 58-2: Data EEPROM Read Command Code

```
#define EEPROM_NOT_READY 8
/*
 * Function returns ERR<1:0> bits or EEPROM_NOT_READY.
 * Requested data is stored in ee_data
 * Returns zero = no error occurred during the read cycle
 * non-zero = error occurred during the read cycle
 * or Data EEPROM is not ready
 */
int data_EEPROM_read(unsigned int ee_addr, int *ee_data)
{
    if (EECONbits.RDY==1)                // If Data EEPROM to be ready
    {
        if (EECONbits.RW==0)             // If no operation underway
        {                                // Execute Read Command
            EEADDR = ee_addr & 0xFFC;    // Set address on 32-bit boundary
            EECONbits.CMD = EEWORDREAD;  // Load CMD<2:0> with
                                         // Data EEPROM read command
            EECONbits.WREN = 0;          // Access for read
            EECONbits.RW = 1;            // Start the operation

            while (EECONbits.RW==1);     // Wait until read is complete
            *ee_data = EEDATA;           // Read the data

            return EECONbits.ERR;
        }
    }
    return EEPROM_NOT_READY;
}
```

Software can clear the RW bit while it is set for a read command. This will abort a read command.

- Data in the EEDATA register may be invalid after the read command is aborted
- There will be no error reported as a result of aborting a read command
- No read complete interrupt will occur as a result of aborting a read command

While the RW bit is set, writes to the EECON (other than ABORT) and EEADDR registers will be ignored.

The only error that can be returned by a read command is “invalid command” (ERR<1:0> = 10), which would occur if EEADDR is not on a 32-bit boundary.

58.3.3 Data EEPROM Write Command

Prior to writing to the Data EEPROM, it must be enabled and the RDY status bit (EECON<14>) must be set by hardware. There can be no ongoing command (RW bit (EECON<7>) = 0) when a new command is issued to the Data EEPROM.

Do the following to execute a Data EEPROM write command:

1. Load the Data EEPROM address to be write (i.e., EEADDR = 0x100).
2. Set the WREN bit to enable for write access (i.e., EECONbits.WREN = 1).
3. Load the program command into the CMD<2:0> bits (i.e., EECONbits.CMD = 0x01).
4. Load the data to be written into the EEDATA register (i.e., EEDATA = 0x13572468).
5. Execute the Data EEPROM unlock sequence using the EEKEY register.
6. Set the RW bit to begin the word write (i.e., EECONbits.RW = 1).
7. Wait until the read cycle is complete and hardware clears RW (i.e., while (EECONbits.RW = 1)).
8. If an error occurred, ERR<1:0> will contain the error code.

Example 58-3: Data EEPROM Write Command Code

```
#define EEPROM_NOT_READY 8
/*
 * Function returns ERR<1:0> bits
 * Returns zero = no error occurred during the write cycle
 * non-zero = error occurred during the write cycle
 * or Data EEPROM is not ready
 */
int data_EEPROM_write(unsigned int ee_addr, int ee_data)
{
    if (EECONbits.RDY==1)             // If Data EEPROM to be ready
    {
        if (EECONbits.RW==0)          // If no operation underway
        {                             // Execute Write Command
            EEADDR = ee_addr & 0xFFC; // Load address on a 32-bit boundary
            EECONbits.CMD = EEWORDPGM;// Load CMD<2:0> with write command
            EECONbits.WREN = 1;       // Access for write
            EEDATA = ee_data;

            EEKEY = 0xED87;           // Write unlock sequence
            EEKEY = 0x1248;

            EECONbits.RW = 1;         // Start the write cycle

            while (EECONbits.RW==1);
            //Wait for write cycle to complete

            // Return ERR<1:0> bits. Zero if no error.
            return EECONbits.ERR;
        }
    }
    return EEPROM_NOT_READY;
}
```

Unlike the read command, the write command cannot be aborted by software. During a write cycle, any software attempt to write to the EECON register will be ignored.

CAUTION

The user must ensure that no attempt is made to concurrently write/erase user program Flash (associated with the NVM registers) and the Data EEPROM. **Failure to observe this limitation may result in a write failure of one or both targets.**

58.3.3.1 WORD WRITE CYCLE TIMING VARIATIONS

When data is written to the Data EEPROM while executing time-critical applications, the user should consider Data EEPROM write command timing variations.

The first 16 writes to a single EEPROM address take approximately 20 µs each. The seventeenth write cycle, and every sixteenth write cycles thereafter, will require a longer write cycle, taking approximately 20 ms.

The entire 20 µs or 20 ms period is considered a write cycle period. During this period, as with all write cycle periods, the RW bit (EECON<7>) remains high and no new Data EEPROM commands may be attempted until the RW bit is cleared by hardware.

58.3.3.2 MANAGING THE LONG WRITE CYCLE

The EEPROM logic requires a longer duration to erase the memory cell before writing the new data on the seventeenth write cycle and every sixteenth write cycle thereafter. This period is significantly longer than the majority of write cycles, which is referred to as a “long write cycle.”

The Data EEPROM logic provides management assistance when this long write cycle occurs. The Imminent Long Write Status (ILW) bit (EECON<3>), will be set following a write cycle when the next write to the same EEPROM address requires a long write cycle.

The user can choose to ignore the ILW bit, and the 20 ms period will occur on the next write cycle to that specific EEPROM address.

For time-critical applications, using the Data EEPROM interrupts with a corresponding Interrupt Service Routine (ISR), may have some advantages over waiting for completion of a write command in a loop.

Alternately, user software can examine the ILW bit after each word write to the Data EEPROM and chose to incur this 20 ms period at a time more convenient for the user application. By rewriting the same data (or new data) to the same address, the “long write cycle” occurs when the user software chooses, rather than at a random point in the future.

As shown in Example 58-4 Data EEPROM Recommended Procedure to Hasten a Long Write Cycle , the function writes data to the EEPROM. If the ILW bit is set after the first write, a second write initiates the long write cycle.

Example 58-4: Data EEPROM Recommended Procedure to Hasten a Long Write Cycle

```
/*
 * Function returns ERR bits
 * Called to write data.
 * The first write cycle is always a short write cycle.
 * If ILW is set after the first write,
 *    a second write is initiated to force the long write cycle.
 * Returns zero = no error occurred during the write cycle
 *        non-zero = error occurred during the write cycle
 *                   or Data EEPROM is not ready
 */
int data_EEPROM_write_managed_long_cycle(unsigned int ee_addr,
                                                  int ee_data)
{
    int ret_err;

    ret_err = data_EEPROM_write(ee_addr, ee_data); //short write cycle

    if ((EECONbits.ILW == 1) && (ret_err == 0))
    {
        // Rewrite the data to the same location if ILW==1
        // This forces the long write cycle.
        // It will take ~20 ms to complete
        ret_err = data_EEPROM_write(ee_addr, ee_data);
    }

    return ret_err;
}
```

58.3.4 Data EEPROM Forced Word Erase

Under normal conditions, there is no need to attempt a Forced Word Erase. The Data EEPROM has internal logic which automatically manages all read/erase/write command sequences. Software execution of the Forced Word Erase command should be used in response to write verification errors (ERR<1:0> = 01 after a write).

In the event a verification error occurs during a write to the Data EEPROM, the user can attempt a Forced Word Erase command.

As shown in Example 58-5 Data EEPROM Forced Word Erase Code , the Forced Word Erase command is similar to the write command except the CMD<2:0> bits (EECON<2:0>) = 010 and no data is written to EEDATA.

Example 58-5: Data EEPROM Forced Word Erase Code

```
#define EEPROM_NOT_READY 8
/*
 * Function returns ERR<1:0> bits
 * Returns zero = no error occurred, word erased properly
 * non-zero = error occurred, word may have fixed bits
 * or Data EEPROM is not ready
 */
int data_EEPROM_forced_word_erase(unsigned int addr)
{
    if (EECONbits.RDY==1)             // If Data EEPROM to be ready
    {
        if (EECONbits.RW==0)          // If no operation underway
        {                             // Execute erase command
            EEADDR = ee_addr;
            EECONbits.CMD = EEPAGEERASE; // Load CMD<2:0> with erase command
            EECONbits.WREN = 1;       // Access for write or erase

            EEKEY = 0xED87;           // Write unlock sequence
            EEKEY = 0x1248;

            EECONbits.RW = 1;         // Start the erase cycle

            while (EECONbits.RW==1);
            //Wait for erase cycle to complete

            // Return ERR<1:0> bits. Zero if no error.
            return EECONbits.ERR;
        }
    }
    return EEPROM_NOT_READY;
}
```

Unlike the read command, the forced word erase command cannot be aborted by software. During an erase cycle, any software attempt to write to the EECON register will be ignored.

CAUTION

The user must ensure that no attempt is made to concurrently write/erase user program Flash (associated with the NVM registers) and the Data EEPROM. **Failure to observe this limitation may result in a write failure of one or both targets.**

58.3.5 Data EEPROM Bulk Erase

As shown in Example 58-6 Data EEPROM Bulk Erase Code , the Bulk Erase command is similar to the write command except the CMD<2:0> bits (EECON<2:0>) = 011 and no data is written to EEDATA.

Example 58-6: Data EEPROM Bulk Erase Code

```
#define EEPROM_NOT_READY 8
/*
 * Function returns ERR<1:0> bits
 * Returns zero = no error occurred, word erased properly
 * non-zero = error occurred, word may have fixed bits
 * or Data EEPROM is not ready
 */
int data_EEPROM_bulk_erase(void)
{
    if (EECONbits.RDY==1)             // If Data EEPROM to be ready
    {
        if (EECONbits.RW==0)          // If no operation underway
        {                             // Execute erase command
            EECONbits.CMD = EEBULKERASE; // Load CMD<2:0> with erase command
            EECONbits.WREN = 1;       // Access for write or erase

            EEKEY = 0xED87;           // Write unlock sequence
            EEKEY = 0x1248;

            EECONbits.RW = 1;         // Start the erase cycle

            while (EECONbits.RW==1);
            //Wait for erase cycle to complete

            // Return ERR<1:0> bits. Zero if no error.
            return EECONbits.ERR;
        }
    }
    return EEPROM_NOT_READY;
}
```

Unlike the read command, the bulk erase command cannot be aborted by software. During an erase cycle, any software attempt to write to the EECON register will be ignored.

CAUTION

The user must ensure that no attempt is made to concurrently write/erase user program Flash (associated with the NVM registers) and the Data EEPROM. **Failure to observe this limitation may result in a write failure of one or both targets.**

58.3.6 Data EEPROM Error Handling

If an error occurs during operation of the Data EEPROM, the Data EEPROM internal logic can be reinitialized by clearing the ERR<1:0> bits (EECON<5:4>).

58.3.6.1 BOR ERROR (ERR<1:0> = 11)

In a BOR event, any active command is aborted. If a write or forced word erase command was ongoing, the user should verify the data at the last write or erase address.

An error interrupt is not initiated. The RDY bit (EECON<14>) is cleared.

Wait for the RDY bit to be set by hardware, and then clear the error by clearing the ERR<1:0> bits.

For additional information, refer to **58.3.1.2 “Data EEPROM Initialization after a BOR event”**.

58.3.6.2 INVALID COMMAND (ERR<1:0> = 10)

When users initiate a command improperly or set the CMD<2:0> bits (EECON<2:0>) with a reserved command, the Data EEPROM will return the ‘Invalid Command’ error.

Examples of improperly initiated commands include:

- Initiating a Data EEPROM read command (WREN = 0 and RW = 1) when the command is not a read command (CMD<2:0> ≠ 000)
- Initiating a Data EEPROM read command (CMD<2:0> = 000 and RW = 1) when write is enabled (WREN = 1)
- Initiating a Data EEPROM read or write command when the address is not 32-bit aligned (EEADDR<1:0> ≠ 00)
- Initiating a Data EEPROM write command (WREN = 1 and RW = 1) when the command is not a write command (CMD<2:0> ≠ 001)
- Initiating a Data EEPROM write command (CMD<2:0> = 001 and RW = 1) when write is disabled (WREN = 0)

Clear the error by clearing the ERR<1:0> bits.

58.3.6.3 VERIFY ERROR (ERR<1:0> = 01)

When a Data EEPROM write or erase command is executed, internal EEPROM logic will verify the data written to the Data EEPROM or that the location has been erased. If there is an error in writing or erasing the data, this verification error will result.

In the event of a verification error, software can attempt to recover the Data EEPROM word storage location by executing the forced word erase command (CMD<2:0> = 010) at the address where the error occurred. Alternately, software may select a different Data EEPROM address to store the data.

58.4 DATA EEPROM INTERRUPTS

To enable or disable and set priority for all interrupts, refer to **Section 8. “Interrupts”** (DS60001108) in the *“PIC32 Family Reference Manual”*.

The following three interrupts are associated with the Data EEPROM:

- The Data EEPROM Error Interrupt (EEERRIF)
- The Data EEPROM Read Complete Interrupt (EERDIF)
- The Data EEPROM Write Complete Interrupt (EEWRIF)

Table 58-2: EEPROM Interrupt Conditions and Actions

Description	Condition	EEPROM Interrupt	Action
Abort of read command	While WREN = 0, RW = 1, software clears RW.	None	Next Data EEPROM command.
Read command complete	Software starts a read command. When RW is cleared by hardware, the read cycle is complete.	EERDIF	Read data from EEDATA.
Write command complete	Starts a write command. When RW is cleared by hardware, the write cycle is complete.	EEWRIF	Next Data EEPROM command.
Write command with error	ERR<1:0> = 01 Software starts a write command. Verification logic detects a write problem.	EEERRIF	Refer to **58.3.6.3 “Verify Error (ERR<1:0> = 01)”**.
Data EEPROM command error occurs	ERR<1:0> = 10	EEERRIF	Clear ERR<1:0> (ERR<1:0> = 00) to reset Data EEPROM logic. If error caused by write, verify last write.
Data EEPROM BOR Event	ERR<1:0> = 11	None	Check for BOR event on initialization of Data EEPROM. If last command was a write, verify last written data.
POR event	ON = 0	None	Initialize Data EEPROM.
BOR event	ON = 1, RDY = 0, CMD<2:0> = 111	None	Wait for RDY = 1 before accessing Data EEPROM.

58.4.1 Data EEPROM Error Interrupt (ERRIF)

The Data EEPROM Error Interrupt is triggered during the following instances:

- A page erase verify failure (during a Page Erase or Word Write command)
- A word program verify failure
- An attempt to execute an invalid command

The Data EEPROM error is indicated by ERR<1:0>!= 00.

If the Data EEPROM error interrupt is enabled, its priority must be higher than all other Data EEPROM interrupts.

Writing the EECON.ERR[1:0] = 2’b00, or successfully setting the EECON.RW = 1 (that is, initiating a subsequent command) will clear the Data EEPROM Error Interrupt.

58.4.2 Data EEPROM Read Complete (EERDIF) and Write Complete (EEWRIF)

A Data EEPROM Read Complete interrupt (EERDIF) is triggered when a read operation completes without an error (ERR<1:0> == 00). A read of the EEDATA register, or successfully setting EECON.RW = 1 (i.e. initiating a subsequent command) will clear the Data EEPROM Read Complete Interrupt.

A Data EEPROM Write Complete interrupt (EEWRIF) is triggered when a write operation completes without an error (ERR<1:0> == 00). A write to the EEDATA register, or successfully setting EECON.RW = 1 (i.e. initiating a subsequent command) will clear the Data EEPROM Write Complete Interrupt.

58.5 DATA EEPROM UNLOCK SEQUENCE

To protect the data stored in the Data EEPROM, each time a write, forced word erase, or bulk erase command is issued, an unlock sequence (see Example 58-7 Data EEPROM Unlock-for-Write Code) must be executed prior to setting the RW bit (EECON<7>).

With the WREN bit (EECON<6>) set, the RW bit cannot be set until the unlock sequence has been executed.

The unlock sequence is not necessary for a read command. Interrupts should be disabled when writing the unlock sequence to the EEKEY register to prevent a disruption of the unlock sequence.

Example 58-7: Data EEPROM Unlock-for-Write Code

```
// The Data EEPROM Unlock sequence must be executed prior to attempting a
// write or erase cycle

    EEKEY = 0xED87;        // Write unlock sequence
    EEKEY = 0x1248;
```

58.6 DATA EEPROM READ ACCESS CONTROL

There are device Configuration Bits to be aware of when setting up the Data EEPROM.

58.6.1 Wait State Configuration Register Settings (EEWS<7:0>)

The Data EEPROM read access count is the number of SYSCLK cycles used in a Data EEPROM memory access. Refer to the **"Data EEPROM"** chapter in the specific device data sheet for more information.

Select the value based on the application operating speed (FSYS). For the PIC32 device family, the setting should be 1 through 20, depending on the device speed. Refer to Table 58-3 for suggested values based on system clock speed.

Note: Setting the value to something higher than recommended will slow device reads.

Table 58-3: Data EEPROM Read Access Configuration(3)

Max System Clock (MHz)	EEWS<7:0>(1) Setting	EEPROM Access (Cycles/Read)	Read Access (Cycles)(2)	Read Access (ns)
< 200	00010011	20	109	545
< 175	00010001	18	99	566
< 150	00001110	15	84	560
< 125	00001100	13	74	592
< 100	00001001	10	59	590
< 75	00000111	8	49	653
< 50	00000100	5	34	680
< 25	00000010	3	24	960

Note 1: EEWS = EEPROM Access Time (ns) * System Frequency (MHz).

2: Due to Finite State Machine overhead, Read Access (Cycles) = [(EEWS + 2) * 5] + 4.

3: This table is provided as an example, with EEPROM Access Time = 100 ns. For device-specific details, please refer to the data sheet for your device.

58.7 OPERATION IN POWER-SAVING AND DEBUG MODES

58.7.1 Operation in Sleep Mode

When the device enters Sleep mode, the state of the EEPROM depends on the state of the FSLEEP bit in the DEVCFG registers. If FSLEEP = 1, the EEPROM will remain powered during Sleep mode, and EEPROM operations may resume as soon as the device comes out of Sleep mode.

If FSLEEP = 0, power will be removed from the EEPROM, and the ON bit (EECON<15>) will be cleared. The ON bit will have to be set, and the RDY bit (EECON<14>) will have to be set by hardware before EEPROM operations can resume.

58.7.2 Operation in Idle Mode

Idle mode has no effect on the Data EEPROM module when an operation is active.

58.7.3 Operation in Debug Mode

The Data EEPROM module does not provide debug freeze capability, therefore has no effect on the Data EEPROM module when a programming operation is active. The CPU continues to be stalled until the data operation completes. The only exception to this is the EEKEY unlock sequence, which is suspended when in Debug mode, allowing the user to single-step through the unlock sequence.

58.7.4 Peripheral Module Disable (PMD)

When the Peripheral Module Disable (PMD) bit associated with the Data EEPROM is set:

- The Data EEPROM will be immediately disabled
- Any ongoing command is immediately aborted
- Module clocks are disabled; power is disconnected from the module

It is recommended that the user disable the Data EEPROM write interrupt (if enabled) and wait until the RW bit (EECON<7>) is clear before setting the module's PMD bit. This will avoid potentially incomplete write cycles.

Example 58-8: Data EEPROM Recommended Procedure for Setting the PMD bit

```
void data_EEPROM_set_PMD( void )
{
     IEC5CLR = 1 << 26;       // Disable Data EEPROM write interrupt, if it
                              // was enabled
     while (EECONbits.RW);    // wait until last command is complete,
     PMD4bits.EEMD = 1;       // and then disable the module
}
```

58.8 EFFECTS OF VARIOUS RESETS

58.8.1 Device Reset

No EECON bits are reset on a device Reset. All other SFR bits are only reset by a POR; however, the state of the EEKEY is reset by a device Reset.

58.8.2 Power-on Reset

All Data EEPROM module registers are forced to their reset states upon a POR.

58.8.3 Watchdog and Deadman Timer Resets

All Data EEPROM module registers are unchanged upon a Watchdog or Deadman Timer Reset.

58.8.4 Factory Reset

To ensure that the Data EEPROM contents are in a known state, the device should be bulk-erased upon the very first boot (i.e., during a factory setup and test).

58.9 RELATED APPLICATION NOTES

This section lists application notes that are related to this section of the manual. These application notes may not be written specifically for the PIC32 device family, but the concepts are pertinent and could be used with modification and possible limitations. The current application notes related to the Data EEPROM module are:

Title	Application Note #
No related application notes at this time.	N/A

Note: Please visit the Microchip web site (www.microchip.com) for additional application notes and code examples for the PIC32 family of devices.

58.10 REVISION HISTORY

Revision A (April 2015)

This is the initial released version of this document.

Revision B (March 2016)

This revision includes the following updates:

- The EEPROM Packed Calibration Data Value Registers were added (see Table 58-1 and Register 58-5 through Register 58-8)
- **58.3.1 “Data EEPROM Initialization”** was updated
- The Data EEPROM Initialization Code was updated (see Example 58-1 Data EEPROM Initialization Code)
- The Data EEPROM Read Command Code was updated (see Example 58-2 Data EEPROM Read Command Code)
- The Data EEPROM Write Command Code was updated (see Example 58-3 Data EEPROM Write Command Code)
- The Data EEPROM Forced Word Erase Code was updated (see Example 58-5 Data EEPROM Forced Word Erase Code)
- The Data EEPROM Bulk Erase Code was updated (see Example 58-6 Data EEPROM Bulk Erase Code)

Minor updates to text and formatting were incorporated in the document

Revision C (December 2018)

This revision includes the following updates:

- **58.4.1 “Data EEPROM Error Interrupt (ERRIF)”** was updated.
- **58.4.2 “Data EEPROM Read Complete (EERDIF) and Write Complete (EEWRIF) ”** was updated.

Minor updates to text and formatting were incorporated throughout the doc.

Revision D (May 2019)

This revision includes the following updates:

- **58.4.1 “Data EEPROM Error Interrupt (ERRIF)”** condition description was re-worded for better clarity.

Revision E (September 2019)

This revision includes the following updates:

- Example 58-1 Data EEPROM Initialization Code was modified to reflect accurate initialization sequence.
- Nomenclature revisions were made to the following registers:
  - Renamed Register 58-5 from EEPCAL10 to DEVEE0
  - Renamed Register 58-6 from EEPCAL32 to DEVEE1
  - Renamed Register 58-7 from EEPCAL54 to DEVEE2
  - Renamed Register 58-8 from EEPCAL76 to DEVEE3

NOTES:

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