TB3260

How to Create Non-Cacheable Memory Region on Cortex-M7 (SAM S70/ E70/ V70/ V71) MCUs Using MPLAB Harmony v3

Introduction

The cache coherency issue is inevitable on applications running on microcontrollers (MCUs) that have cacheable memory regions, which use Direct Memory Access (DMA) for data transfer operations. This is due to the CPU performing a read/write from the cache while the DMA transfers data between the peripheral and physical memory.

One of the methods to address cache coherency is to create a coherent or non-cacheable memory region and place data variables in contention within it. When the data is made coherent, the CPU always accesses the data from the main memory (SRAM).

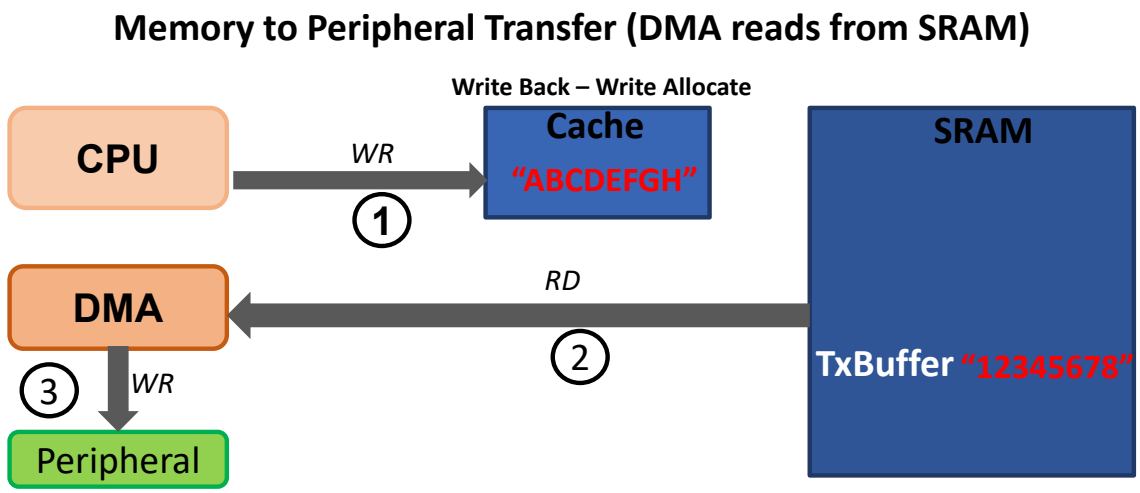
This document explains how to create a non-cacheable memory region and allocate data variables under contention in the non-cacheable region using MPLAB Harmony v3.

Note: The concepts discussed in this document are common for all Arm®Cortex®-M7 MCUs, and the SAM E70 MCU is used as an example to discuss the concepts.

1. Description

The following figure illustrates one form of cache coherency issue observed on the SAME70 MCU.

Figure 1-1. Cache Coherency (DMA Reads from SRAM)

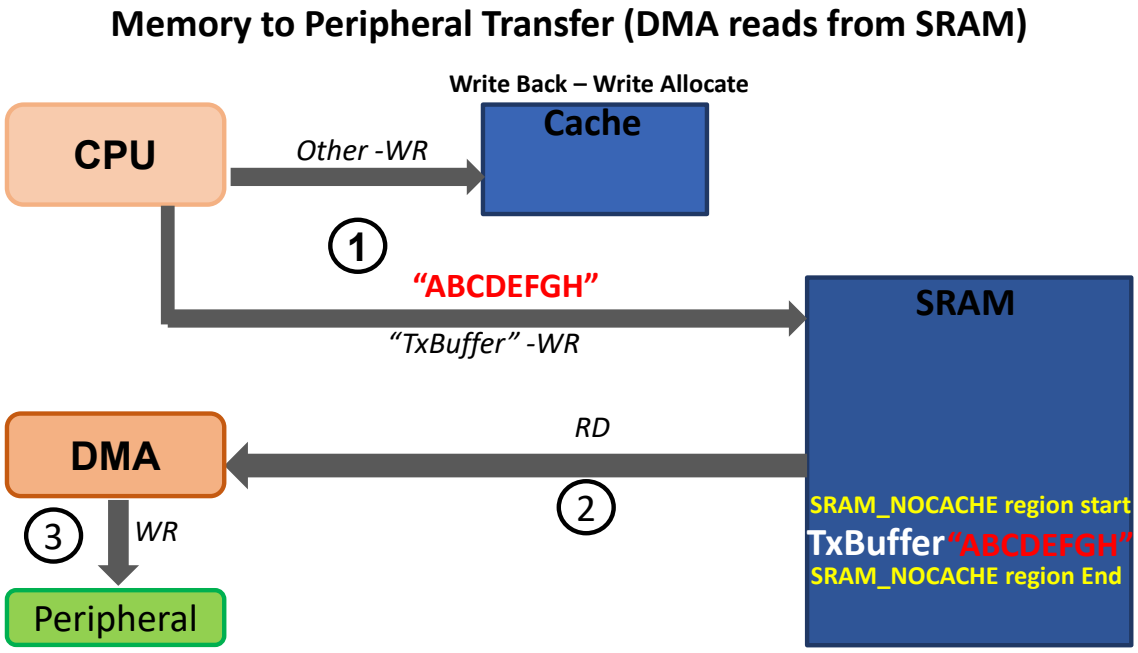


The application submits request to transfer the data buffer TxBuffer (value ABCDEFGH) to the peripheral. The CPU populates the DMA write buffer (TxBuffer) with the data to be written (value ABCDEFGH) to the peripheral. However, due to the set cache policy *Write Back and Write Allocate,* the DMA write buffer (TxBuffer) is available in the data cache. Therefore, it is not updated to the main memory. The DMA write buffer (TxBuffer) in the main memory still contains the old value (12345678).

When the DMA is triggered to initiate the memory to peripheral transfer, the DMA reads the buffer (TxBuffer) from the main memory (12345678). As a result, the DMA ends up transferring stale data to the peripheral.

One of the ways to address the above cache coherency issue in the SAME70 MCU is create a non-cacheable region and allocate the data in contention to the non-cacheable region. The following figure illustrates how the cache coherency issue observed in the figure above is addressed by creating a non-cacheable region.

Figure 1-2. Cache Coherency Solution (Non-Cacheable Region)



The user configures the Memory Protection Unit (MPU) in the SAME70 to not cache a part of the SRAM memory and allocates the DMA write buffer (TxBuffer) in the non-cacheable memory region.

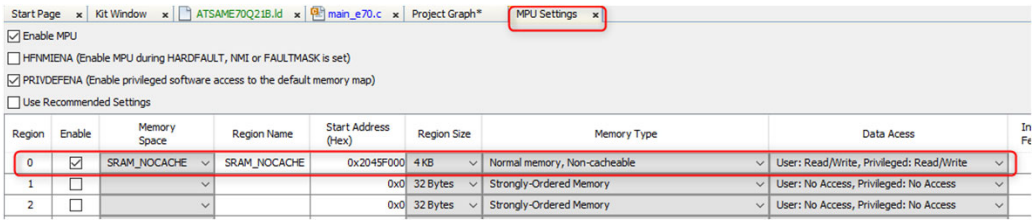
An access by the CPU to populate the DMA write buffer (TxBuffer) goes to the main memory as it is configured to be unavailable in the data cache. However, due to the set cache policy Write Back and Write Allocate, the other data accessed by the application continues to be cached.

When the DMA is triggered to initiate the memory-to-peripheral transfer, the DMA reads the buffer (TxBuffer) from the main memory (ABCDEFGH). As a result, the DMA transfers the correct data to the peripheral.

The following steps are used to create a non-cacheable region at address 0x2045F000 with a size of 4 Kb. The DMA write buffer(TxBuffer) will be allocated in this region.

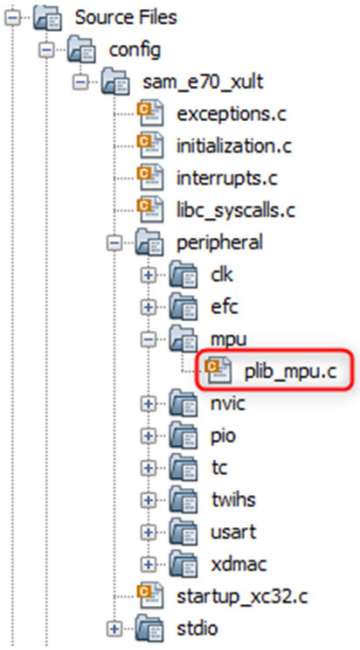
1. To configure a non-cacheable region using MPU Configurator, follow these steps:
   1.1. Open MPLAB Harmony v3 project and launch the MPLAB Harmony 3 Configurator.
   1.2. Launch the MPU Configurator window by going to the drop-down menu *MHC* > *Tools* > *MPU Configuration*.
   1.3. Configure the non-cacheable region as SRAM_NOCACHE as shown in the following figure:

Figure 1-3. MPU settings - SRAM_NOCACHE Region



   1.4. Regenerate the MPLAB Harmony v3 project.
   1.5. If it is not present, the peripheral library (PLIB) for MPU is added to the project:

Figure 1-4. MPU PLIB



1.6. In the PLIB file, `plib_mpu.c`, the `MPU_Initialize` function has the following code added to configure the non-cacheable region:

```
    /*** Configure MPU Regions  ***/

    /* Region 0 Name: SRAM_NOCACHE, Base Address: 0x2045f000, Size: 4KB  */
    MPU->RBAR = MPU_REGION(0, 0x2045f000);
    MPU->RASR = MPU_REGION_SIZE(11) | MPU_RASR_AP(MPU_RASR_AP_READWRITE_Val) |
MPU_ATTR_NORMAL \
                | MPU_ATTR_ENABLE | MPU_ATTR_EXECUTE_NEVER ;
```

1.7. The function `MPU_Initialize` is called from the source file, `startup_xc32.c`.

2. To create a non-cacheable SRAM section in the linker script file follow these steps.
To create a non-cacheable SRAM section, the default linker script file used by the MPLAB Harmony v3 project must be customized.

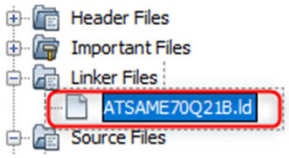
2.1. Depending on the MCU part selected in your MPLAB Harmony v3 project, the MPLAB X IDE uses the default linker script file available in the XC32 toolchain (compiler) path; usually available at `C:\Program Files (x86)\Microchip\xc32\v2.30\pic32c\lib\proc`.

2.2. For the SAME70 MCU, the MPLAB Harmony v3 project with the ATSAME70Q21B as the MCU, uses the linker script file `C:\Program Files (x86)\Microchip\xc32\v2.30\pic32c\lib\proc\ATSAME70Q21B\ATSAME70Q21B.ld`.

2.3. Copy the default linker script file `ATSAME70Q21B.ld` and paste it in the src folder of the MPLAB Harmony v3 project.

2.4. Add the linker script file in the src folder to the MPLAB Harmony v3 project in MPLABX IDE under the Linker Files section.

Figure 1-5. Adding Linker Script



2.5. Add the following sections in the linker script file:

- Under Memory-Region Macro Definitions add the highlighted code:

```
#ifndef RAM_ORIGIN
#  define RAM_ORIGIN 0x20400000
#endif
#ifndef RAM_LENGTH
#  define RAM_LENGTH 0x60000
#elif (RAM_LENGTH > 0x60000)
#  error RAM_LENGTH is greater than the max size of 0x60000
#endif

#ifndef SRAM_NOCACHE
#  define SRAM_NOCACHE 0x2045F000
#endif
#ifndef SRAM_NOCACHE_LENGTH
#  define SRAM_NOCACHE_LENGTH 0x1000
#elif (SRAM_NOCACHE_LENGTH > 0x60000)
#  error SRAM_NOCACHE_LENGTH is greater than the max size of 0x60000
#endif
```

- Under Memory-Region Definitions add the highlighted code:

```
MEMORY
{
  rom (LRX) : ORIGIN = ROM_ORIGIN, LENGTH = ROM_LENGTH
  ram (WX!R) : ORIGIN = RAM_ORIGIN, LENGTH = RAM_LENGTH-__XC32_ITCM_LENGTH-
__XC32_DTCM_LENGTH
  ram_nocache (RWX) : ORIGIN = SRAM_NOCACHE, LENGTH = SRAM_NOCACHE_LENGTH
  itcm (WX) : ORIGIN = ITCM_ORIGIN, LENGTH = __XC32_ITCM_LENGTH
  dtcm (WX!R) : ORIGIN = DTCM_ORIGIN, LENGTH = __XC32_DTCM_LENGTH
  config_D0000000 : ORIGIN = 0xD0000000, LENGTH = 0x4
  config_D0000004 : ORIGIN = 0xD0000004, LENGTH = 0x4
  config_D0000008 : ORIGIN = 0xD0000008, LENGTH = 0x4
  config_D000000C : ORIGIN = 0xD000000C, LENGTH = 0x4
  config_D0000010 : ORIGIN = 0xD0000010, LENGTH = 0x4

}
```

- Under Section Definitions add the highlighted code:

```
    .vectors :
    {
        . = ALIGN(4);
        _sfixed = .;
        KEEP(*(.vectors .vectors.* .vectors_default .vectors_default.*))
        KEEP(*(.isr_vector))
        KEEP(*(.reset*))
        KEEP(*(.after_vectors))
    } > VECTOR_REGION

    .ram_nocache (NOLOAD):
    {
        . = ALIGN(4);
        _s_ram_nocache = .;
        *(.ram_nocache)
        . = ALIGN(4);
        _e_ram_nocache = .;
    } > ram_nocache
```

- Save the custom linker script file, `ATSAME70Q21B.ld`.

3. Assigning the DMA write buffer TxBuffer in the non-cacheable region:

In the application code, while declaring the DMA write buffer (TxBuffer), use the attribute as shown below to allocate it in the non-cacheable region:

```
uint8_t __attribute__ ((section (".ram_nocache")))TxBuffer[100] = {0};
```

The application uses the DMA write buffer (TxBuffer) in the DMA transfer APIs:

```
XDMAC_ChannelTransfer(XDMAC_CHANNEL_0, TxBuffer,
                  (const void *)&(USART1_REGS->US_THR), strlen((const char*)TxBuffer));
```

The non-cacheable region approach to address the cache coherence issues:

- Keeps the application simple
- No explicit cache management is required
- No requirement for buffer alignment and buffer size

Though the non-cacheable region approach provides the above benefits, it comes with a cost of some performance degradation, as the coherent or non-cached data can only be accessed from the main memory.

2. References

1. Managing Cache Coherency on Cortex-M7 Based MCUs: http://ww1.microchip.com/downloads/en/DeviceDoc/Managing-Cache-Coherency-on-Cortex-M7-Based-MCUs-DS90003195A.pdf.
2. ARM Cortex-M7 Processor Technical Reference Manual: http://infocenter.arm.com/help/index.jsp?topic=/com.arm.doc.ddi0489d/Chdcghid.html.
3. Usage of XDMAC on SAM S/SAM E/SAM V: https://www.microchip.com/wwwappnotes/appnotes.aspx?appnote=en592128.

The Microchip Website

Microchip provides online support via our website at http://www.microchip.com/. This website is used to make files and information easily available to customers. Some of the content available includes:

- **Product Support** – Data sheets and errata, application notes and sample programs, design resources, user's guides and hardware support documents, latest software releases and archived software
- **General Technical Support** – Frequently Asked Questions (FAQs), technical support requests, online discussion groups, Microchip design partner program member listing
- **Business of Microchip** – Product selector and ordering guides, latest Microchip press releases, listing of seminars and events, listings of Microchip sales offices, distributors and factory representatives

Product Change Notification Service

Microchip's product change notification service helps keep customers current on Microchip products. Subscribers will receive email notification whenever there are changes, updates, revisions or errata related to a specified product family or development tool of interest.

To register, go to http://www.microchip.com/pcn and follow the registration instructions.

Customer Support

Users of Microchip products can receive assistance through several channels:

- Distributor or Representative
- Local Sales Office
- Embedded Solutions Engineer (ESE)
- Technical Support

Customers should contact their distributor, representative or ESE for support. Local sales offices are also available to help customers. A listing of sales offices and locations is included in this document.

Technical support is available through the website at: http://www.microchip.com/support

Microchip Devices Code Protection Feature

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

Legal Notice

Information contained in this publication regarding device applications and the like is provided only for your convenience and may be superseded by updates. It is your responsibility to ensure that your application meets with

your specifications. MICROCHIP MAKES NO REPRESENTATIONS OR WARRANTIES OF ANY KIND WHETHER EXPRESS OR IMPLIED, WRITTEN OR ORAL, STATUTORY OR OTHERWISE, RELATED TO THE INFORMATION, INCLUDING BUT NOT LIMITED TO ITS CONDITION, QUALITY, PERFORMANCE, MERCHANTABILITY OR FITNESS FOR PURPOSE. Microchip disclaims all liability arising from this information and its use. Use of Microchip devices in life support and/or safety applications is entirely at the buyer's risk, and the buyer agrees to defend, indemnify and hold harmless Microchip from any and all damages, claims, suits, or expenses resulting from such use. No licenses are conveyed, implicitly or otherwise, under any Microchip intellectual property rights unless otherwise stated.

Trademarks

The Microchip name and logo, the Microchip logo, Adaptec, AnyRate, AVR, AVR logo, AVR Freaks, BesTime, BitCloud, chipKIT, chipKIT logo, CryptoMemory, CryptoRF, dsPIC, FlashFlex, flexPWR, HELDO, IGLOO, JukeBlox, KeeLoq, Kleer, LANCheck, LinkMD, maXStylus, maXTouch, MediaLB, megaAVR, Microsemi, Microsemi logo, MOST, MOST logo, MPLAB, OptoLyzer, PackeTime, PIC, picoPower, PICSTART, PIC32 logo, PolarFire, Prochip Designer, QTouch, SAM-BA, SenGenuity, SpyNIC, SST, SST Logo, SuperFlash, Symmetricom, SyncServer, Tachyon, TempTrackr, TimeSource, tinyAVR, UNI/O, Vectron, and XMEGA are registered trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

APT, ClockWorks, The Embedded Control Solutions Company, EtherSynch, FlashTec, Hyper Speed Control, HyperLight Load, IntelliMOS, Libero, motorBench, mTouch, Powermite 3, Precision Edge, ProASIC, ProASIC Plus, ProASIC Plus logo, Quiet-Wire, SmartFusion, SyncWorld, Temux, TimeCesium, TimeHub, TimePictra, TimeProvider, Vite, WinPath, and ZL are registered trademarks of Microchip Technology Incorporated in the U.S.A.

Adjacent Key Suppression, AKS, Analog-for-the-Digital Age, Any Capacitor, AnyIn, AnyOut, BlueSky, BodyCom, CodeGuard, CryptoAuthentication, CryptoAutomotive, CryptoCompanion, CryptoController, dsPICDEM, dsPICDEM.net, Dynamic Average Matching, DAM, ECAN, EtherGREEN, In-Circuit Serial Programming, ICSP, INICnet, Inter-Chip Connectivity, JitterBlocker, KleerNet, KleerNet logo, memBrain, Mindi, MiWi, MPASM, MPF, MPLAB Certified logo, MPLIB, MPLINK, MultiTRAK, NetDetach, Omniscient Code Generation, PICDEM, PICDEM.net, PICkit, PICtail, PowerSmart, PureSilicon, QMatrix, REAL ICE, Ripple Blocker, SAM-ICE, Serial Quad I/O, SMART-I.S., SQI, SuperSwitcher, SuperSwitcher II, Total Endurance, TSHARC, USBCheck, VariSense, ViewSpan, WiperLock, Wireless DNA, and ZENA are trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

SQTP is a service mark of Microchip Technology Incorporated in the U.S.A.

The Adaptec logo, Frequency on Demand, Silicon Storage Technology, and Symmcom are registered trademarks of Microchip Technology Inc. in other countries.

GestIC is a registered trademark of Microchip Technology Germany II GmbH & Co. KG, a subsidiary of Microchip Technology Inc., in other countries.

All other trademarks mentioned herein are property of their respective companies.

ISBN: 978-1-5224-6037-4

Quality Management System

For information regarding Microchip's Quality Management Systems, please visit http://www.microchip.com/quality.

Worldwide Sales and Service

AMERICAS	ASIA/PACIFIC	ASIA/PACIFIC	EUROPE
Corporate Office 2355 West Chandler Blvd. Chandler, AZ 85224-6199 Tel: 480-792-7200 Fax: 480-792-7277 Technical Support: http://www.microchip.com/support Web Address: http://www.microchip.com **Atlanta** Duluth, GA Tel: 678-957-9614 Fax: 678-957-1455 **Austin, TX** Tel: 512-257-3370 **Boston** Westborough, MA Tel: 774-760-0087 Fax: 774-760-0088 **Chicago** Itasca, IL Tel: 630-285-0071 Fax: 630-285-0075 **Dallas** Addison, TX Tel: 972-818-7423 Fax: 972-818-2924 **Detroit** Novi, MI Tel: 248-848-4000 **Houston, TX** Tel: 281-894-5983 **Indianapolis** Noblesville, IN Tel: 317-773-8323 Fax: 317-773-5453 Tel: 317-536-2380 **Los Angeles** Mission Viejo, CA Tel: 949-462-9523 Fax: 949-462-9608 Tel: 951-273-7800 **Raleigh, NC** Tel: 919-844-7510 **New York, NY** Tel: 631-435-6000 **San Jose, CA** Tel: 408-735-9110 Tel: 408-436-4270 **Canada - Toronto** Tel: 905-695-1980 Fax: 905-695-2078	**Australia - Sydney** Tel: 61-2-9868-6733 **China - Beijing** Tel: 86-10-8569-7000 **China - Chengdu** Tel: 86-28-8665-5511 **China - Chongqing** Tel: 86-23-8980-9588 **China - Dongguan** Tel: 86-769-8702-9880 **China - Guangzhou** Tel: 86-20-8755-8029 **China - Hangzhou** Tel: 86-571-8792-8115 **China - Hong Kong SAR** Tel: 852-2943-5100 **China - Nanjing** Tel: 86-25-8473-2460 **China - Qingdao** Tel: 86-532-8502-7355 **China - Shanghai** Tel: 86-21-3326-8000 **China - Shenyang** Tel: 86-24-2334-2829 **China - Shenzhen** Tel: 86-755-8864-2200 **China - Suzhou** Tel: 86-186-6233-1526 **China - Wuhan** Tel: 86-27-5980-5300 **China - Xian** Tel: 86-29-8833-7252 **China - Xiamen** Tel: 86-592-2388138 **China - Zhuhai** Tel: 86-756-3210040	**India - Bangalore** Tel: 91-80-3090-4444 **India - New Delhi** Tel: 91-11-4160-8631 **India - Pune** Tel: 91-20-4121-0141 **Japan - Osaka** Tel: 81-6-6152-7160 **Japan - Tokyo** Tel: 81-3-6880- 3770 **Korea - Daegu** Tel: 82-53-744-4301 **Korea - Seoul** Tel: 82-2-554-7200 **Malaysia - Kuala Lumpur** Tel: 60-3-7651-7906 **Malaysia - Penang** Tel: 60-4-227-8870 **Philippines - Manila** Tel: 63-2-634-9065 **Singapore** Tel: 65-6334-8870 **Taiwan - Hsin Chu** Tel: 886-3-577-8366 **Taiwan - Kaohsiung** Tel: 886-7-213-7830 **Taiwan - Taipei** Tel: 886-2-2508-8600 **Thailand - Bangkok** Tel: 66-2-694-1351 **Vietnam - Ho Chi Minh** Tel: 84-28-5448-2100	**Austria - Wels** Tel: 43-7242-2244-39 Fax: 43-7242-2244-393 **Denmark - Copenhagen** Tel: 45-4485-5910 Fax: 45-4485-2829 **Finland - Espoo** Tel: 358-9-4520-820 **France - Paris** Tel: 33-1-69-53-63-20 Fax: 33-1-69-30-90-79 **Germany - Garching** Tel: 49-8931-9700 **Germany - Haan** Tel: 49-2129-3766400 **Germany - Heilbronn** Tel: 49-7131-72400 **Germany - Karlsruhe** Tel: 49-721-625370 **Germany - Munich** Tel: 49-89-627-144-0 Fax: 49-89-627-144-44 **Germany - Rosenheim** Tel: 49-8031-354-560 **Israel - Ra'anana** Tel: 972-9-744-7705 **Italy - Milan** Tel: 39-0331-742611 Fax: 39-0331-466781 **Italy - Padova** Tel: 39-049-7625286 **Netherlands - Drunen** Tel: 31-416-690399 Fax: 31-416-690340 **Norway - Trondheim** Tel: 47-72884388 **Poland - Warsaw** Tel: 48-22-3325737 **Romania - Bucharest** Tel: 40-21-407-87-50 **Spain - Madrid** Tel: 34-91-708-08-90 Fax: 34-91-708-08-91 **Sweden - Gothenberg** Tel: 46-31-704-60-40 **Sweden - Stockholm** Tel: 46-8-5090-4654 **UK - Wokingham** Tel: 44-118-921-5800 Fax: 44-118-921-5820