PIC32MZ Graphics (DAK/DAL/DAR/DAS) Family

PIC32MZ Graphics DAK/DAL/DAR/DAS Family Silicon Errata and Data Sheet Clarifications

PIC32MZ Graphics DAK/DAL/DAR/DAS Family

The PIC32MZ Graphics DAK/DAL/DAR/DAS family of devices that you have received conform functionally to the current Device Data Sheet (DS60001565**C**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in the table below.

The errata described in this document will be addressed in future revisions of the PIC32MZ Graphics DAK/DAL/DAR/DAS family silicon.

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current.

Data Sheet clarifications and corrections (if applicable) can be located in Data Sheet Clarifications section, that is, following the discussion of silicon issues.

Table 1. SILICON DEVREV VALUES

Part Number	Device ID (DEVID[27:0])(1)	Revision ID for Silicon Revision (DEVID[31:28])(1)
		B1
PIC32MZ1025DAK169	0x8A0C053	0x3
PIC32MZ1025DAL169	0x8A0D053	
PIC32MZ1064DAK169	0x8A0F053	
PIC32MZ1064DAL169	0x8A10053	
PIC32MZ2025DAK169	0x8A15053	
PIC32MZ2025DAL169	0x8A16053	
PIC32MZ2064DAK169	0x8A18053	
PIC32MZ2064DAL169	0x8A19053	
PIC32MZ1025DAR169	0x8A42053	
PIC32MZ1025DAS169	0x8A43053	
PIC32MZ1064DAR169	0x8A45053	
PIC32MZ1064DAS169	0x8A46053	
PIC32MZ2025DAR169	0x8A4B053	
PIC32MZ2025DAS169	0x8A4C053	
PIC32MZ2064DAR169	0x8A4E053	
PIC32MZ2064DAS169	0x8A4F053	

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.....continued		
Part Number	**Device ID (DEVID[27:0])(1)**	**Revision ID for Silicon Revision (DEVID[31:28])(1)**
		B1
PIC32MZ1025DAK176	0x8A78053	0x3
PIC32MZ1025DAL176	0x8A79053	
PIC32MZ1064DAK176	0x8A7B053	
PIC32MZ1064DAL176	0x8A7C053	
PIC32MZ2025DAK176	0x8A81053	
PIC32MZ2025DAL176	0x8A82053	
PIC32MZ2064DAK176	0x8A84053	
PIC32MZ2064DAL176	0x8A85053	
PIC32MZ1025DAR176	0x8AAE053	
PIC32MZ1025DAS176	0x8AAF053	
PIC32MZ1064DAR176	0x8AB1053	
PIC32MZ1064DAS176	0x8AB2053	
PIC32MZ2025DAR176	0x8AB7053	
PIC32MZ2025DAS176	0x8AB8053	
PIC32MZ2064DAR176	0x8ABA053	
PIC32MZ2064DAS176	0x8ABB053	

Note:

1. Refer to the “Memory Organization” and “Special Features” chapters in the current device Data Sheet (DS60001565**C**) for detailed information on Device and Revision IDs for your specific device.

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1. Silicon Issue Summary

Table 1-1. Silicon Issue Summary

Module	Feature	Item	Issue Summary	Affected Revisions(1)
				B1
ADC	DNL	2.1.1	DNL Specification is not met and upto 10 missing codes are possible.	X
ADC	Turbo Mode	2.1.2	Turbo Mode is Not Functional.	X
ADC	External VREF	2.1.3	Excessive current flows through VREF- pin when external voltage reference is used, and voltage on VREF- pin is greater than AVSS.	X
Crypto	Partial Packet	2.2.1	The Crypto Engine does not support partial packet processing.	X
Crypto	Zero-length Packet	2.2.2	The Crypto Engine does not support a Hash operation on an empty string.	X
CTMU	Triggers	2.3.1	Edge Sequencing mode (EDGSEQEN bit (CTMUCON<10>)) and Edge modes are not functional.	X
CTMU	TGEN	2.3.2	When the TGEN bit is set, manual current sourcing from CTMU is not possible.	X
Deep Sleep	Power Down	2.4.1	Deep Sleep mode is not functional.	X
DMA	PMD Bits	2.5.1	Setting the PMD bit for DMA (PMD7<4>) does not disable clocks to the DMA peripheral.	X
EBI	Chip Select	2.6.1	For Asynchronous NOR Flash, EBI internal clock specification, T_{EBICLK} (EB10), is not met.	X
EBI	VDDIO Range	2.6.2	EBI is not functional when VDDIO < 2.5V.	X
EBI	EBIRDYx pin when EBI is Enabled	2.6.3	When the EBI is enabled, the EBIRDYx pins function as EBIRDYx pins only.	X
Input Capture	Debug	2.7.1	Debug breakpoints are not supported when using Input Capture with DMA.	X
I^2C	Speed	2.8.1	I^2C module does not meet low period of the SCL clock (t_{LOW}) parameter from I^2C specification for clock frequency >= 400 KHz.	X
I^2C	Start/Restart	2.8.2	When the I^2C module is in Client mode, Start and Restart interrupts are not functional.	X
I^2C	I^2C Client	2.8.3	The 7-bit address that matches the 10-bit upper address value (111_10xx) is not accepted regardless of the STRICT bit setting.	X
PMP	Status Flags	2.9.1	The PMP input buffer full flag, IB0F, and the output buffer underflow, OBUF, are getting set as soon as the PMP module is enabled in Client mode (PMPTTL bit (PMCON<10>) is equal to '1').	X
SDHC	MMC	2.10.1	Data from the MMC card can not be read correctly when the block size is set smaller than 512 bytes.	X
SDHC	Card Detect	2.10.2	The SDHC module may not function if the SDCD pin is not used.	X
SDHC	Card Detect Status	2.10.3	Card detect status indication through the CDSLVL bit (SDHCSTAT1<18>) is inverted.	X
SDHC	Write Protect Status	2.10.4	Write protect status indication through the WPSLVL bit (SDHCSTAT1<19>) is inverted.	X
SDHC	Stop at Block Gap	2.10.5	The Stop at Block Gap feature of the SDHC module is not functional.	X
Sleep	IPD	2.11.1	3 mA increase in sleep current when PB5DIV is disabled.	X
Sleep	Wake-up	2.11.2	Multiple sleep attempts which occur before the CPU has fully awakened, may stall the CPU until the next reset event.	X
SOSC	Ready Status	2.12.1	The validity of the SOSCRDY bit (CLKSTAT<4>) is not guaranteed.	X
SPI	Block Transmission	2.13.1	At the end of a transmission, the SRMT bit can indicate the completion of the transmission for one PBCLK even though the transmission has one block remaining.	X
SQI	Operational Frequency	2.14.1	SQI does not meet the maximum Serial Clock Frequency (F_{CLK}) specification from the Data Sheet when VDDIO < 2.5V.	X
SQI	Special Functions Registers	2.14.2	The CPU stalls if the SQI Special Function Registers are read before the REFCLKO2 clock is enabled after a Reset.	X
Temperature Sensor	IVTEMP Temperature Sensor	2.15.1	The temperature sensor IVTEMP (ADC channel 43) does not function.	X

.....continued

Module	Feature	Item	Issue Summary	Affected Revisions(1)
				B1
Timer1	Asynchronous Counter	2.16.1	Timer1 in Asynchronous External Counter mode does not reflect the first count from an external T1CK input.	X
Timer1	TMR1 Register	2.16.2	TMR1 register of Timer1 in Asynchronous mode remains at initial set value for five external clock pulses after wake-up from Sleep mode.	X
Timer1	Asynchronous Mode	2.16.3	Timer1 counts beyond the period value in Asynchronous mode when the period is 0x01.	X
Timer1	Gated Mode	2.16.4	Timer1 does not work properly in Gated mode with prescaler enabled.	X
Timer1	TMR1 Register Writes	2.16.5	Back-to-back writes to the TMR1 register are not allowed for four PBCLK cycles.	X
Timer1	Asynchronous Timer1	2.16.6	The Asynchronous Timer Write Disable bit, TWDIS(TxCON<12>), and the Asynchronous Timer Write in Progress bit, TWIP (TxCON<11>), are non-functional.	X
Timer2-9	Match	2.17.1	If timer match coincides with entry into sleep mode, timer event triggers and interrupt may not occur.	X
Timer2-9	Debug	2.17.2	On a debug breakpoint, TMRx register, x=2-9, may not be representative of the correct value.	X
Timer2-9	Match	2.17.3	If timer match coincides with entry into Idle mode, timer event triggers and interrupt may not occur.	X
UART	High-Speed Mode	2.18.1	The UART Stop bit duration is shorter than expected in High-Speed mode (UxMODE.BRGH = 1) for baud rates less than 7.5 Mbps.	X
UART	OERR bit	2.18.2	Clearing the receive buffer overrun error through the OERR bit (UxSTA<1>) clears the receive buffer.	X
USB	Host Resume	2.19.1	USB Host module does not send correct resume signal on the USB bus on subsequent suspend/ resume sequences.	X
USB	Remote Resume	2.19.2	USB Host module unexpectedly wakes up the CPU from sleep when remote resume is enabled	X
USB	Resume	2.19.3	USBRF bit (USBCRCON<25>) is not functional.	X
USB	LPM	2.19.4	Link Power Management (LPM) Feature is not functional.	X
USB	Host Disconnect Detection	2.19.5	USB Host module does not wakeup CPU from sleep when a USB device is disconnected.	X
USB	FIFO	2.19.6	Writing '1' to the FLUSH bit (USBIENCSRx<19>, where x = 1- 7) does not flush the TX FIFO and reset the TX FIFO pointer.	X
VBAT	VBAT	2.20.1	VBAT is not functional.	X
CFG	Unique ID	2.21.1	Unique ID (DEVSNx) is not programmed in the devices released	X

Note:

1. Only those issues indicated in the last column apply to the current silicon revision.

2. Silicon Errata Issues

This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current.

2.1 ADC

2.1.1 DNL

DNL Specification is not met and upto 10 missing codes are possible.

Workaround
None.

Affected Silicon Revisions

B1							
X							

2.1.2 Turbo Mode

Turbo mode (TRBEN bit (ADCCON1<31>) = 1) is not functional when two channels are linked for the purpose of increasing throughput.

Workaround
Users can still increase the effective throughput rate by interleaving ADC cores and trigger sources by connecting multiple dedicated high-speed ADCs to the same analog input, and staggering the respective ADCx core triggers appropriately.

Affected Silicon Revisions

B1							
X							

2.1.3 External VREF

Excessive current flows through the VREF- pin when external voltage reference is used, and voltage on the VREF- pin is greater than AVSS.

Workaround
Connect the VREF- pin to AVSS. Dynamic range can be changed after varying voltage on the VREF+ pin.

Affected Silicon Revisions

B1							
X							

2.2 Crypto

2.2.1 Partial Packet

The output digest of a partial message cannot be used as the initial vector for continuing the cryptographic operation on the remainder of the message. The full message must be processed in one operation.

Workaround
None.

Affected Silicon Revisions

B1							
X							

2.2.2 Zero-length Packet

The Crypto Engine does not support a hash operation on an empty string (i.e., string with zero length). The Crypto Engine times out and does not return a valid hash.

Workaround
Use the fixed known hash of the empty string.

Affected Silicon Revisions

B1							
X							

2.3 CTMU

2.3.1 Triggers

Edge Sequencing mode (EDGSEQEN bit (CTMUCON<10>)) and Edge mode are not functional.

Workaround
Use level modes.

Affected Silicon Revisions

B1							
X							

2.3.2 TGEN

When the TGEN bit is set, manual current sourcing (i.e., setting the EDG1STAT bit (CTMUCON<24>)) from CTMU is not possible.

Workaround
None.

Affected Silicon Revisions

B1							
X							

2.4 Deep Sleep

2.4.1 Power Down

Deep Sleep mode is not functional.

Workaround
None.

Affected Silicon Revisions

B1							
X							

2.5 DMA

2.5.1 PMD Bits

Setting the PMD bit for DMA (PMD7<4>) does not disable clocks to the DMA peripheral.

Workaround
Use the ON bit (DMACON<15>) to enable or disable DMA globally, or use the CHEN bit (DCHxCON<7>) to enable or disable individual channels.

Affected Silicon Revisions

B1							
X							

2.6 EBI

2.6.1 Chip Select

For Asynchronous NOR Flash, EBI internal clock specification, T_{EBICLK} (EB10) is not met.

Workaround
When asynchronous NOR is attached to EBI, the system frequency must be reduced to 180 MHz for it to function properly.

Affected Silicon Revisions

B1							
X							

2.6.2 VDDIO Range

EBI is not functional when VDDIO < 2.5V.

Workaround
None.

Affected Silicon Revisions

B1							
X							

2.6.3 EBIRDYx pin when EBI is Enabled

When EBI is enabled, the EBIRDYx pins function as EBIRDYx pins only, and all other pin functions (GPIO, ADC, I^2C and so on) are not functional.

Workaround

None.

Affected Silicon Revisions

B1							
X							

2.7 Input Capture

2.7.1 Debug

Debug breakpoints are not supported when using Input Capture with DMA.

Workaround

None.

Affected Silicon Revisions

B1							
X							

2.8 I^2C

2.8.1 Speed

I^2C host module does not meet low period of the SCL clock (t_{LOW}) parameter from I^2C specification for clock frequency >= 400 kHz.

Workaround

None.

Affected Silicon Revisions

B1							
X							

2.8.2 Start/Restart

When the I^2C module is in Client mode, Start and Restart Interrupts are not occurring or properly reflected in the IFSx flag bits.

Workaround

Use software polling to test the I^2C Start or Restart Status bit, S (I2CxSTAT<3).

Affected Silicon Revisions

B1							
X							

2.8.3 I²C Client

The 7-bit address that matches the 10-bit upper address value (111_10xx) is not accepted regardless of the STRICT bit setting.

Workaround

None.

Affected Silicon Revisions

B1							
X							

2.9 PMP

2.9.1 Status Flags

The PMP Input Buffer Status Full bit (IB0F (PMSTAT<8>) and the Output Buffer Underflow Status bit (OBUF (PMSTAT<6>) are set as soon as the PMP module is enabled in Client mode (i.e., the PMPTTL bit (PMCON<10>) is equal to '1').

Workaround

After PMP Client mode initialization and before enabling PMP interrupts, clear the Input Buffer Full Flag (IB0F bit (PMSTAT<8>)), the Output Buffer Underflow Flag (OBUF bit (PMSTAT<6>)), and the corresponding PMP IFSx interrupt flags.

Affected Silicon Revisions

B1							
X							

2.10 SDHC

2.10.1 MMC

Data from the MMC card can not be read correctly when the block size is set smaller than 512 bytes (i.e., the BSIZE<9:0> bits (SDHCBLKCON<9:0>) are smaller than 0x200).

Workaround

None.

Affected Silicon Revisions

B1							
X							

2.10.2 Card Detect

The SDHC module may not function if the SDCD pin is not used.

Workaround 1:
Ensure that the SDCD pin is used and driven to a low state externally.

Workaround 2:

Set CDSSEL (SDHCCON1<7>) to '1' and CDTLVL (SDHCCON1<6>) to '0'.

Affected Silicon Revisions

B1							
X							

2.10.3 Card Detect Status

Card-detect status indication through the CDSLVL bit (SDHCSTAT1<18>) is inverted.

Workaround 1:
Use ACMD42 to detect the card's presence.

Workaround 2:

If SDCD is used for card detect, add a software work around to invert the CDSLVL (SDHCSTAT1<18>) state.

Affected Silicon Revisions

B1							
X							

2.10.4 Write Protect Status

Write-protect status indication through the WPSLVL bit (SDHCSTAT1<19>) is inverted.

Workaround 1:
If SDWP is used for Write-protect, use the SDWPPOL bit (CFGCON2<28>) to invert the WPSLVL bit (SDHCSTAT1<19>) state.

Workaround 2:

If SDWP is used for Write-protect, add a software work around to invert the WPSLVL bit (SDHCSTAT1<19>) state.

Affected Silicon Revisions

B1							
X							

2.10.5 Stop at Block Gap

The Stop at Block Gap feature of the SDHC module is not functional.

Workaround
None.

Affected Silicon Revisions

B1							
X							

2.11 Sleep

2.11.1 IPD

When PBCLK5 is disabled (i.e., the ON bit (PB5DIV<15>) = 0), there is a 3 mA increase in sleep IPD current.

Workaround

Do not disable PBCLK5 before entering Sleep mode.

Affected Silicon Revisions

B1							
X							

2.11.2 Wake-up

Multiple sleep attempts (i.e., WAIT instruction with the SLPEN bit (OSCCON<4>) =1) which occur within 20 µs of awake event, before the CPU has fully awakened, can cause the CPU to stall until a Power-on Reset (POR) event.

Workaround

Be sure that at least 20 µs elapse before attempting to put the CPU to sleep (WAIT instruction with SLPEN bit (OSCCON<4>) =1) after it awakens from a previous sleep.

Affected Silicon Revisions

B1							
X							

2.12 SOSC

2.12.1 Ready Status

The validity of the SOSCRDY bit (CLKSTAT<4>) is not guaranteed.

Workaround

None.

Affected Silicon Revisions

B1							
X							

2.13 SPI

2.13.1 Block Transmission

Just before the last block of a transmission is shifted out to the SPI pins, the SRMT bit may incorrectly indicate that the transmission is done. However, this does not affect the Transmit Buffer Empty Interrupt (STXISEL<1:0> bits (SPIxCON<3:2>) = 0).

Workaround

Use the interrupt notification rather than polling the SRMT bit to determine when a transmission has completed.

Affected Silicon Revisions

B1							
X							

2.14 SQI

2.14.1 Operational Frequency

SQI peripheral does not meet maximum Serial Clock Frequency (F_{CLK}) specification from the data sheet when VDDIO < 2.5V.

Workaround

None.

Affected Silicon Revisions

B1							
X							

2.14.2 Special Functions Register

After a Reset, the first access to the SQI SFRs must be a write. A read access can stall the CPU, requiring a Reset to clear. The typical initialization code may include a write to the SQIEN bit. The SQI1CFGbits.SQIEN=0 instruction is a read, modify, and write sequence. After a Reset, this sequence will stall the CPU. Similarly, only reading the SQI SFRs will also stall the CPU if that read is the first access after a Reset.

Workaround

Users must enable REFCLKO2 before reading the registers from the SQI peripheral.
Do not use the “SQI1CFGbits.SQIEN=0” instruction to enable the SQI, instead use the “SQI1CFGCLR= ”_SQICFG_SQIEN_MASK“ instruction.

Affected Silicon Revisions

B1							
X							

2.15 Temperature Sensor

2.15.1 IVTEMP Temperature Sensor

The temperature sensor, IVTEMP (ADC channel 43), is not functional.

Workaround

Consider using CTMUT temperature sensor ADC channel (AN40).

Affected Silicon Revisions

B1							
X							

2.16 Timer1

2.16.1 Asynchronous Counter

In Asynchronous external counter mode, (i.e., TCS bit (T1CON<1> = 1), TSYNC bit (T1CON<2> = 0), and TECS<1:0> (T1CON<9:8> = '0b01)), Timer1 does not reflect the first count from an external T1CLK input.

Workaround
None.

Affected Silicon Revisions

B1							
X							

2.16.2 TMR Register

The Timer1 register (TMR1) in Asynchronous external counter mode, (i.e., TCS bit (T1CON<1> = 1), TSYNC bit (T1CON<2> = 0), and TECS<1:0> (T1CON<9:8> = '0b01)), remains at the initial set value for five external clock pulses after wake-up from Sleep mode.

Workaround
None.

Affected Silicon Revisions

B1							
X							

2.16.3 Asynchronous Mode

Timer1 counts beyond the period value in Asynchronous mode when the period is 0x01.

Workaround
Set the Timer1 period, PR1, to a value greater than 1.

Affected Silicon Revisions

B1							
X							

2.16.4 Gated Mode

Timer1 does not work properly in Gated mode (i.e., TGATE bit (T1CON<7> = 1), TCS bit (T1CON<1> = 0) with the prescaler enabled (TCKPS<1:0> bits (T1CON<5:4>) = ‘0b00)).

Workaround
None.

Affected Silicon Revisions

B1							
X							

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2.16.5 TMR1 Register Writes

Back-to-back CPU writes to the TMR1 register are not allowed for at least four PBCLK cycles.

Workaround

None.

Affected Silicon Revisions

B1							
X							

2.16.6 Asynchronous Timer1

The Asynchronous Timer Write Disable bits (TWDIS (TxCON<12>)) and the Asynchronous Timer Write In Progress bits (TWIP (TxCON<11>)) are not functional.

Workaround

None.

Affected Silicon Revisions

B1							
X							

2.17 Timer2-9

2.17.1 Match

If timer match coincides with entry into Sleep mode, timer event triggers and interrupt may not occur.

Workaround

None.

Affected Silicon Revisions

B1							
X							

2.17.2 Debug

On a debug breakpoint, TMRx register, x=2-9, may not be representative of the correct count value.

Workaround

None.

Affected Silicon Revisions

B1							
X							

2.17.3 Match

When timer operation is discontinued in IDLE mode (i.e., the SIDL bit (TxCON <13>) is set), and timer match coincides with entry into Idle mode, timer event triggers and interrupt may not occur.

Workaround
None.

Affected Silicon Revisions

B1							
X							

2.18 UART

2.18.1 High-Speed Mode

The UART TX Stop bit duration is shorter than the expected in High-Speed mode (i.e., the BRGH bit (UxMODE<3>) = 1) for baud rates less than 7.5 Mbps.

Workaround
For baud rates less than 7.5 Mbps, operate the UART in standard Speed mode, that is, the BRGH bit (UxMODE<3> = 0) and calculate UxBRG register value. For baud rates greater than 7.5 Mbps, operate the UART in High-Speed mode (i.e., BRGH bit (UxMODE<3>) = 1) and re-calculate the UxBRG register value.

Affected Silicon Revisions

B1							
X							

2.18.2 OERR Bit

Clearing the receive buffer overrun error through the OERR bit (UxSTA<1>) clears the receive buffer. This condition occurs when the RUNOVF bit (UxMODE<16>) is set, and an overflow condition occurs.

Workaround
When a receive buffer overrun error occurs, read the entire receive FIFO through the UxRXREG register before clearing the OERR bit (UxSTA<1>).

Affected Silicon Revisions

B1							
X							

2.19 USB

2.19.1 Host Resume

USB Host module does not send the correct resume signal on the USB bus on subsequent suspend or resume sequences.

Workaround
None.

Affected Silicon Revisions

B1							
X							

2.19.2 Remote Resume

USB Host module unexpectedly wakes up the CPU from sleep when remote resume is enabled. (i.e., when the USBWKUPEN bit (USBCRCON<0>) is equal to '1').

Workaround

None.

Affected Silicon Revisions

B1							
X							

2.19.3 Resume

The USBRF bit (USBCRCON<25>) is not functional.

Workaround

Do not poll the USBRF bit (USBCRCON.<25>), instead use Suspend or Resume interrupt.

Affected Silicon Revisions

B1							
X							

2.19.4 LPM

USB Link Power Management (LPM) Feature is not functional.

Workaround

None.

Affected Silicon Revisions

B1							
X							

2.19.5 Host Disconnect Detection

USB Host module does not wakeup CPU from sleep when a USB device is disconnected.

Workaround

None.

Affected Silicon Revisions

B1							
X							

2.19.6 FIFO

Writing ‘1’ to the FLUSH bit (USBIENCSRx <19>, where x = 1-7) does not flush the TX FIFO and reset the TX FIFO pointer. As a result, the TXPKTRDY bit (USBIENCSRx <16>, where x = 1-7) is not cleared and the USB interrupt is not generated.

Workaround

To clear the TX FIFO, repeat the following action twice in a row:

Simultaneously set the FLUSH bit (USBIENCSRx <19>, where x = 1-7) and clear the TXPKTRDY bit (USBIENCSRx <16>, where x = 1-7).

Affected Silicon Revisions

B1							
X							

2.20 V_{BAT}

2.20.1 V_{BAT}

The V_{BAT} pin is not functional. Connect the V_{BAT} pin to VDDIO.

Workaround

None.

Affected Silicon Revisions

B1							
X							

2.21 CFG

2.21.1 Unique ID

Unique ID (DEVSNx, x = 0,1,2,3) is not programmed in the devices released earlier than trace code dated below.

- 1941GUB for devices without internal DDR2
- 194318D for devices with internal DDR2

Workaround

None.

Affected Silicon Revisions

B1							
X							

3. Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS60001565**C**):

Note: The corrected information is shown in **bold** type. Where possible, the original bold text formatting has been removed for clarity.

3.1 MPLL Maximum Output Frequency

Table 44-25 MPLL CLOCK TIMING REQUIREMENTS has been updated, and the corrected information is shown in **bold** type:

TABLE 44-25: MPLL CLOCK TIMING REQUIREMENTS							
AC CHARACTERISTICS			Standard Operating Conditions: VDDIO = 2.2V to 3.6V, VDDCORE = 1.7V to 1.9V (unless otherwise stated) Operating temperature -40°C < TA < +85°C for Industrial				
Param. No.	Symbol	Characteristic(1)	Min.	Typ.	Max.	Units	Conditions
MP10	MFIN	MPLL Input Frequency	8	—	64	MHz	—
MP11	MFVCO	MPLL Vco Frequency Range	400	—	1600	MHz	—
MP12	MFMPLL	MPLL Output Frequency	8	—	**200**	MHz	—
MP13	MLOCK	MPLL Start-up Time (Lock Time)	—	—	1500 x 1/MFIN	µs	—
MP14	MPJ	MPLL Period Jitter	—	—	0.015	%	—
MP15	MCJ	MPLL Cycle Jitter	—	—	0.02	%	—
MP16	MLTJ	MPLL Long-term Jitter	—	—	0.5	%	—

Note:

1. These parameters are characterized, but not tested in manufacturing.

4. Revision History

Revision E Document - 10/2022
The following Silicon Errata were updated in this revision:

- EBI - EBIRDYx pin when EBI is Enabled 2.6.3

Revision D Document - 05/2021
The I^2C, SPI and I^2S standards use the terminology "Master" and "Slave". The equivalent Microchip terminology used in this document is "Host" and "Client" respectively.

The following Data Sheet Clarifications were added:

- MPLL Maximum Output Frequency

The following Silicon Errata were added in this revision:

- USB - FIFO 2.19.6

Revision C Document - 09/2020
The following Silicon Errata were added in this revision:

- ADC - External VREF 2.1.3
- CFG - Unique ID 2.21.1

Revision B Document - 04/2019
Changed data sheet reference number from DS60001561A to DS60001565A.

Revision A Document - 03/2019
This is the initial released version of this document.

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