The PIC32MX1XX/2XX 28/44-pin XLP family devices that you have received conform functionally to the current Device Data Sheet (DS60001404E), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the PIC32MX1XX/2XX 28/44-pin XLP family silicon.

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision (A3).

Note: If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

### TABLE 1: SILICON DEVREV VALUES

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Device ID&lt;sup&gt;(1)&lt;/sup&gt;</th>
<th>Revision ID for Silicon Revision&lt;sup&gt;(1)&lt;/sup&gt;</th>
</tr>
</thead>
<tbody>
<tr>
<td>PIC32MX154F128B</td>
<td>0x07800053</td>
<td></td>
</tr>
<tr>
<td>PIC32MX174F256B</td>
<td>0x07801053</td>
<td></td>
</tr>
<tr>
<td>PIC32MX254F128B</td>
<td>0x07808053</td>
<td></td>
</tr>
<tr>
<td>PIC32MX274F256B</td>
<td>0x07803053</td>
<td></td>
</tr>
<tr>
<td>PIC32MX154F128D</td>
<td>0x07804053</td>
<td></td>
</tr>
<tr>
<td>PIC32MX174F256D</td>
<td>0x07805053</td>
<td></td>
</tr>
<tr>
<td>PIC32MX254F128D</td>
<td>0x07806053</td>
<td></td>
</tr>
<tr>
<td>PIC32MX274F256D</td>
<td>0x07807053</td>
<td></td>
</tr>
</tbody>
</table>

Note 1: Refer to the “Memory Organization” and “Special Features” chapters in the current Device Data Sheet (DS60001404E) for a detailed information on Device and Revision IDs for your specific device.
# TABLE 2: SILICON ISSUE SUMMARY

<table>
<thead>
<tr>
<th>Module</th>
<th>Feature</th>
<th>Item</th>
<th>Issue Summary</th>
<th>Affected Revisions(1)</th>
<th>A1</th>
<th>A3</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADC</td>
<td>IVREF</td>
<td>1</td>
<td>Reading internal IVREF from the ADC module is not supported.</td>
<td>X</td>
<td></td>
<td></td>
</tr>
<tr>
<td>CLKO</td>
<td>Clock Output</td>
<td>2</td>
<td>A clock signal is present on the CLKO pin, regardless of the clock source and</td>
<td>X X</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>setting of the CLKO Enable Configuration bit, during a Power-on Reset (POR)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Configuration Words</td>
<td>Mismatch</td>
<td>3</td>
<td>Configuration word mismatch logic is non-functional.</td>
<td>X X</td>
<td></td>
<td></td>
</tr>
<tr>
<td>CTMU</td>
<td>Edge-sensitive Trigger</td>
<td>4</td>
<td>Edge-sensitive trigger is not functioning for generating an Asynchronous pulse.</td>
<td>X X</td>
<td></td>
<td></td>
</tr>
<tr>
<td>CTMU</td>
<td>CTED Input</td>
<td>5</td>
<td>The EDGEN bit generates a glitch on the CTED input causing a false trigger.</td>
<td>X X</td>
<td></td>
<td></td>
</tr>
<tr>
<td>CTMU</td>
<td>Temperature Sensor</td>
<td>6</td>
<td>Temperature sensor measurement is not supported for CTMUCON&lt;1:0&gt; = range 2 or 3.</td>
<td>X X</td>
<td></td>
<td></td>
</tr>
<tr>
<td>CTMU</td>
<td>Temperature Sensor</td>
<td>7</td>
<td>Internal temperature sensor accuracy does not meet the data sheet specification.</td>
<td>X X</td>
<td></td>
<td></td>
</tr>
<tr>
<td>CTMU</td>
<td>Idle</td>
<td>8</td>
<td>CTMU current source isn't enabled in Idle mode (CTMUSIDL bit = 1), which</td>
<td>X X</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>prevents ADC, if enabled in Idle mode, from being able to measure the CTMU</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>temperature sensor.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CTMU</td>
<td>Current Sourcing</td>
<td>9</td>
<td>The CTMU module does not meet the current sourcing range data sheet</td>
<td>X X</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>specifications.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CTMU</td>
<td>Time Generation</td>
<td>10</td>
<td>When Time Generation mode is enabled by setting the TGEN bit (CTMUCON&lt;12&gt;),</td>
<td>X X</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>the manual current sourcing set by the EDG1STAT bit (CTMUCON &lt;24&gt;) from the</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>CTMU is non-functional.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Deep Sleep</td>
<td></td>
<td>11</td>
<td>The user application must not attempt to enter Deep Sleep mode for a period</td>
<td>X</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>of 50 µs after exiting Reset on start-up or the device will never recover and</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>is no longer able to be erased and/or reprogrammed.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Deep Sleep</td>
<td>DSGPR1 Register</td>
<td>12</td>
<td>On transition from Deep Sleep mode to VBAT mode, semaphore DSGPR1 register</td>
<td>X X</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>does not retain data.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Deep Sleep</td>
<td>Configuration Word</td>
<td>13</td>
<td>If a rare Configuration Word bit mismatch occurs while in Deep Sleep mode,</td>
<td>X</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>the device will be non-functional until a POR.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Deep Sleep</td>
<td>DSBOR</td>
<td>14</td>
<td>Inconsistent DSBOR status bit (DSCON&lt;1&gt;) values occur after a Deep Sleep BOR</td>
<td>X X</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>event.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Deep Sleep</td>
<td>Current Specification</td>
<td>15</td>
<td>The Deep Sleep Current specification is not met at less than 0ºC operation.</td>
<td>X X</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Deep Sleep</td>
<td>DSWAKE</td>
<td>16</td>
<td>Upon wake-up from Deep Sleep mode, the DSWAKE register does not always</td>
<td>X X</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>indicate the correct wake-up event source.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Deep Sleep</td>
<td>DPSLP Status Bit</td>
<td>17</td>
<td>The DPSLP Deep Sleep Mode status bit, DPSLP (RSCON&lt;10&gt;), is incorrectly set</td>
<td>X</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>even though Deep Sleep mode was not entered on a drop from VDD nominal to a</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>VPOR reset trip.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>FSCM</td>
<td>Interrupts</td>
<td>18</td>
<td>The Fail-Safe Clock Monitor should be a NMI interrupt instead of a user-</td>
<td>X</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>selectable IEC0&lt;29&gt; interrupt.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>I²C</td>
<td>Idle</td>
<td>19</td>
<td>The I²C module resets after Idle mode when the SIDL bit (I2CxCON&lt;13&gt;) is set.</td>
<td>X X</td>
<td></td>
<td></td>
</tr>
<tr>
<td>I²C</td>
<td>Start/Restart</td>
<td>20</td>
<td>When the I²C module is in Slave mode, Start and Restart interrupt are not</td>
<td>X X</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>functional on all devices.</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Note 1:** Only those issues indicated in the last column apply to the current silicon revision.
### Table 2: Silicon Issue Summary (Continued)

<table>
<thead>
<tr>
<th>Module</th>
<th>Feature</th>
<th>Item</th>
<th>Issue Summary</th>
<th>Affected Revisions(1)</th>
</tr>
</thead>
<tbody>
<tr>
<td>I(^2)C</td>
<td>Start/Stop</td>
<td>21.</td>
<td>The I(^2)C Start bit, S (I2CSTAT&lt;3&gt;), is not cleared and the Stop bit, P (I2CSTAT&lt;4&gt;), is not set when an external I(^2)C master creates a Stop condition immediately after a Start condition.</td>
<td>X X</td>
</tr>
<tr>
<td>TDO</td>
<td>Programming</td>
<td>22.</td>
<td>Hardware automatically configures and enables the TDO output pin function, which toggles when any PGECx/PGEDx pair are used during programming.</td>
<td>X</td>
</tr>
<tr>
<td>I/O</td>
<td>Injection Current</td>
<td>23.</td>
<td>Non-5(\mathrm{v}) tolerant I/O pins do not support the high-side injection current parameter specification (DI60b) (\mathrm{VIN} &gt; \mathrm{VDD}).</td>
<td>X X</td>
</tr>
<tr>
<td>Input Capture</td>
<td>Debug</td>
<td>24.</td>
<td>Freeze in Debug is not supported when using ICAP with DMA.</td>
<td>X X</td>
</tr>
<tr>
<td>LVD</td>
<td>Interrupt</td>
<td>25.</td>
<td>An HLVD interrupt is a NMI type instead of a user-selectable IEC0&lt;29&gt; interrupt.</td>
<td>X</td>
</tr>
<tr>
<td>LVD</td>
<td>—</td>
<td>26.</td>
<td>The LVD module is non-functional and the HLVD module trip thresholds do not meet the data sheet specifications.</td>
<td>X X</td>
</tr>
<tr>
<td>SOSC</td>
<td>SOSC Crystals</td>
<td>27.</td>
<td>SOSC crystals with ESR &lt;= 50 k(\Omega) fail to oscillate at -40ºC.</td>
<td>X X</td>
</tr>
<tr>
<td>PMP</td>
<td>Input/Output Buffers</td>
<td>28.</td>
<td>The PMP input buffer full flag, IB0F, and the output buffer underflow, OBUF, are getting set as soon as the PMP module is enabled in Slave mode (PMP TTL bit (PMCON&lt;10&gt;) is equal to ‘1’).</td>
<td>X X</td>
</tr>
<tr>
<td>PMP</td>
<td>Interrupts</td>
<td>29.</td>
<td>No PMP interrupts are generated in EPSP mode when the WAITE&lt;1:0&gt; bits (PMMODE&lt;1:0&gt;) are equal to ‘0’.</td>
<td>X X</td>
</tr>
<tr>
<td>RCON</td>
<td>Deep Sleep</td>
<td>30.</td>
<td>If the DSEN bit (DSCON&lt;15&gt;) is equal to ‘1’, Deep Sleep Enable is set during a VDD nominal to BOR back to VDD nominal event, the Deep Sleep Status bit, DPSLP (RCON&lt;10&gt;) is set even though Deep Sleep mode was never entered.</td>
<td>X</td>
</tr>
<tr>
<td>RTCC</td>
<td>RTCC</td>
<td>31.</td>
<td>The RTCC module does not function in VBAT mode.</td>
<td>X X</td>
</tr>
<tr>
<td>SPI</td>
<td>TMR1 Register</td>
<td>32.</td>
<td>The Shift Register Empty Status bit, SRMT (SPIxSTAT&lt;7&gt;), may be incorrect when the shift register becomes empty when a transmit becomes empty at the same time.</td>
<td>X X</td>
</tr>
<tr>
<td>Timer1</td>
<td>TMR1 Register</td>
<td>33.</td>
<td>In Asynchronous mode, the TMR1 register remains at the initial set value for 5 external clock pulses after wake-up from Sleep mode.</td>
<td>X X</td>
</tr>
<tr>
<td>Timer1</td>
<td>Counter Mode</td>
<td>34.</td>
<td>In asynchronous external counter mode, Timer1 does not reflect the first count from an external T1CLK input.</td>
<td>X X</td>
</tr>
<tr>
<td>Timer1</td>
<td>Asynchronous Mode</td>
<td>35.</td>
<td>In Asynchronous mode, Timer 1 counts beyond the period value when the period is 0x01.</td>
<td>X X</td>
</tr>
<tr>
<td>Timer1</td>
<td>Gated Mode</td>
<td>36.</td>
<td>Timer1 does not work properly in Gated mode with the prescaler enabled.</td>
<td>X X</td>
</tr>
<tr>
<td>Timer1</td>
<td>TMR1 Register Writes</td>
<td>37.</td>
<td>Back-to-back writes to the TMR1 register are not allowed for four PBCLK cycles.</td>
<td>X X</td>
</tr>
<tr>
<td>Timer1</td>
<td>Asynchronous Timer</td>
<td>38.</td>
<td>The Asynchronous Timer Write Disable bit, TWDIS (TxCN&lt;12&gt;), and the Asynchronous Timer Write in Progress bit, TWIP (TxCN&lt;11&gt;), are non-functional.</td>
<td>X X</td>
</tr>
<tr>
<td>Timer1</td>
<td>Reset</td>
<td>39.</td>
<td>The Timer1 TCK input propagates undefined values if left floating after a Reset.</td>
<td>X X</td>
</tr>
</tbody>
</table>

Note 1: Only those issues indicated in the last column apply to the current silicon revision.
### TABLE 2: SILICON ISSUE SUMMARY (CONTINUED)

<table>
<thead>
<tr>
<th>Module</th>
<th>Feature</th>
<th>Item</th>
<th>Issue Summary</th>
<th>Affected Revisions&lt;sup&gt;(1)&lt;/sup&gt;</th>
</tr>
</thead>
<tbody>
<tr>
<td>Timer2-Timer5</td>
<td>Debug Breakpoint</td>
<td>40.</td>
<td>On a debug breakpoint, TMRx, x=2-5, may not be representative of the correct value.</td>
<td>X X</td>
</tr>
<tr>
<td>Timer2-Timer5</td>
<td>Internal Output</td>
<td>41.</td>
<td>Internal Output clock to various peripherals, such as Output Compare modules, are not gated OFF on an active TxCK input, despite the TGATE bit (TxCON&lt;7&gt;) being disabled (i.e., set to '0').</td>
<td>X X</td>
</tr>
<tr>
<td>Timer2-Timer5</td>
<td>Period Match</td>
<td>42.</td>
<td>Timer TMR event trigger/interrupt on a period match may not occur if it coincides with entry into Sleep mode.</td>
<td>X X</td>
</tr>
<tr>
<td>USB</td>
<td>Interrupts</td>
<td>43.</td>
<td>UIDLE interrupts cease if the UIDLE interrupt flag is cleared.</td>
<td>X X</td>
</tr>
<tr>
<td>USB</td>
<td>Specifications</td>
<td>44.</td>
<td>USB D+/D- Rise/Fall Times do not meet the data sheet specifications with five meter cable greater than +55ºC.</td>
<td>X X</td>
</tr>
<tr>
<td>USB</td>
<td>Low-Speed</td>
<td>45.</td>
<td>When the USB module is configured for Low-Speed operation, (i.e., LSPD bit (U1EPx&lt;7&gt;) = 1), the interrupt timer sets the T1MSECIF interrupt status flag (U1OTGIR&lt;T1MSECIF&gt;) every 8 ms instead of the expected 1 ms.</td>
<td>X X</td>
</tr>
<tr>
<td>USB</td>
<td>Activity Status</td>
<td>46.</td>
<td>If SYSCLK slowed to less than 16 MHz while the USB link is idle, powered-down, or detached, software may not receive indication of USB activity Resume, SRP, HNP or reattach soon enough to meet the USB protocol. USB interrupts may also not be asserted in time.</td>
<td>X X</td>
</tr>
<tr>
<td>PMP</td>
<td>Slave Mode</td>
<td>47.</td>
<td>PMP in slave when in TTL mode is de-featured.</td>
<td>X X</td>
</tr>
<tr>
<td>IVREF</td>
<td>Comparator</td>
<td>48.</td>
<td>Internal 1.2v IVREF reference is not supported for use with comparator reference.</td>
<td>X X</td>
</tr>
<tr>
<td>CTMU</td>
<td>CTMU</td>
<td>49.</td>
<td>Capacitive measurement and time measurement features are not supported.</td>
<td>X X</td>
</tr>
<tr>
<td>Deep Sleep</td>
<td>IPD</td>
<td>50.</td>
<td>Deep Sleep current exceeds maximum specification from -40ºc to 0ºc.</td>
<td>X X</td>
</tr>
<tr>
<td>UART</td>
<td>High-Speed Mode</td>
<td>51.</td>
<td>The UART Stop bit duration is shorter than expected in High-Speed mode (UxMODE.BRGH = 1) for baud rates less than 7.5 MBPS.</td>
<td>X X</td>
</tr>
<tr>
<td>SOSC</td>
<td>SOSCRDY</td>
<td>52.</td>
<td>SOSCRDY may not properly reflect SOSC status when SOSC is disabled.</td>
<td>X X</td>
</tr>
<tr>
<td>USB Low-Speed Mode</td>
<td>Low-Speed Mode</td>
<td>53.</td>
<td>USB Low-Speed Device and Host modes are not supported.</td>
<td>X X</td>
</tr>
</tbody>
</table>

**Note 1:** Only those issues indicated in the last column apply to the current silicon revision.
Silicon Errata Issues

1. Module: ADC
Converting the Internal IVREF Band Gap, 1.2V, (internal AN14), the voltage source is not supported and will yield indeterminate results.

Work around
None.

Affected Silicon Revisions

<table>
<thead>
<tr>
<th>A1</th>
<th>A3</th>
</tr>
</thead>
<tbody>
<tr>
<td>X</td>
<td>X</td>
</tr>
</tbody>
</table>

2. Module: CLKO
During any active reset, the OSC2/CLKO/RPA3/RA3 pin defaults temporarily to the CLKO output pin. A clock signal is present on the CLKO pin, regardless of the clock source and setting of the CLKO Enable Configuration bit, while the device is in Reset.

Work around
None.

Affected Silicon Revisions

<table>
<thead>
<tr>
<th>A1</th>
<th>A3</th>
</tr>
</thead>
<tbody>
<tr>
<td>X</td>
<td>X</td>
</tr>
</tbody>
</table>

3. Module: Configuration Words
Configuration Words mismatch logic is non-functional. Conversely, no device Reset as defined by the CMR bit (RCON<9>) would result from a very rare run-time Flash Configuration Word(s) bit change.

Work around
None.

Affected Silicon Revisions

<table>
<thead>
<tr>
<th>A1</th>
<th>A3</th>
</tr>
</thead>
<tbody>
<tr>
<td>X</td>
<td>X</td>
</tr>
</tbody>
</table>

4. Module: CTMU
Edge Sequencing mode, controlled by the EDGSEQUEN bit (CTMU<2>), and Edge mode are not functional.

Work around
Use level modes instead.

Affected Silicon Revisions

<table>
<thead>
<tr>
<th>A1</th>
<th>A3</th>
</tr>
</thead>
<tbody>
<tr>
<td>X</td>
<td>X</td>
</tr>
</tbody>
</table>

5. Module: CTMU
When set, the Edge Enable bit, EDGEN (CTMU<11>), generates a glitch on the selected CTEDx input, which causes a false trigger.

Work around
None.

Affected Silicon Revisions

<table>
<thead>
<tr>
<th>A1</th>
<th>A3</th>
</tr>
</thead>
<tbody>
<tr>
<td>X</td>
<td>X</td>
</tr>
</tbody>
</table>

6. Module: CTMU
Temperature sensor measurement is not supported for the IRNG<1:0> bits (CTMU<1:0> = '0b01 and '0b10, current range 1 or 2.

Work around 1
Use IRNG<1:0> bit '0b00 or '0b11.

Work around 2
Set the ADC sample rate for the temperature sensor to less than 1 kbps.

Affected Silicon Revisions

<table>
<thead>
<tr>
<th>A1</th>
<th>A3</th>
</tr>
</thead>
<tbody>
<tr>
<td>X</td>
<td>X</td>
</tr>
</tbody>
</table>

7. Module: CTMU
Internal temperature sensor accuracy does not meet ±2°C specification, instead it is ±6°C.

Work around
None.

Affected Silicon Revisions

<table>
<thead>
<tr>
<th>A1</th>
<th>A3</th>
</tr>
</thead>
<tbody>
<tr>
<td>X</td>
<td>X</td>
</tr>
</tbody>
</table>
8. Module: CTMU

If the ADC module is enabled in Idle mode, it should override the setting of the CTMUSIDL bit (CTMUCON<13>) = 1, (i.e., discontinue CTMU module operation when the device enters Idle mode), and if the ADC module attempts to make a CTMU temperature sensor measurement. However, it cannot because CTMU current sources aren't enabled in Idle mode.

Work around

Set the CTMUSIDL bit to '0' to continue module operation when the device enters Idle mode.

Affected Silicon Revisions

<table>
<thead>
<tr>
<th>A1</th>
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<tbody>
<tr>
<td>X</td>
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</tr>
</tbody>
</table>

9. Module: CTMU

The CTMU is greater than the maximum current sourcing range specifications in the data sheet when the IRNG bits in the CTMUCON register are set to '0b00 (715 µA max.) and '0b11 (71.5 µA max.), and when the device ambient temperature is less than +90ºC.

Work around

None.

Affected Silicon Revisions

<table>
<thead>
<tr>
<th>A1</th>
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<tbody>
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</table>

10. Module: CTMU

When Time Generation mode is enabled by setting the TGEN bit (CTMUCON<12>), the manual current sourcing set by the EDG1STAT bit (CTMUCON <24>) from the CTMU is non-functional.

Work around

None.

Affected Silicon Revisions

<table>
<thead>
<tr>
<th>A1</th>
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<tbody>
<tr>
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</table>

11. Module: Deep Sleep

The user application must not attempt to enter Deep Sleep mode for a period of 50 µs after exiting Reset on start-up or the device will never recover and is no longer able to be erased and/or reprogrammed.

Work around

Insure application does not enter deep sleep mode for at least 50 µs after any reset. Institute 50 µs delay using timer or software delay loop.

Affected Silicon Revisions

<table>
<thead>
<tr>
<th>A1</th>
<th>A3</th>
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<tbody>
<tr>
<td>X</td>
<td>X</td>
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</tbody>
</table>

12. Module: Deep Sleep

On transition from Deep Sleep mode to VBAT mode, the semaphore DSGPR1 register does not retain its content as expected.

Work around

Enable DSBOR.

Affected Silicon Revisions

<table>
<thead>
<tr>
<th>A1</th>
<th>A3</th>
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<tbody>
<tr>
<td>X</td>
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</tr>
</tbody>
</table>

13. Module: Deep Sleep

If a rare Configuration Word bit mismatch occurs while in Deep Sleep, the device will be non-functional until a POR.

Work around

None.

Affected Silicon Revisions

<table>
<thead>
<tr>
<th>A1</th>
<th>A3</th>
</tr>
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<tbody>
<tr>
<td>X</td>
<td>X</td>
</tr>
</tbody>
</table>
14. Module: Deep Sleep
Inconsistent DSBOR status bit (DSCON<1>) values occur after a Deep Sleep BOR event.

**Work around**
None.

**Affected Silicon Revisions**

<table>
<thead>
<tr>
<th>A1</th>
<th>A3</th>
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<th>X</th>
</tr>
</thead>
</table>

15. Module: Deep Sleep
Exceeds maximum Deep Sleep current specification at less than +25ºC:
- At 0ºC, 5000 nA instead of 500 nA
- At -40ºC, 7500 nA instead of 150 nA

**Work around**
None.

**Affected Silicon Revisions**

<table>
<thead>
<tr>
<th>A1</th>
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</thead>
</table>

16. Module: Deep Sleep
Upon wake-up from Deep Sleep, the DSWAKE register does not always indicate the correct wake-up event source.

**Work around**
None.

**Affected Silicon Revisions**

<table>
<thead>
<tr>
<th>A1</th>
<th>A3</th>
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</thead>
</table>

17. Module: Deep Sleep
When Deep Sleep is enabled, DPSLP bit (RCON<10>) = 1, the DPSLP Deep Sleep Mode status bit (DPSLP) is incorrectly set on exit from VBAT even though Deep Sleep mode was not entered after a BOR/POR reset event.

**Work around**
None.

**Affected Silicon Revisions**

<table>
<thead>
<tr>
<th>A1</th>
<th>A3</th>
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</thead>
</table>

18. Module: FSCM
The Fail-Safe Clock Monitor should be a Non-maskable Interrupt (NMI) instead of a general purpose user-selectable IEC0<29> interrupt.

**Work around**
None.

**Affected Silicon Revisions**

<table>
<thead>
<tr>
<th>A1</th>
<th>A3</th>
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<th>X</th>
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</table>

19. Module: I²C
The I²C module and SFRs are reset after entry into Idle mode when the SIDL bit (I2CxCON<13>) is set to ‘1’ and module operation discontinues when the device enters Idle mode.

**Work around**
None.

**Affected Silicon Revisions**

<table>
<thead>
<tr>
<th>A1</th>
<th>A3</th>
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</table>

20. Module: I²C
When the I²C module is in Slave mode, Start and Restart Interrupts are not occurring or properly reflected in the IFSx flag bits on all devices.

**Work around**
Use software polling to test the I²C Start/Restart status bit, S (I2CxSTAT<3>).

**Affected Silicon Revisions**

<table>
<thead>
<tr>
<th>A1</th>
<th>A3</th>
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<th>X</th>
</tr>
</thead>
</table>
21. Module: I²C
The I²C Start bit, S (I2C1STAT<3>), is not cleared and the Stop bit, P (I2C1STAT<4>), is not set when an external I²C master creates a Stop condition immediately after a Start condition.

Work around
None.

Affected Silicon Revisions

<table>
<thead>
<tr>
<th>A1</th>
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<tbody>
<tr>
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</table>

22. Module: TDO
Hardware automatically configures and enables the TDO output pin function, which toggles when any PGECx/PGEDx pair is used during programming.

Work around
None.

Affected Silicon Revisions

<table>
<thead>
<tr>
<th>A1</th>
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</table>

23. Module: I/O
Non-5v tolerant I/O pins do not support the high-side injection current parameter specification DI60b (i.e., VIN > VDD). Even if the injection current is limited to less than 5 mA, a device reset can occur.

Work around
None.

Affected Silicon Revisions

<table>
<thead>
<tr>
<th>A1</th>
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<tbody>
<tr>
<td>X</td>
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</table>

24. Module: Input Capture
Freeze in Debug not supported when using ICAP with DMA.

Work around
None.

Affected Silicon Revisions

<table>
<thead>
<tr>
<th>A1</th>
<th>A3</th>
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<tbody>
<tr>
<td>X</td>
<td>X</td>
</tr>
</tbody>
</table>

25. Module: LVD
A HLVD interrupt is a NMI type instead of a general purpose user selectable IEC0<29> interrupt.

Work around
None.

Affected Silicon Revisions

<table>
<thead>
<tr>
<th>A1</th>
<th>A3</th>
</tr>
</thead>
<tbody>
<tr>
<td>X</td>
<td></td>
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</table>

26. Module: LVD
The LVD module is non-functional the HLVD module trip thresholds do not meet the data sheet specifications.

Work around
None.

Affected Silicon Revisions

<table>
<thead>
<tr>
<th>A1</th>
<th>A3</th>
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</thead>
<tbody>
<tr>
<td>X</td>
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</tr>
</tbody>
</table>

27. Module: SOSC
SOSC crystals with ESR less than or equal to 50 kΩ fail to oscillate at -40ºC.

Work around
Select SOSC crystals with an ESR greater than 50 kΩ.

Affected Silicon Revisions

<table>
<thead>
<tr>
<th>A1</th>
<th>A3</th>
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<tbody>
<tr>
<td>X</td>
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</table>

28. Module: PMP
The PMP input buffer full flag, IB0F, and the output buffer underflow flag, OBUF, are set as soon as the PMP module is enabled in Slave mode (PMPTTL bit (PMCON<10>) is equal to '1').

Work around
During PMP slave mode initialization and before PMP interrupts are enabled, clear the input buffer full flag (IB0F bit (PMSTAT<8>) and the output buffer underflow flag (OBUF bit (PMSTAT<6>) when clearing any pending IFSx interrupt flags.

Affected Silicon Revisions

<table>
<thead>
<tr>
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<tbody>
<tr>
<td>X</td>
<td>X</td>
</tr>
</tbody>
</table>
29. Module: PMP
No PMP interrupts are generated in Enhanced Parallel Slave Port (EPSP) mode when the WAITE<1:0> bits (PMMODE<1:0>) are equal to ‘0’.

Work around
None.

Affected Silicon Revisions

<table>
<thead>
<tr>
<th>A1</th>
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<tr>
<td>x</td>
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</tbody>
</table>

30. Module: RCON
If the DSEN bit (DSCON<15>) is equal to ‘1’, Deep Sleep Enable is set during a VDD to BOR back to VDD event, the Deep Sleep Status bit, DPSLP (RCON<10>) is set even though Deep Sleep mode was never entered.

Work around
None.

Affected Silicon Revisions

<table>
<thead>
<tr>
<th>A1</th>
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<tr>
<td>x</td>
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</table>

31. Module: RTCC
The RTCC module does not function in VBAT mode. The RTCC timer does not increment, and therefore, does not keep time.

Work around
None.

Affected Silicon Revisions

<table>
<thead>
<tr>
<th>A1</th>
<th>A3</th>
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<tbody>
<tr>
<td>x</td>
<td>x</td>
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</table>

32. Module: SPI
The Shift Register Empty status bit, SRMT (SPIxSTAT<7>), may be incorrect when the shift register becomes empty when a transmit becomes empty at the same time.

Work around
None.

Affected Silicon Revisions

<table>
<thead>
<tr>
<th>A1</th>
<th>A3</th>
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<tbody>
<tr>
<td>x</td>
<td>x</td>
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</table>

33. Module: Timer1
In Asynchronous mode, (i.e., TCS bit (T1CON<1> = 1, TSYNC bit (T1CON<2> = 0, and TCS<1:0> (T1CON<9:8> = ‘0b01), the TMR1 register remains at the initial set value for 5 external clock pulses after wake-up from Sleep mode.

Work around
None.

Affected Silicon Revisions

<table>
<thead>
<tr>
<th>A1</th>
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<tbody>
<tr>
<td>x</td>
<td>x</td>
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</tbody>
</table>

34. Module: Timer1
In Asynchronous mode, (i.e., TCS bit (T1CON<1> = 1, TSYNC bit (T1CON<2> = 0, and TCS<1:0> (T1CON<9:8> = ‘0b01), Timer1 does not reflect the first count from an external T1CLK input

Work around
None.

Affected Silicon Revisions

<table>
<thead>
<tr>
<th>A1</th>
<th>A3</th>
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</thead>
<tbody>
<tr>
<td>x</td>
<td>x</td>
<td></td>
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</tbody>
</table>

35. Module: Timer1
Timer1 counts beyond the period value in Asynchronous mode when the period is 0x01.

Work around
Set Timer1 period, PR1 to greater than 1.

Affected Silicon Revisions

<table>
<thead>
<tr>
<th>A1</th>
<th>A3</th>
<th></th>
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<tbody>
<tr>
<td>x</td>
<td>x</td>
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</tr>
</tbody>
</table>

36. Module: Timer1
Timer1 does not work properly in Gated mode (i.e., TGATE bit (T1CON<7>) = 1, TCS bit (T1CON<1> = 0) with the prescaler enabled (TCKPS<1:0> bits (T1CON<5:4>) = ‘0b00).

Work around
None.

Affected Silicon Revisions

<table>
<thead>
<tr>
<th>A1</th>
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<tbody>
<tr>
<td>x</td>
<td>x</td>
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</tbody>
</table>
37. Module: Timer1

Back-to-back CPU writes to the TMR1 register are not allowed for at least four PBCLK cycles.

Work around
None.

Affected Silicon Revisions

<table>
<thead>
<tr>
<th>A1</th>
<th>A3</th>
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<tbody>
<tr>
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<td>X</td>
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</table>

38. Module: Timer1

The Asynchronous Timer Write Disable bit, TWDIS (TxCON<12>), and the Asynchronous Timer Write in Progress bit, TWIP (TxCON<11>), are non-functional.

Work around
None.

Affected Silicon Revisions

<table>
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<tr>
<th>A1</th>
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<tbody>
<tr>
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<td>X</td>
</tr>
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</table>

39. Module: Timer1

The Timer1 external TCK input pin propagates undefined values if left floating after a Reset.

Work around
Place a 10k pull-down resistor on the T1CLK pin.

Affected Silicon Revisions

<table>
<thead>
<tr>
<th>A1</th>
<th>A3</th>
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<tbody>
<tr>
<td>X</td>
<td>X</td>
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</tbody>
</table>

40. Module: Timer2-Timer5

On a debug breakpoint, TMRx, where ‘x’ = 2-5, may not be representative of the correct count value.

Work around
None.

Affected Silicon Revisions

<table>
<thead>
<tr>
<th>A1</th>
<th>A3</th>
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<tbody>
<tr>
<td>X</td>
<td>X</td>
</tr>
</tbody>
</table>

41. Module: Timer2-Timer5

The Timerx internal output clock to various peripherals, such as Output Compare modules, are not gated OFF on an active TxCK input, despite the TGATE bit (TxCON<7>) being disabled (i.e., set to ‘0’). This condition may affect other peripherals that may utilize them.

Work around
None.

Affected Silicon Revisions

<table>
<thead>
<tr>
<th>A1</th>
<th>A3</th>
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<tbody>
<tr>
<td>X</td>
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</table>

42. Module: Timer2-Timer5

A Timer TMR event trigger/interrupt on a period match may not occur if it coincides with entry into Sleep mode.

Work around
None.

Affected Silicon Revisions

<table>
<thead>
<tr>
<th>A1</th>
<th>A3</th>
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<tbody>
<tr>
<td>X</td>
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</tbody>
</table>

43. Module: USB

If the Idle Detect Interrupt Enable bit (IDLEIE bit (U1IE<4>)), is equal to ‘1’ and the bus has been idle for more than 3 ms while the UIDLE interrupt flag is set; if software clears the interrupt flag and the bus remains idle, the UIDLE interrupt flag will not re-trigger a second time even after an additional 3 ms of J-state bus Idle condition.

Work around
Software can leave the UIDLE bit set until it has received some indication of bus resumption like “Resume” or “Reset”. If, any time, the UIDLE bit is set, it would be acceptable to suspend the USB module, as long as this code is protected by USB Sleep Entry Guard (USLPGRD (U1PWRC<4>)) and USB Activity Pending (UACTPND (U1PWRC<7>)). Note that this will require software to clear the UIDLE interrupt enable bit to exit the USB ISR if using interrupt-driven code.

Work around
None.

Affected Silicon Revisions

<table>
<thead>
<tr>
<th>A1</th>
<th>A3</th>
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<tbody>
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</tbody>
</table>

44. Module: USB

USB D+/D- Rise/Fall Times do not meet the specification with a 5 meter cable greater than +55°C. This will not affect certification as it is performed at +25°C.

Work around 1

---

DS80000739E-page 10 © 2017-2020 Microchip Technology Inc.
Insure the USB cable is less than 3 meters in length.

**Work around 2**

Insure ambient device temperature of less than +55°C.

**Affected Silicon Revisions**

<table>
<thead>
<tr>
<th>A1</th>
<th>A3</th>
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</table>

45. **Module: USB**

When the USB module is configured for Low-Speed operation, (i.e., LSPD bit (U1EPx<7>) = 1), the interrupt timer sets the T1MSECIF interrupt status flag (U1OTGIR<T1MSECIF>) every 8 ms instead of the expected 1 ms.

**Work around**

Instead, use a general purpose timer for a period of 1 ms.

**Affected Silicon Revisions**

<table>
<thead>
<tr>
<th>A1</th>
<th>A3</th>
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<tbody>
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</tbody>
</table>

46. **Module: USB**

If SYSCLK is slowed to less than 16 MHz while the USB link is idle, powered-down, or detached then the software may not receive indication of USB activity Resume, SRP, HNP, or reattach soon enough to meet the USB protocol. USB interrupts may also not be asserted in time.

**Work around**

None.

**Affected Silicon Revisions**

<table>
<thead>
<tr>
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<tr>
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</tr>
</tbody>
</table>

47. **Module: PMP**

PMP in Slave mode PMMODE<9:8> = 0b00 or 0b01 (i.e., MODE<1:0>) and PMCON<10>=1, (i.e., PMPTTL). The PMP module uses TTL input buffers then CS de-asserts before RD or WR strobe violating hold time requirements.

**Work around**

Use in Schmitt Trigger input buffer mode PMCON<10>=0 (i.e., PMPTTL=0).

48. **Module: IVREF**

Internal 1.2V IVREF reference is not supported for use with comparator reference.

**Work around**

Use CMxCON<4> (i.e., CREF) instead as the comparator voltage reference source.

**Affected Silicon Revisions**

<table>
<thead>
<tr>
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</table>

49. **Module: CTMU**

The current sources of the various ranges are not constant as expected, therefore the capacitive and time measurement features of the CTMU are not supported.

**Work around**

None.

**Affected Silicon Revisions**

<table>
<thead>
<tr>
<th>A1</th>
<th>A3</th>
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<tbody>
<tr>
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</tr>
</tbody>
</table>
50. Module: Deep Sleep

Exceeds maximum Deep Sleep current specification upon initial entry into Deep Sleep from -40ºc to 0ºc:

<table>
<thead>
<tr>
<th>Temp</th>
<th>DS &lt;35 sec</th>
<th>DS +45 sec</th>
<th>DS +100 sec</th>
<th>DS &gt;150 sec</th>
</tr>
</thead>
<tbody>
<tr>
<td>-40ºc</td>
<td>500 µA</td>
<td>80 µA</td>
<td>20 µA</td>
<td>3 µA</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Temp</th>
<th>DS &lt;32 sec</th>
<th>DS +60 sec</th>
<th>DS +90 sec</th>
<th>DS &gt;130 sec</th>
</tr>
</thead>
<tbody>
<tr>
<td>0ºc</td>
<td>180 µA</td>
<td>45 µA</td>
<td>15 µA</td>
<td>0.5 µA</td>
</tr>
</tbody>
</table>

Note: “DS” stands for Deep Sleep entry.

Work around

None.

Affected Silicon Revisions

A1  A3
X   X

51. Module: UART

The UART TX Stop bit duration is shorter than the expected in High-Speed mode (BRGH (UxMODE<3>) = 1) for baud rates less than 7.5 MBPS.

Work around

For baud rates less than 7.5 MBPS, operate the UART in Standard-Speed mode, that is, BRGH (UxMODE<3>) = 0. For baud rates greater than 7.5 MBPS operate the UART in High-Speed mode, that is, BRGH (UxMODE<3>) =1.

Affected Silicon Revisions

A1  A3
X   X

52. Module: SOSC

CLKSTAT.SOSCRDY remains a high when the SOSC is Off (OSCCON.SOSCEN = 0). CLKSTAT.SOSCRDY accurately reflects crystal status when SOSC is On (OSCCON.SOSCEN = 1).

Work around

None.

Affected Silicon Revisions

A1  A3
X   X

53. Module: USB Low-Speed Mode

USB Low-Speed mode is not functional in both Device and Host modes due to signal integrity compliance issues.

Work around

None.

Affected Silicon Revisions

A1  A3
X   X
Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS60001404E):

<table>
<thead>
<tr>
<th>Note: Corrections are shown in bold. Where possible, the original bold text formatting has been removed for clarity.</th>
</tr>
</thead>
</table>

There are no new data sheet clarifications to report at this time.
APPENDIX A: REVISION HISTORY

Rev A Document (4/2017)
Initial release of this document for revision A1 silicon, which includes the following silicon issues:


Rev B Document (8/2017)
Data Sheet Clarification 1. 28-Lead QFN-S Package was added.
Added silicon issues: 47 (PMP), 48 (IREF), 49 (CTMU), 50 (Deep Sleep).
Updated 1.

Rev C Document (9/2018)
Added silicon issue: 51. UART.

Rev D Document (01/2019)
Added Silicon Revision A3.

Rev E Document (04/2020)
Added Silicon Issue 52. SOSC
Added Silicon Issue 53. USB Low-Speed Mode.
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ISBN: 978-1-5224-5946-0

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## AMERICAS

**Corporate Office**
2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7200
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