

## PIC32CM MC00 Family Data Sheet Clarifications and Silicon Errata

### PIC32CM MC00 Family

The PIC32CM MC00 family of devices that you have received conforms functionally to the current Device Data Sheet (DS60001638B), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in the following table.

The errata described in this document will be addressed in future revisions of the PIC32CM MC00 family of devices.

**Note:** This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current.

Data Sheet clarifications and corrections (if applicable) are located in [Data Sheet Clarifications](#), following the discussion of silicon issues.

**Table 1. PIC32CM MC00 Family Silicon Device Identification**

Devices	Device ID (DID[31:0])	Silicon Revision ID (DID.REVISION[3:0])
		A1
PIC32CM1216MC00032	0x11070x00	0x0
PIC32CM6408MC00032	0x11070x01	0x0
PIC32CM1216MC00048	0x11070x06	0x0
PIC32CM6408MC00048	0x11070x07	0x0

**Note:**

1. Refer to the “*Device Service Unit*” chapter in the current Device Data Sheet (DS60001638B) for a detailed information on Device Identification and Revision IDs for a specific device.

## Silicon Errata Summary

Module	Feature	Errata Number	Issue Summary	Affected Revisions
				A1
<a href="#">NVMCTRL</a>	DATA FLASH	<a href="#">1.1.1</a>	CPU writes to any memory or register while a write or erase operation is ongoing in the Data Flash address space will stall the AHB bus for the duration of the write or erase operation. CPU reads are not impacted..	X
<a href="#">NVMCTRL</a>	CEHL	<a href="#">1.1.2</a>	The CEHL feature is not functional.	X
<a href="#">SERCOM I<sup>2</sup>C</a>	Repeated Start	<a href="#">1.2.1</a>	For Master Write operations (excluding High-Speed mode) in 10-bit addressing mode, writing CTRLB.CMD = 0x1 does not correctly issue a Repeated Start command.	X
<a href="#">SERCOM I<sup>2</sup>C</a>	Repeated Start	<a href="#">1.2.2</a>	For High-Speed Master Write operations, writing CTRLB.CMD = 0x1 issues a STOP command instead of a Repeated Start, making repeated start not possible in that mode.	X
<a href="#">SERCOM I<sup>2</sup>C</a>	NACK and Repeated Start	<a href="#">1.2.3</a>	For High-Speed Master Read operations, sending a NACK (CTRLB.CMD = 0x2) forces a STOP to be issued, making repeated start not possible in that mode.	X
<a href="#">OSCCTRL</a>	FDPLL Unlock	<a href="#">1.3.1</a>	Spurious DPLL unlocks may be detected during operation.	X

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## 1. PIC32CM MC00 Errata Issues

The following issues apply to the PIC32CM MC00 family of devices.

### 1.1 Non-Volatile Memory Controller (NVMCTRL)

#### 1.1.1 DATA FLASH

CPU writes to any memory or register while a write or erase operation is ongoing in the Data Flash address space will stall the AHB bus for the duration of the write or erase operation. CPU reads are not impacted.

The stall duration will be up to the maximum time of the Flash write or erase operation:

Page Write time: 2.5 ms

Row Erase time: 6 ms

Sector Erase time: 8 ms

#### Workaround

Perform Data Flash modify operations in a safe region of the application where CPU writes are not required.

#### Affected Silicon Revisions

A1				
X				

#### 1.1.2 CEHL

The Chip Erase Hard Lock (CEHL) feature is not functional and will not provide any code protection capabilities. The Secure Bit (SB) is not affected, and can be used for code protection.

#### Workaround

None.

#### Affected Silicon Revisions

A1				
X				

## 1.2 SERCOM I<sup>2</sup>C

### 1.2.1 Repeated Start

For Master Write operations (excluding High-Speed mode) in 10-bit Addressing mode, writing CTRLB.CMD = 0x1 does not correctly issue a Repeated Start command.

#### Workaround

Write the same 10-bit address with the same direction bit to the ADDR.ADDR register to generate a Repeated Start.

#### Affected Silicon Revisions

A1				
X				

### 1.2.2 Repeated Start

For High-Speed Master Write operations, writing CTRLB.CMD = 0x1 issues a STOP command instead of a Repeated Start, making repeated start is not possible in that mode.

**Workaround**  
None.

#### Affected Silicon Revisions

A1				
X				

### 1.2.3 NACK and Repeated Start

For High-Speed Master Read operations, sending a NACK (CTRLB.CMD = 0x2) forces a STOP to be issued, making repeated start is not possible in that mode.

**Workaround**  
None.

#### Affected Silicon Revisions

A1				
X				

## 1.3 OSCCTRL

### 1.3.1 FDPLL Unlock

When using FDPLL at temperature below 25°C, spurious DPLL unlocks (OSCCTRL.DPLLSTATUS.LOCK = 0) may be detected while the FDPLL still adheres to the electrical characteristics metrics defined in section 43.16 of the data sheet. During these unlock periods, the DPLL output clock is halted and then restarts.

#### Workaround

When using FDPLL at temperature below 25°C, enable the lock bypass (OSCCTRL.DPLLCTRLB.LBYPASS = 1) to avoid losing FDPLL clock output during a false unlock status. The workaround does not avoid false unlock indications, but it disables the gating of the FDPLL clock output by the lock status; therefore, the clock is issued even if the FDPLL status shows unlocked.

#### Pseudo Code

Set OSCCTRL.DPLLCTRLB.LBYPASS = 1

Set DPLLCTRLA.ENABLE = 1

Wait (OSCCTRL.DPLLSTATUS.CLKRDY = 1)

Set Source for GCLK with DPLL

#### Affected Silicon Revisions

A1				
X				

## **2. Data Sheet Clarifications**

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS60001638B):

**Note:** Corrections in tables, registers, and text are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

There are no Data Sheet Clarifications to report at this time.

### **3. Appendix A: Revision History**

#### **Revision C - 02/2021**

The following update was performed for this revision:

- Added Silicon Issue [OSCCTRL FDPLL Unlock 1.3.1](#)

#### **Revision B - 11/2020**

The following updates were performed for this revision:

- Updated Silicon Die Revision from A0 to A1
- Updated the errata numbering schema to reflect those errata which were removed

#### **Revision A - 07/2020**

This is the initial released version of this document.

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