PIC18F to PIC24F to SAMD2x Migration and Performance Enhancement Guide

INTRODUCTION

This document describes the features of the PIC18F, PIC24F, and SAMD2x architecture. It highlights the differences and similarities of various peripherals, and discusses the factors that need to be considered while migrating from PIC18F to PIC24F, and from PIC24F to SAMD2x. In addition, there have been many updates to the PIC18F architecture, one of the most notable being the addition of Direct Memory Access (DMA). This document notes the differences between the older devices (without DMA) and newer devices (with DMA), both in relation to each other and in relation to PIC24F and the SAMD2x when applicable.

CPU CORE

Note: This migration document details the transition from PIC18F devices to PIC24F devices, and from PIC24F devices to SAMD2x devices. Please note that some features may not be available. Refer to the device-specific data sheet for more details. The device data sheets and errata are available for download from the Microchip Worldwide Website at: http://www.microchip.com.

Although the PIC24F architecture is significantly different from the PIC18F architecture, the PIC24F MCUs can be viewed as a natural extension of the PIC18F devices.

The SAMD2x architecture is comparatively different from the PIC24F architecture. The SAMD2x MCU is based on the ARM® Cortex® M0+ architecture and PIC24F belongs to the MIPS architecture family. This document will help ease migration concerns when moving from one family to another. Most of the changes are data bit width, instruction word size, instruction clocking scheme, and stack and core registers, primarily affect assembly-based programs. Other hardware features have been added to enhance the processing performance. Changes are summarized in Table 1.

TABLE 1: CPU CORE FEATURE COMPARISON

Features	All PIC18F Devices	PIC24F Devices	SAMD2x Device
Instruction Size	16 bits	24 bits	16 bits or 32 bits
Instruction Clocking	TCY = FOSC/4	TCY = FOSC/2	Instructions – single clock cycle Load/Store – 2 clock cycles Memory barrier – 3 clock cycles
Working Registers	1 (W, WREG)	16 (W0-W15)	16 (R0-R15) R0-R12 (General Purpose) R13 (SP - Stack Pointer) R14 (LR - Link Register) R15 (PC - Program Counter)
STATUS Registers	One (STATUS)	Two (STATUS and CORCON)	One (Program Status Register (PSR))
Stack	Hardware, 32 Levels	Software	Software (1)
Hardware Multiplier	8x8	17x17	Fast (Single cycle)
Hardware Divider	No	Hardware Assisted Division Using DIV and REPEAT	No

Features	All PIC18F Devices	PIC24F Devices	SAMD2x Device
Bit Shifting/Rotation	Single Bit, Left or Right, Rotation Only	Barrel Shifting Up to 15 Bits, Left or Right, Shift or Rotate	Logical Left or Right shift, Arithmetic Right shift and Rotate Right
Program Space Visibility (PSV)	No	Yes	No

Note 1: The processor implements two stacks, the main stack and the process stack, with independent copies of the stack pointer. In Thread mode, the CONTROL register controls whether the processor uses the main stack or the process stack. In Handler mode, the processor always uses the main stack.

Migration Considerations

The primary consideration when migrating from PIC18F to PIC24F is that the PIC24F core uses FOSC/2 as its instruction clock, as opposed to the FOSC/4 instruction clock of the PIC18F device. This effectively doubles the instruction rate at the same input clock speed, but also changes the base clock used by many peripherals that utilize the instruction clock as their basis. This frequency change needs to be accounted for when migrating to ensure that peripherals function as expected. Most other changes in the CPU between the PIC18F and the PIC24F devices are handled automatically by the compiler and do not affect programs written in C.

A SAMD2x CPU running at up to 48 MHz consists of clock sources controlled by the SYSCTRL (System Control), Generic Clock Controller (GCLK), and Power Manager.

Clock sources controlled by SYSCTRL provide a time base that is used by other components, such as Generic Clock Generators. Example clock sources are the internal 8 MHz oscillator (OSC8M), External crystal oscillator (XOSC) and the Digital frequency locked loop (DFLL48M).

Generic Clock Generators are programmable prescalers which use the system clock and Generic Clock Multiplexer to generate clocks for peripherals.

The Power Manager (PM) generates and controls the synchronous clocks on the system. This includes the CPU, bus clocks (APB, AHB), as well as the synchronous (to the CPU) user interfaces of the peripherals. It contains clock masks that can turn on or off the user interface of a peripheral, as well as prescalers for the CPU and bus clocks.

As the CPU and the peripherals can be in different clock domains, they are clocked from different clock sources and/or with different clock speeds, some peripheral accesses by the CPU need to be synchronized. In this case the peripheral includes a SYNCBUSY status register that can be used to check if a sync operation is in progress.

Differences Between PIC18F Devices without DMA and PIC18F Devices with DMA

There are few differences in the core between older and newer PIC18F devices that fundamentally change the migration path between them or to PIC24F devices.

MEMORY MAP AND PROGRAM MEMORY

Both the PIC18F and PIC24F architectures use the same general schema for their program memory spaces.

The SAMD2x uses memory mapped architecture. The processor has a default memory map that provides up to 4 GB of addressable memory. Global memory space is divided into code, SRAM, peripherals, IOBUS and System sections.

Aside from the self-evident differences in width, PIC24F devices also incorporate a larger addressing range and enhanced visibility features in data space. The organization of the space and the location of non-program memory features also differ somewhat, and must be considered when porting an application.

The Flash memory of the SAMD2x is a non-volatile memory (NVM) used to store executable instructions as well as some calibration data and default configuration settings. The SAMD2x compilers will use most of the Flash memory addresses to store instructions.

The key differences between the memory organization of PIC18F, PIC24F, and SAMD2x devices are presented in Table 2.

TABLE 2: MEMORY ORGANIZATION FEATURE COMPARISON

Features	PIC18F without DMA	PIC18F with DMA	PIC24F	SAMD2x
Organization	16-bit, Byte Addressable	16-bit, Byte Addressable	24-bit, Word Addressable	32-bit, Word Addressable
Total Addressable Range	4 Mbytes (22-bit magnitude)	4 Mbytes (22-bit magnitude)	8 Mbytes (24-bit magnitude)	2^{32} 8-bit bytes
Maximum Available User Program Space (upper boundary address)	2 Mbytes (1FFFFFh)	2 Mbytes (1FFFFFh)	8 Mbytes (7FFFFFh)	256Kbytes (40000h) (Device Variant A)
Boot Block Support	Most Devices	Most Devices	No	No
Interrupt/Reset/Trap Vectors	00h, 08h, 18h	00h, 08h, 18h (in Legacy mode), Controlled by IVTBASE (in Vectored mode)	00h to 1FFh	E000E100h
Configuration Word Locations	300000h to 30000Fh	300000h to 30FFFFh (whole area is reserved, most devices have fewer Configuration Words)	In the Last Implemented Location of the Flash Program Memory	NVM Base Address (1) + 0x00800000
Device ID Locations	3FFFFEh and 3FFFFFh	3FFFFEh and 3FFFFFh	FF0000h and FF0002h	41002018h

Note 1: Nonvolatile Memory (NVM) is a reprogrammable Flash memory that retains program and data storage even with the power off. The NVM Base address is referred to as the start address of the NVM.

Migration Considerations

The first consideration is the size of the Program Counter (PC). There are 22 bits for PIC18F devices and 24 bits for PIC24F devices, and 32 bits for SAMD2x devices. This largely affects applications that directly write to the Program Counter, as the actual program memory sizes on these devices varies from family to family and is not inherently larger on PIC18F or PIC24F. The second consideration is that if the PIC18F device does not support vectored interrupts, it will have a much smaller reserved space for interrupts than an equivalent PIC24F device (only locations 00h, 08h and 18h, on the PIC18F, with 00h to 1FFh on PIC24F devices).

The SAMD2x devices support nested vectored interrupts which are controlled by the Nested Vectored Interrupt Controller (NVIC), which supports a 32 interrupt line with reserved memory space for interrupts (E000E100h).

On a system reset, the vector table is fixed at address 0x00000000. Privileged software can write to the VTOR (Vector Table Offset Register) to relocate the vector table start address to a different memory location, in the range 0x00000000 to 0xFFFFFF80 in multiples of 256 bytes.

A final consideration is that while most PIC18F devices have hardware support for a dedicated boot block (with separate write/code-protect controls for this section), PIC24F devices do not.

In the SAMD2x, the boot loader section can be allocated at the beginning of the main array in NVM Flash starting at offset zero. The lower rows in the NVM main address space can be allocated as a boot loader section by using the BOOTPROT fuses, the boot loader section is protected by the lock bits corresponding to this address space and by the BOOTPROT [2:0] fuse.

Differences Between PIC18F Devices without DMA and PIC18F Devices with DMA

There are few differences in the program memory between older and newer PIC18F devices that fundamentally change the migration path between them or to PIC24F devices.

DATA MEMORY SPACE

TABLE 3: DATA MEMORY SPACE FEATURE COMPARISON

Features	PIC18F without DMA	PIC18F with DMA	PIC24F	SAMD2x
Addressing Range (size)	12 bits (4,096 bytes maximum)	14 bits (16,384 bytes maximum)	16 bits (65,536 bytes maximum)	32 bits (2^{32} bytes maximum) **(1)**
Segmentation	Linear Range, Banked Addressing; Linear Addressing for Some Instructions	Linear Range, Banked Addressing; Linear Addressing for Some Instructions	Linear Range, No Segmentation	N/A
Special Access Areas	Access RAM (bottom of lowest bank, top of highest bank)	Access RAM (bottom of lowest bank, top of highest bank)	Near Data Space (bottom 8k)	No
SFR Location	Top n Banks (depending on number of peripherals/SFRs)	Top n Banks (depending on number of peripherals/SFRs)	Distributed throughout Near Memory	Peripherals section (AHB-APB bridge)
Stack	Hardware, 32 Levels Deep, Not Mapped in Memory Space	Hardware, 32 Levels Deep, Not Mapped in Memory Space	Soft Stack Starting at 0800h, User-Configurable End of Stack	Part of Internal SRAM, user-configurable size through linker script
Data Access	Byte (direct or indirect)	Byte (direct or indirect)	Double word, word or Byte (all direct or indirect)	Double word, word, Byte and Half word (direct or indirect)
Hardware PSV	No	No	Yes, Into Top Half of Data Space	No

Note 1: This is the maximum size from core perspective. For the specific device, Refer to the memories section in the data sheet.

Address Range and Segmentation

Older PIC18F devices have a data memory space with a 12-bit address range. In theory, the data space has a linear range and can be addressed directly by several of the PIC18F instructions. For the most part, however, the data space functions as a segmented space. Since most PIC18F instructions can only contain the eight lower bits of a data address, the data space is effectively divided into 16 banks of 256 bytes each. The exact memory location is also determined by the Bank Select Register (BSR), which contains the upper four bits of the address. The entire range of the data space is 4 Kbytes, of which some or all, may be implemented as data RAM.

Some newer PIC18F devices have a data memory space with a 14-bit address range. They act similarly to older PIC18F devices, with the exception that there are up to 64 banks of 256 bytes, and a 6-bit BSR instead of a 4-bit one. Similarly, this puts the entire range of the data space at 16 Kbytes instead of 4 Kbytes.

In contrast, the PIC24F data space is implemented as a single linear range of addresses. Most instructions can directly access any address within the first 8 Kbytes of the range without the use of bank selection. The entire data space range is 64 Kbytes. Of this, only the first 32 Kbytes are implementable as data RAM; the upper 32 Kbytes are a virtual memory space that is used for PSV, refer to **"Program Space Visibility"**. The differences between the data memory organization of the PIC18F, PIC24F, and SAMD2x devices are presented in Table 3.

The internal high-speed RAM on the SAMD2x devices enables the CPU to read or write the application data in a single instruction cycle. Refer to the data sheet for memory on the device.

SFR LOCATIONS

In PIC18F architecture, all SFRs are located at the very top of data memory as a more or less contiguous block (actual addresses depend on the device in question; as previously mentioned, newer devices have a larger data range). In PIC24F architecture, SFRs reside in the lowest 2 Kbytes of the memory space, from addresses, 0000h through 07FFh.

In the SAMD2x architecture, SFRs reside in memory space, from addresses 40000000h through 43000000h. This memory is divided in to AHB-APB peripheral bridges.

SPECIAL ACCESS AREAS

The effective segmentation of the PIC18F data space makes it necessary for some way of accessing SFRs and critical application data quickly. This is done by creating a virtual data space bank, known as the Access RAM, which is composed of the lower half of the lowest bank and the upper half of the upper bank. This scheme makes certain that the SFR space is always available, regardless of the contents of the BSR. Use of the Access RAM is included as an argument in PIC18F assembly language and is hard-coded in the instruction's opcode. In the PIC24F data space, the first 8 Kbytes of data RAM, between the addresses of 0000h and 1FFFh, are referred to as the Near Data Space. Addresses in this space, including all SFRs, are accessible directly from all Direct Memory Access (DMA) instructions.

In the SAMD2x, no special access areas in the data SRAM exist. SFRs are accessed through the AHB-APB bridge memory mapped addresses. Peripheral registers and the registers controlling the I/O pins are mapped to memory locations. The CPU accesses the peripherals and I/O pin registers by reading or writing to specific mapped memory addresses. Peripherals are accessed through one of three peripheral bridges. Direct access to the I/O pins is accomplished by accessing the IOBUS mapped addresses. The processor implements a dedicated single-cycle I/O port. The single-cycle I/O port is memory mapped and supports all the load and store instructions providing single-cycle access to peripherals.

PROGRAM SPACE VISIBILITY

Both PIC18F and PIC24F architectures allow for the direct access of information stored in the program memory space as data. For PIC18F, data from program memory are read in the data space by the use of TBLRD commands, with access being done on a word-by-word basis. For PIC24F devices, program memory is also made available through hardware-enabled Program Space Visibility (PSV). When used, any 32 Kbyte segment of the program space may be mapped into the upper 32 Kbyte area of the data space on a read-only basis. PSV uses a hardware register, PSVPAG, to define which page of program memory will be mapped. The PSV is controlled in software by the PSV bit (CORCON).

PROGRAM STACK

As discussed in the **"CPU Core"** section on page 1, PIC18F devices use a hardware stack for program flow management. The stack is not memory-mapped and has a fixed size of 32 levels, but the Top-of-Stack (TOS) is mapped through the TOSU/H/L and STKPTR SFRs. PIC24F architecture uses a stack implemented entirely in mapped data space. The stack begins at 0800h in Near Data Space, just outside of the SFR area, and grows towards higher memory addresses using the W15 register as a dedicated pointer. The size of the stack is entirely user-defined with the SFR register, SPLIM, which sets the address for stack overflow traps.

The SAMD2x stack is part of the internal SRAM memory. The processor uses a full descending stack. This means the stack pointer indicates the last stacked item on the stack memory. When the processor pushes a new item onto the stack, it decrements the stack pointer, then writes the item to the new memory location. Stacks can be configurable from where to start, then it descends from the top of its configured region.

DATA ACCESS

PIC18F architecture can only work with data in terms of bytes. In contrast, the PIC24F data space, organized in 2-byte words, allows many instructions to work with data as bytes, words or double words (32 bytes). The data type is determined by the argument used with the instruction.

The SAMD2x architecture can operate on bytes, halfword, word, and double words. Processor control registers are only accessible using word transfers. Any attempt to read or write a halfword or byte is unpredictable.

READ-WHILE WRITING

The SAMD2x devices have Read-While Writing (RWW) capability. RWW is the portion of the Flash array that can be set to emulate the EEPROM. The amount of Flash available for EEPROM emulation is established by the Non-Volatile Memory Controller (NVMCTRL).

INTERRUPT CONTROLLER

The PIC24F interrupt controller contains several expansions on the legacy PIC18F. In addition, newer PIC18F devices have added a “vectored interrupt” feature that adds a number of increased user options for interrupts.

The SAMD2x supports the Nested Vectored Interrupt Controller (NVIC). All External interrupt signals are connected to the NVIC, and the NVIC prioritizes the interrupts.

Table 4 summarizes the differences between the devices.

TABLE 4: INTERRUPT CONTROLLER FEATURE COMPARISON

Features	PIC18F without DMA	PIC18F with DMA	PIC24F	SAMD2x
Assignable Interrupt Priority	High or Low	High or Low	8 Levels, User-Defined	4 Levels (0 - Highest Priority)
Interrupt Latency	3 or 4 TCY	2 TCY (vectored interrupts disabled) or 3 TCY (vectored interrupts enabled)	5 TCY (fixed)	15 Cycles
Priority Exit from Sleep and Idle Modes	No	No	Yes	Yes
Interrupt Nesting and Disable Option	No	No	Yes	Yes
Software-Selectable Core Interrupt Priority Level (IPL)	No(1)	No(1)	Yes	Yes
Trap Vectors	No	No	Yes (4)	Supports Hard Faults (2)
Unique Interrupt/Trap Source	No	Yes, Interrupt Vector Table (IVT)	Yes	No
Alternate Interrupt Vector Table (AIVT)	No	Yes, Vector Table Base Address is Fully Relocatable	Yes, Two Choices	Relocation of the vector table
Natural Priority Unmaskable or Non-Maskable Interrupts	No	No	Yes	Yes (one NMI)
Capable of Disabling Interrupts for a Specific Number of TCY	No	No	Yes	No

Note 1: A high-priority interrupt can interrupt a low-priority interrupt.
2: A hard fault is an exception that occurs because of an error during normal or exception processing.

Unique PIC24F Interrupt Features

- **User-Assignable Priority:** Users can also give each interrupt one of eight levels of priority, which can be used to override the natural priority
- **Software-Assigned Core Priority:** Users can also set a threshold priority level at which the CPU will respond to interrupts
- **Interrupt Nesting:** The use of natural priority and user-assigned priority allows multiple interrupt events to be nested; this feature can also be selectively disabled
- **Hard and Soft Traps:** Up to eight non-maskable hard traps with high natural priority are provided to flag potentially serious events, such as math (divide-by-0), stack overflow/underflow, address or data alignment and oscillator failure
- **Priority Exit from Power-Saving Modes:** Allows the application to either resume normal code execution or jump to an ISR, depending on the Interrupt Priority Level

Note: For further information on traps, refer to the specific device data sheet.

Unsupported PIC18F Features

All interrupt features on PIC18F devices without DMA are supported in the PIC24F interrupt controller. PIC18F devices with DMA functionality have a relocatable Interrupt Vector Table base address that allows for more control of the Interrupt Vector Table location than the PIC24F interrupt controller, which only has two options for the Interrupt Vector Table addresses.

Non-Maskable Traps

In PIC24F architecture, there are four hardware trap events with interrupts that can never be disabled:

- Address Decode Error
- Oscillator Failure
- Stack Error
- Math (Overflow) Error

These errors always force an immediate jump to specific interrupt vectors. The two most serious errors (Address Decode and Oscillator Failure) are hard traps; these must be cleared before the CPU execution can continue. All traps have their own individual flag bit. In addition to these unmaskable events, the PIC24F architecture can be expanded at a future time to include up to four additional traps. PIC18F architecture does not have an equivalent to the hardware trap. PIC18F stack error events are treated as Resets.

Unique SAMD2x Interrupt Features

1. Software can set the priority of each interrupt. The NVIC and the Cortex-M0+ processor core are closely coupled, providing low latency interrupt processing. To reduce interrupt latency and jitter, the Cortex-M0+ processor implements both interrupt late-arrival and interrupt tail-chaining mechanisms, as defined by the ARMv6-M architecture. The worst-case interrupt latency, for the highest priority active interrupt in a zero-wait state system not using jitter suppression, is 15 cycles.
2. Up to 32 external interrupt inputs, each with four levels of priority.
3. Each of the 29 interrupt lines is connected to one peripheral instance.
4. Dedicated Non-Maskable Interrupt (NMI) input.
5. Support for both level-sensitive and pulse-sensitive interrupt lines.
6. Relocation of the vector table.

Bit Name Changes and Mapping

PIC24F devices maintain the same general nomenclature for interrupt bit names as PIC18F devices, with two important differences. Both families maintain interrupt enable, flag and priority bits that are generically named xxxIE, xxxIF and xxxIP (where 'xxx' is the mnemonic for the interrupt source). The first major difference is the presence of three interrupt priority bits for each source, instead of the one used for PIC18F devices. These bits, generically named xxxIP2 through xxxIP0, allow the interrupt to be assigned to one of eight relative priority levels. The other difference is the number of interrupt sources. While many interrupts have the same (or very similar) name as PIC18F devices, others are new. Other interrupts have similar names but have a different meaning from their PIC18F counterparts. Users should refer to the appropriate PIC24F device data sheet for a complete list of interrupts and their meanings.

Setup and Enabling Interrupts

The following are the required steps to set up and enable interrupts on PIC18F devices:

1. Clear the interrupt flag status bit associated with the peripheral in the associated PIRx or INTCONx register.
2. Enable the interrupt source by setting the interrupt enable control bit associated with the source in the appropriate PIEx or INTCONx register.

Note:	The interrupt flag still needs to be cleared prior to exiting an ISR.

Optional steps:

1. Select the user-assigned priority level for the interrupt source by writing to the control bits in the RCON register. Select high priority or low priority using the priority bit in the corresponding IPRx register. The interrupt priority feature is enabled by setting the IPEN bit (RCON[7]).
2. (On newer PIC18F devices) Enable or disable the Interrupt Vector Table using the MVECEN Configuration bit and configure the IVTBASE register for the location of the Interrupt Vector Table.

The following are the required steps to set up and enable interrupts on PIC24F devices:

1. Set the NSTDIS bit (INTCON1[15]) if nested interrupts are not desired.
2. Clear the interrupt flag status bit associated with the peripheral in the associated IFSx register.
3. Enable the interrupt source by setting the interrupt enable control bit associated with the source in the appropriate IECx register.

Note:	The Interrupt/trap flag still needs to be cleared prior to exiting an ISR.

The following steps are required to set up and enable interrupts on the SAMD2x devices:

1. Interrupts must be globally enabled for interrupt requests to be generated. They must be enabled in the NVIC interrupt enable register (SETENA bits in ISER).
2. The NVIC Interrupt Priority registers IPR0-IPR7

provide a priority field for each interrupt which has four levels of priority.

3. Each peripheral can have one or more interrupt flags, located in the peripherals Interrupt Flag Status and Clear (INTFLAG) register. The Interrupt flag is set when the Interrupt condition occurs. Each interrupt in the peripheral can be individually enabled by writing a one to the corresponding bit in the peripherals Interrupt Enable Set (INTENSET) register.

Note: The interrupt request remains active until either the interrupt flag is cleared, the interrupt is disabled, or the peripheral is reset. Before enabling the interrupt, it is recommended to clear the interrupt flags.

Optional step:

Select the user-assigned priority level for the interrupt source by writing the control bits in the appropriate IPCx register. The priority level will depend on the specific application and type of interrupt source. If multiple priority levels are not desired, the IPCx register control bit for all enabled interrupt sources may be programmed to the same non-zero value.

Note: Upon Reset, all interrupts are assigned a default priority level of 4.

Disabling User Interrupts

To disable interrupts on PIC18F devices, it is only necessary to clear the GIE bit (GIEH or GIEL if priority levels are used).

The SAMD2x interrupts can be disabled by writing a one to the corresponding bit in the peripherals Interrupt Enable Clear (INTENCLR) register. Interrupts can be globally disabled in the NVIC interrupt enable register (CLRENA bits in ICER).

To disable user interrupts on PIC24F devices, these steps are required:

1. Push the current STATUS Register (SR) value onto the software stack using the PUSH instruction.
2. Force the CPU to Priority Level 7 by inclusive ORing the value, 0Eh, with the low byte of the STATUS Register. To enable user interrupts, the POP instruction may be used to restore the previous STATUS Register value.

Note: The DISI instruction allows interrupts of Priority Levels 1-6 to be disabled for a fixed period of time.

Migration Considerations

PIC18F architecture only has the ability to assign either high or low-priority interrupts to individual sources. PIC24F architecture allows the assignment of multiple priority levels for interrupts (Priorities 0 through 7 are user-defined and Priorities 8 through 15 are hardware-defined). At the very least, interrupts in native PIC18F applications will need to be reassessed and their priority levels redefined in PIC24F terms.

Note: The Interrupt/trap flag still needs to be cleared prior to exiting an ISR.

For both PIC18F and PIC24F devices, the RETFIE instruction exits an Interrupt Service Routine (ISR), but this instruction does behave slightly different depending on the microcontroller. For PIC18F, this instruction will set the GIE bit to re-enable global interrupts. Since the GIE bit does not exist for PIC24F, this instruction will restore the previous priority level.

The SAMD2x architecture can assign four levels of priority which can be user configurable, the highest being zero. There are few system and core level interrupts with default priorities which cannot be changed. The user must use the NVIC to activate the interrupts. Interrupts must be globally enabled first using the ISER register.

SERIAL PERIPHERAL INTERFACE (SPI)

The PIC24F SPI peripheral is a superset of the PIC18F architecture and many of the features are similar. PIC18F devices with DMA have many more features closer to the PIC24F SPI features.

The PIC24F SPI peripheral is considered a “stand-alone” peripheral, where PIC18F devices incorporate the SPI function into the larger Master Synchronous Serial Port (MSSP) peripheral, which also includes I^2C. But PIC18F devices with DMA have a similar stand-alone SPI module as in the PIC24F family.The SAMD2x SPI is part of the serial communication interface (SERCOM) peripheral. The SERCOM can be configured in one of several supported modes: I^2C, SPI or USART. When an instance of a SERCOM peripheral is configured and enabled, all the resources of that SERCOM instance will be dedicated to the selected mode.

The differences between the SPI peripherals of the PIC18F, PIC24F and SAMD2x devices are provided in Table 5.

TABLE 5: SPI FEATURE COMPARISON

Features	PIC18F		PIC24F	SAMD2x
	With MSSP	With Stand-Alone SPI		
Master and Slave modes	Yes	Yes	Yes	Yes
Clock Polarity and Edge Select	Yes	Yes	Yes	Yes
FIFO	No	Yes	Yes	Up to 16-bytes internal FIFO
Separate Transmit and Receive Buffer	No	Yes	Yes (Enhanced mode)	One-level transmit buffer, two-level receive buffer
Dedicated Baud Rate Counter	No	Yes	Yes	Uses SERCOM baud rate generator
Operation with DMA	No	Yes	Yes(2)	Yes
Transfer Data Width	8	1 to 8-bit	8/16	8/9
Frame Mode Support	No	No	Yes	Yes
Peripheral Pin Select (PPS)	No	Yes	Yes(1)	Yes
I^2S	No	No	Yes(2)	No

Note 1: Not all devices have PPS, refer to the device-specific data sheet to check for the PPS feature availability.
2: I^2S is available only on PIC24F variants, such as PIC24FJ128GA310, PIC24FJ128GB204, PIC24FJ256GB410/412 and PIC24FJ1024GA/GB610. Refer to the specific device data sheet for feature availability.

Migration Considerations

The only significant issue when migrating is the Master mode clock frequency calculation. Because the PIC24F instruction clock is based on FOSC/2, the peripheral clock is at a different rate than the PIC18F architecture. Use the equations provided in the **“Serial Peripheral Interface (SPI)”** chapter of the specific device data sheet to calculate the correct SPI clock speed.

SAMD2x:

The SERCOM bus clock (CLK_SERCOMx_APB) can be enabled and disabled in the Power Manager.

A generic clock (GCLK_SERCOMx_CORE) is required to clock the SPI. This clock must be configured and enabled in the Generic Clock Controller before using the SPI. This generic clock is asynchronous to the bus clock. Therefore, writes to certain registers will require synchronization to the clock domains, therefore some registers need to be synchronized when written or read. (Write-synchronization is denoted by the "Write-Synchronized" property in the register description.)

To use the DMA and Interrupts with the SPI, the DMAC and NVIC should be configured.

Differences Between PIC18F Devices without DMA and PIC18F Devices with DMA

Similar to the PIC24F devices, PIC18F devices with DMA have distinct SPI and I^2C modules, instead of a shared MSSP module. This SPI also has several features, such as FIFOs and separate transmit/receive buffers, that make migration from the PIC18F devices with DMA to PIC24F devices even more straightforward.

INTER-INTEGRATED CIRCUIT (I^2C)

Both PIC18F and PIC24F architectures support 7 and 10-Bit Addressing modes, General Call Addressing, clock stretching, 100 and 400 kHz data rates and multi-master networking.

The SAMD2x I^2C is part of the serial communication interface (SERCOM) peripheral which supports 7 and 10-Bit Addressing,100 kHz, 400 kHz, 1 MHz and 3.4 MHz data rates.

Table 6 shows comparisons of the features available in PIC24F and PIC18F and SAMD2x devices.

TABLE 6: I^2C FEATURE COMPARISON

Features	PIC18F		PIC24F	SAMD2x
	with MSSP	with Stand-Alone I^2C		
Supported Bus Speeds	100 kHz/400 kHz	100 kHz/400 kHz/ 1 MHz	100 kHz/400 kHz/1 MHz	100 kHz/400 kHz/1 MHz/3.4 MHz
10-Bit Addressing Mode	No	Yes	Yes	Yes
Multi-Master Support	Yes	Yes	Yes	Yes
Configurable Address Masking	6 Bits	7 or 10 Bits	7 or 10 Bits	7 or 10 Bits
General Call Support	No	Yes	Yes	Yes
Clock Stretching Option	Yes	Yes	Yes	Yes
Operation with DMA	No	Yes	No	Yes
Slew Rate Control	Yes	Yes	Yes	Yes
I^2C/SMBus Input Levels	Yes	Yes	Yes	Yes
Reserved Address Support	Yes(1)	Yes	Yes	Yes
Bus Repeater Mode	No	No	Yes	No
Firmware Mode	Yes	No	No(2)	No

Note 1: Refer to the specific device data sheet for information on which addresses are reserved for particular devices.

2: The PIC24F I^2C peripheral does not have a Firmware Controlled Master mode configuration (similar to the PIC18F mode, where SSPM[3:0] = 1011). As a result, PIC24F I^2C firmware implementation must use port input (V_{IH} and V_{IL}) levels.

Migration Considerations

The difference between the PIC24F and PIC18F I^2C peripherals can lead to complications during migration. A common issue is to not account for the address shift in the I2CxMSK and I2CxADD registers.

The Least Significant I^2C address bit in the PIC18F SSPxADD register is bit '1', where in the PIC24F I2CxADD register, it is bit '0'. A simple shift prior to loading or after reading the address will resolve the difference.

SAMD2x:

The SERCOM bus clock (CLK_SERCOMx_APB) can be enabled and disabled in the Power Manager. Two generic clocks are used by SERCOM are GCLK_SERCOMx_CORE and GCLK_SERCOM_SLOW.

The core clock (GCLK_SERCOMx_CORE) can clock the I^2C when working as a master. The slow clock (GCLK_SERCOM_SLOW) is required only for certain functions, such as, SMBus timing. These two clocks must be configured and enabled in the Generic Clock Controller (GCLK) before using the I^2C. The clocks write and read to the registers, which must be synchronized.

Differences Between PIC18F Devices without DMA and PIC18F Devices with DMA

Similar to the PIC24F devices, the PIC18F devices with DMA have distinct SPI and I^2C modules, instead of a shared MSSP module. This I^2C also has several features, such as 10-bit Addressing and general call support, that make migration from PIC18F devices with DMA to PIC24F devices even more straightforward. The stand-alone PIC18F I^2C module also has SMBus 3.0 input level support.

DIRECT MEMORY ACCESS (DMA)

PIC24F devices, as well as some of the PIC18F devices, support the DMA feature. The Direct Memory Access (DMA) module is designed to service data transfers between different memory regions directly, without intervention from the CPU. By eliminating the need for CPU-intensive management of handling interrupts intended for data transfers, the CPU can now spend more time on other tasks.

The SAMD2x device contains both a DMA and a CRC engine referred to as the DMAC. The DMAC can transfer data between memories and peripherals and therefore off-load these tasks from the CPU. It enables high data transfer rates with minimum CPU intervention and reduces CPU load.

The differences between the DMA of PIC18F, PIC24F, and SAMD2x devices are presented in Table 7.

TABLE 7: DMA FEATURE COMPARISON

Features	PIC18F		PIC24F[1]	SAMD2x
	PIC18F without DMA	PIC18F with DMA		
DMA	No	Yes	Yes	Yes
Multiple DMA Channel Support	No	Yes	Yes	Yes
Transfer mode (data memory to SFR/SFR to data memory)	No	Yes	Yes	Yes
Data Read from EEPROM/Flash	No	Yes	No	No
Addressable Source and Destination	No	Yes	Yes	Yes
Start Using Software Trigger	No	Yes	Yes	Yes
Start Using Interrupt Trigger	No	Yes	Yes	Yes
Source Address Increment/Decrement Mode	No	Yes	Yes	Yes
Destination Address Increment/Decrement Mode	No	Yes	Yes	Yes
Separate Counter for Source and Destination	No	Yes	No	No
DMA Abort Interrupt Trigger	No	Yes	No	No

Note 1: DMA is available only on PIC24F variants, such as PIC24FJ128GA310, PIC24FJ128GB204, PIC24FJ256GB410/412 and PIC24FJ1024GA/GB610. Refer to the specific device data sheet for availability of the features.

Migration Considerations

There are some differences in the features of the DMA, as well as the mode of operation, between the PIC18F and PIC24F families. some of the major differences are explained below:

1. One of the major differences in the DMA between the PIC18F and PIC24F families is the ability for a PIC18F device to access the Flash program memory and the data EEPROM memory for read operation. In PIC24F devices, the data can only be transferred between SFRs and data RAM or vice versa. In PIC18F devices, the SMT[1:0] (DMAxSSA) bits can be used to point to where the source data can be read from. SMTx bits can point to the data read from SFRs/GPRs, EEPROM or program Flash.
2. The SAMD2x supports four transfers, such as peripheral-to-peripheral, peripheral-to-memory, memory-to-peripheral, and memory-to-memory. The basic transfer unit is a beat, which is defined as a single bus access. There can be multiple beats in a single block transfer and multiple block transfers in a DMA transaction. The DMA transfer is based on descriptors, which hold transfer properties, such as the source and destination addresses, transfer counter, and other additional transfer control information. The descriptors can be static or linked. When static, a single block transfer is performed. When linked, several transfer descriptors can be used to enable multiple block transfers within a single DMA transaction.
3. Another difference is the count or the size of the data to be communicated. In PIC24F devices, there is only one count or size register, whereas in PIC18F devices, there is a size register for both destination (DMAxDSZ) and source (DMAxSSZ) registers. In SAMD2x devices there is only one count register.

Differences Between PIC18F Devices without DMA and PIC18F Devices with DMA

The DMA is one of the defining features of newer PIC18F devices.

LIQUID CRYSTAL DISPLAY

The devices and some of the PIC18F devices support the Liquid Crystal Display (LCD) module. Table 8 provides the features, operations, and comparisons of the LCD features between the PIC18F and PIC24F devices. The LCD functionality on the devices is very similar and it is easy to migrate from a PIC18F device to a PIC24F device.

Note: Liquid crystal display module is not supported on the SAMD2x devices.

TABLE 8: LCD FEATURE COMPARISON

Features	PIC18F(1)	PIC24F(1)
LCD	Yes	Yes
LCD Operation in Sleep	Yes	Yes
Static, 1/2 and 1/3 Bias	Yes	Yes
4 COM and 8 COM Multiplexing(2)	Yes	Yes
Charge Pump Biasing(3)	Yes	Yes
External Resistor Biasing	Yes	Yes
Internal Resistor Ladder Biasing(4)	Yes	Yes
Type A and Type B Support	Yes	Yes
LCD Prescaler Option	Yes	Yes
Multiple Option for LCD Clock	Yes	Yes

Note 1: Not all devices support LCD. Check the specific device data sheet to make sure the LCD is supported.

2: Multiplexing of 8 COM is not supported on all LCD devices. Make sure to check the specific device data sheet to see if 8 COM is supported.

3: The charge pump is supported for LCD operation when the V_{DD} is going below the LCD glass specification. Not all devices support this feature. Refer to the device data sheet to check the availability of the specific features supported.

4: An internal resistor is provided to generate the bias voltage needed for the LCD module internally; this is to save board space and cost. There is dynamic resistor switching implemented based on the user need to keep the current consumption low. Verify with the device data sheet for more details; all the LCD devices may not have the feature implemented.

Migration Considerations

The features and mode of operation of the LCD is very similar in the PIC18F and PIC24F devices. The only care that needs to be taken is if the system clock is used as the LCD clock. Depending on the specific device clock, the prescaler clock for the LCD should be corrected, thus the LCD is within an acceptable range of operation.

Differences Between PIC18F Devices without DMA and PIC18F Devices with DMA

There is no current PIC18F device with DMA that supports the LCD peripheral.

UNIVERSAL ASYNCHRONOUS RECEIVER TRANSMITTER

The PIC24F devices and some of the PIC18F devices support the Universal Asynchronous Receiver Transmitter (UART) module.

The SAMD2x USART is a part of serial communication interface (SERCOM) peripheral. SERCOM can be configured in any one of the supported modes: I^2C, SPI, and USART. When an instance of SERCOM is configured and enabled, all the resources of that SERCOM instance will be dedicated to the selected mode. Table 9 shows the comparison of the UART features between the PIC18F, PIC24F, and SAMD2x devices.

TABLE 9: UART FEATURE COMPARISON

Features	PIC18F(1)		PIC24F(1)	SAMD2x
	PIC18F without DMA	PIC18F with DMA		
Asynchronous (full-duplex) operation with: • Auto wake-up on Character Reception • Auto-Baud Calibration • 12-bit Break Character Transmission	Yes	Yes	Yes	Supports Full duplex operation
Full-Duplex 8-bit or 9-bit Data Transmission through the TX and RX pins	Yes	Yes	Yes	Supports 5,6,7,8 or 9-bit Data Transmission
Support for 9-bit mode with Address Detect (9th bit = 1)	Yes	Yes	Yes	No
Hardware Flow Control Option with $\overline{\text{UxCTS}}$ and $\overline{\text{UxRTS}}$ Pins	No	Yes	Yes	Yes
Number of Stop bits	1	1, 1.5, 2	1, 2	1 or 2
Selectable Idle Polarity	No	Yes	Yes	No
Baud Rate Generator	Dedicated 8-bit/ 16-bit	Dedicated 8-Bit/ 16-bit	16-bit	16-bit/8-bit
BRG Prescaler	Yes	Yes	Yes	No
IrDA® Encoder and Decoder Logic	No	No	Yes	Yes
16x Baud Clock Output for IrDA Support	No	No	Yes	Yes
FIFO Transmit Data Buffer	No	Yes	Yes	Yes
FIFO Receive Data Buffer	No	Yes	Yes	Yes
Loopback Mode for Diagnostic Support	No	No	Yes	Yes
Hardware Parity Support (8-bit data)	No	No	Yes	Yes
Parity Error Detection	No	Yes	Yes	Yes
Hardware Sync Byte Generation	Yes	Yes	Yes	No
Support for Sync and Break Characters	Yes	Yes	Yes	Yes
Wake-up Enable	Yes	Yes	Yes	Yes
Framing and Buffer Overrun Error Detection	Yes	Yes	Yes	Yes
Interrupt Options	Transmit and Receive	Transmit, Receive and UART Error Event	Transmit, Receive and UART Error Event	Transmit, Receive and UART Error Event
DMX	No	Yes	Yes	No
DALI	No	Yes	Yes	No
LIN	No	Yes	Yes	No

Note 1: Not all devices may include these features. Refer to the device data sheet to check the availability of the specific features supported.

Note: The PIC24F UART does not support synchronous communications. If synchronous serial communication is required, use the SPI module instead.

Migration Considerations

When migrating from a PIC18F design to a PIC24F, the user must consider the following:

1. Because the fundamental instruction cycle rate is different (FOSC/2 for PIC24F, FOSC/4 for PIC18F), projects that are being ported from PIC18F to PIC24F will need to have baud rates recalculated.
2. SAMD2x supports both asynchronous and synchronous mode. Baud rate calculation should be considered while using the USART.
3. Routines for 9-bit communication will need to be modified. PIC18F USARTs require the 9th bit to be read from, or written to, another register.

Differences Between PIC18F Devices without DMA and PIC18F Devices with DMA

The PIC18F devices with DMA add hardware protocol support (DMX, DALI and LIN/J2602), as well as several other features that make migration to the PIC24F devices more straightforward. In addition, like the PIC24F UART, they do not support the Synchronous mode that older PIC18F devices do.

REAL-TIME CLOCK AND CALENDAR

The Real-Time Clock and Calender (RTCC) provides the user with a RTCC function that can be calibrated.

In the SAMD2x, the RTCC is referred to as the RTC (Real Time Counter). The RTC is a 32-bit counter with a 10-bit programmable prescaler that typically runs continuously to keep track of time. The RTC can wake up the device from sleep modes using the alarm/compare wake up, periodic wake up, or overflow wake up mechanisms.

Table 10 shows the key features and differences of the Real-Time Clock and Calendar (RTCC) between the PIC18F and PIC24F and SAMD2x devices.

TABLE 10: RTCC FEATURE COMPARISON

Features	PIC18F(1)	PIC24F(1)	SAMD2x
RTCC(1)	Yes	Yes	Supports 32-bit or 16-bit counter and calendar mode
Updates Time: Hours, Minutes and Seconds	Yes	Yes	Yes
24-Hour Format (military time)	Yes	Yes	12/24 hour
Calendar: Weekday, Date, Month and Year	Yes	Yes	Supports Day
Configurable Alarm	Yes	Yes	Yes
Year Range: 2000 to 2099	Yes	Yes	Year (A value counting the offset from a reference (defined in software))
Leap Year Correction	Yes	Yes	Yes
BCD Format for Compact Firmware	Yes	Yes	No
Low-Power Operation	Yes	Yes	Yes
User Calibration	Yes	Yes	No
External 50 Hz or 60 Hz External Input	No	Yes	Maximum 48 Mhz
User Calibration Effect in Seconds	Every 60 Seconds	Every 15 Seconds	No
Alarm Repeat	Yes, Up to 255 Times	Yes, Up to 255 Times	No
Alarm Mask	Yes	Yes	Yes
RTCC Power Control	No	Yes	Yes
Selectable Clock Source	Yes	Yes	Yes

Note 1: Not all PIC24F and PIC18F devices support the RTCC module. Refer to the specific device data sheet to check if the RTCC module is available. Some of the PIC18F devices with RTCC include the PIC18F46J11, PIC18F46J50,PIC18F87J94, PIC18F87J90, PIC18FX7J13 and PIC18F87J72 families. Some of the PIC24F devices with RTCC include the PIC24FJ128GA010, PIC24FJ128GA310, PIC24FJ128GB410, PIC24FJ128GB204, PIC24FJ256GA610, PIC24FJ64GA006, PIC24FJ32MC104 and PIC24FJ256GA705 families.

Migration Considerations

When migrating from a PIC18F design to a PIC24F, the user must consider the following:

1. The features for the RTCC module are very similar between the devices, but the PIC24F devices include some additional features. For the legacy RTCC attributes, there are no major differences. For the RTCC input clock options, refer to the specific device data sheet.
2. The SAMD2x supports a 12-hour format and does not support a weekday option.

Differences Between PIC18F Devices without DMA and PIC18F Devices with DMA

There is no current PIC18F device with DMA that supports the RTCC peripheral.

CYCLIC REDUNDANCY CHECK (CRC) GENERATOR

The PIC24F CRC module allows for hardware calculations of CRC checksums, instead of having to utilize software bandwidth to complete the same calculations. Legacy PIC18F devices do not have hardware CRC support, but PIC18F devices with DMA have a similar CRC module to the PIC24F devices.

In the SAMD2x, The Device Service Unit (DSU) provides support for calculating a cyclic redundancy check (CRC32) value for a memory area (including the NVM Flash and AHB RAM).

When the CRC32 command is issued from:

- The internal range, the CRC32 can be operated at any NVM memory location.
- The external range, the CRC32 operation is restricted depending on the mode configured in Access Mode (AMOD) bits in the Address register.

When configured as '0', the CRC32 is restricted to the full Flash array area (EEPROM emulation area not included) DATA is forced to 0xFFFFFFFF before calculation (no seed). When configured as '1', the CRC32 of the whole EEPROM emulation area DATA is forced to 0xFFFFFFFF before calculation (no seed).

The differences between the CRC modules are provided in Table 11.

TABLE 11: CRC FEATURE COMPARISON

Features	PIC18F		PIC24F	SAMD2x
	PIC18F without DMA	PIC18F with DMA		
Polynomial Size	N/A	Up to 16	Up to 16	Up to 32
Interrupt	N/A	Upon CRC Completion as well as Scanner Completion	On CRC Completion	No
NVM Scanner	N/A	Scans Program Memory or EEPROM and Feeds Data to CRC Engine	No	No
Input FIFO	N/A	No	8-Deep, 16-bit or 16-Deep, 8-bit	No

Migration Considerations

The primary consideration when migrating from PIC18F is that the PIC18F CRC module is primarily used with the NVM scanner to perform CRC checksums on program memory. The PIC24F CRC module does not contain a built-in scanner the way the PIC18F module does, so it will require the use of software or other modules to perform the same functionality. In addition, the PIC24F CRC module has a FIFO on its input instead of just a single set of registers, so inputting data to the module works slightly differently.

In the SAMD2x, the CRC32 calculation for a memory range is started after writing the start address into the Address register (ADDR), and the size of the memory range into the Length register (LENGTH). Both must be word aligned, this should be considered while migrating. The initial value used for the CRC32 calculation must be written to the Data register (DATA). This value is 0xFFFFFFFF, which is usually the CRC seed.

The calculated CRC32 value can be read out from the Data register. The read value must match standard CRC32 implementations.

Differences Between PIC18F Devices without DMA and PIC18F Devices with DMA

Only PIC18F devices with DMA support this module.

TIMERS

PIC24F timers broadly support the basic PIC18F timer features found in Timer0 and Timer1/3/5, including Asynchronous and Synchronous Counter modes, Timer and Gated Timer modes, and 32 kHz crystal support. PIC24F timers are designed to have more generic functions, whereas PIC18F timers are intended for dedicated purposes. This specialization has only increased with PIC18F devices with DMA, which include the new 8-bit Timer2/4/6 module with hardware limit functions and the signal measurement timer, a 32-bit timer meant for performing capture/compare and measuring functions on incoming digital signals, both of which have specific functions. Conversely, each PIC24F 16-bit timer has a dedicated period register, selectable prescaler and period match flag, and can operate in either Counter or Timer mode for generic purposes. Two 16-bit PIC24F timers can also be combined to make a single 32-bit timer.

The SAMD2x Timer/Counter (TC) consists of a counter, a prescaler, compare/capture channels and control logic. The counter can be set to count events, or to count clock pulses. The counter, together with the compare or capture channels, can be configured to timestamp input events, allowing capture of frequency and pulse width. It can perform waveform generation, such as frequency generation and pulse-width modulation (PWM).

The differences between the Timer module of PIC18, PIC24F, and SAMD2x devices are provided in Table 12.

TABLE 12: TIMERS FEATURE COMPARISON

Features	PIC18F		PIC24F	SAMD2x
	PIC18F without DMA	PIC18F with DMA		
Timer Width	8/16-bit	8/16/24-bit	16/32-bit	8/16/32-bit
General Purpose Timer Mode	All Timers	All Timers	All Timers	TC3 to TC7
Asynchronous Counter Mode	Timer1/3	All Timers	Timer1/2/4	Yes
Synchronous Counter Mode	Timer0/1/3	All Timers	All Timers	No
Period Register	Timer2/4	Timer0/2/4/6 and SMT	All Timers	TC3 to TC7
32 kHz Crystal Support	Timer1	All Timers	Timer1	Yes
Other Clock Sources	No	All Timers	No	Yes
Timer Gate Option	No	Timer1/3/5	All Timers	No
Prescaler	All Timers	All Timers	All Timers	TC3 to TC7
Postscaler	Timer2/4	Timer0/2/4/6	No	No
Special Event Trigger	Yes	Yes	Yes	Yes
System Clock Source Rate	FOSC/4	FOSC/4	FOSC/2	TC3 max. Freq – 96 MHz TC4 to TC7 Max. Freq – 48 MHz
Hardware Limit Features	No	Timer2/4/6	No	No
Signal Measurement Features (pulse width, time between edges)	No	SMT	No	Frequency generation Single-slope PWM

Migration Considerations

The biggest consideration of migration is that timer functionality may not be on the same timers between PIC18F and PIC24F devices. Period registers are on all PIC24F timers, rather than only some of the PIC18F timers. Prescalers are present on both architectures, but PIC18F prescalers differ by each timer, while PIC24F prescalers are the same for each timer. Finally, PIC24F timers do not have postscalers, a feature that is common on many PIC18F timers. Either a software solution or different prescaler/period option may be needed in order to achieve the same timer period on a PIC24F device.

The SAMD2x contains Timer/Counter capability in five timers (TC3 to TC7), all the functionalities specified in the features are supported in all the TC instances. The Timer can be configured as 8/16/32-bit. Unlike the PIC24F, the TC module consists of a Compare or capture module allowing capture of frequency and pulse width. It supports waveform generation and the DMA functionality can be used with timers and counters.

The Timer/Counter for Control (TCC) Applications is another module in the SAMD2x which exhibits a few more features, such as Dual-slope PWM, Pattern gen-

eration, low-side and high-side output with programmable dead-time insertion and so on, which are suitable for motor applications.

Differences Between PIC18F Devices without DMA and PIC18F Devices with DMA

The PIC18F devices with DMA have many more timer features than the legacy variants, which make them match up better with PIC24F devices and make migration easier. Both Asynchronous and Synchronous modes are now available on all timers, along with 32 kHz crystal support. More timers have period registers, and Timer1, 3 and 5 offer gated timer functionality. These features mean that migrating generic timer code from PIC18F devices with DMA to PIC24F devices has even fewer considerations, as most features are shared between the two.

The newer PIC18F devices also have some new timers for more specific applications. The Timer2/4/6 module on PIC18F devices with DMA is an 8-bit timer with a period register, which can be started, run, frozen or reset by external signals (either from other peripherals or an external pin). The module also has One-Shot and Monostable modes. These timers can be used with the PWM to perform more sophisticated waveform control, such as pulse density modulation. There are no equivalent timers on the PIC24F devices.

PIC18F devices with DMA also have the SMT, a 24-bit timer intended for measuring a variety of digital signal parameters, such as pulse width, frequency and duty cycle, as well as use as a synchronous timer or asynchronous counter. It also has gated timer features and a period match register. There is no equivalent timer on the PIC24F devices, although the 32-bit timers on the PIC24F can perform most of the non-signal measurement functions of the SMT, for example, if the SMT is only being used as a large timer.

CONFIGURABLE LOGIC CELL (CLC)

The PIC24F Configurable Logic Cell (CLC) module allows the user to specify combinations of signals as inputs to a logic function and to use the logic output to control other peripherals or I/O pins. The legacy PIC18F devices have no equivalent feature, but the PIC18F devices with DMA also have a CLC module. The CLC modules between the PIC18F devices with DMA and the PIC24F devices are almost identical. Table 13 provides the differences in the CLC modules.

Note: Configurable Logic Cell module is not supported on the SAMD2x devices.

TABLE 13: CLC FEATURE COMPARISON

Features	PIC18F		PIC24F
	PIC18F without DMA	PIC18F with DMA	
Number of Input Selections (total)	0	Up to 64	Up to 32
Number of Input Selections (per data gate)	0	Up to 64	Up to 8
Logic Output to other Peripherals	N/A	Yes	Yes
CLC Output Pin	N/A	Relocatable with PPS	Fixed Pin
Interrupt	N/A	Rising and Falling Edges	Rising and Falling Edges
Output Enable	N/A	Controlled through PPS	Separate Control Bit

Migration Considerations

The only considerations when migrating from PIC18F CLCs to PIC24F CLCs is with the inputs and outputs. The PIC24F CLCs are more limited in their CLC inputs. The PIC18F CLC modules allow for up to 64 inputs and allow those inputs to go to all four of the data gates, while the PIC24F devices have only 32 inputs, of which only eight go to each data gate. In addition, both the input and output pins for the PIC18F CLC can be moved through PPS, while the CLC pins on PIC24F devices are static. Finally, due to the output pins' static nature, the PIC24F CLC has a separate output enable pin that needs to be considered when outputting the CLC to said external pin.

Differences Between PIC18F Devices without DMA and PIC18F Devices with DMA

Only PIC18F devices with DMA support this module.

CAPTURE/COMPARE/PWM

The PIC24F capture and compare modules exhibit the same features as the PIC18F Capture/Compare/PWM (CCP) and ECCP peripherals. The differences between the CCP peripherals of PIC18F and PIC24F devices are provided in Table 14.

Note: The SAMD2x exhibits these features in the Timer/Counter (TC) and Timer/Counter for Control (TCC) Applications, for additional information, refer to the **"Timers"**.

TABLE 14: CCP/ECCP FEATURE COMPARISON

Features	PIC18F(1)	PIC24F(1)	SAMD2x
CCP/ECCP Features	Yes	Yes	Yes
Configurable Timer Sources	Yes	Yes	Yes
Capture Pin Prescaler	1, 4, 16	1, 4, 16	No
Capture Buffer	Yes	Yes	Yes
Capture Timer Width	Yes	Yes	Yes
Selectable Captures per Interrupt	Yes	Yes	No
Selectable Output Compare Pin States	Yes	Yes	Yes
Special Event Trigger	Yes	Yes	Yes
Number of PWM Outputs per Peripheral	Yes	Yes	Yes
Half-Bridge/Full-Bridge PWM Support	Yes	Yes	Yes
PWM Dead-Band Support	No(2)	Yes	Yes

Note 1: Refer to the device data sheet to check the availability of the specific features supported.
2: Devices with CWG (Configurable Waveform Generator) and COG (Configurable Output Generator) offer dead-band support. Check the device data sheet to see if the feature is supported.

The PIC24F input capture and output compare modules can use either Timer2 or Timer3, where the PIC18F modules can use either Timer1 or Timer3. Capture events can be generated on every rising, falling, 4th rising and 16th rising edge of the ICx pin.

With Single Compare Match mode selected, both architectures can select the initial state of the OCx pin. Upon the match, the pin can either transition or toggle. For each mode and in both architectures, the output compare interrupt flag is set.

In the SAMD2x, the TC3 to TC7(Timer/Counter) can be configured in compare/capture mode. In compare operations, the counter value is continuously compared to the values in the CCx (compare/capture register). In case of a match the TC can request DMA transactions, generate interrupts or events for the Event System. In waveform generator mode, these comparisons are used to set the waveform period or pulse width.

A Capture operation can be enabled to perform input signal period and pulse width measurements, or to capture selectable edges from an internal event from the Event System.

All of the PIC18F PWM modes are supported by the PIC24F family. The significant difference is that each output compare peripheral can generate only one output. Therefore, half-bridge support requires two peripherals and full-bridge support requires four.

PIC24F PWM mode is an extension of the output compare peripheral. This mode is similar to the Single Output Compare mode and with the addition of Fault protection pins, OCFA and OCFB, can stop the pulse train; similar to the PIC18F PWM mode.

Some of the PIC24F devices have dedicated modules, called MCCP and SCCP, which stands for the Multiple or Single Capture/Compare peripheral. The devices that include these modules have multiple modes of operation, where they can work as a timer, capture, compare, as well as a PWM option. There are multiple input clock features for these devices. Please refer to the device data sheet to check the availability of the MCCP or SCCP modules.

On the SAMD2x, for a single-slope PWM generation, the period time (T) is controlled by the TOP value, and the CCx (compare/capture register) controls the duty cycle of the generated waveform output. For dual-slope PWM generation, the period setting (TOP) is controlled by PER, while the CCx controls the duty cycle of the generated waveform output. The counter repeatedly counts from ZERO to PER, and then from PER to ZERO.

Migration Considerations

The PIC24F output compare peripheral clock source is based on FOSC/2 which differs from the PIC18F FOSC/4 clock source. Ensure the equations available in the product data sheet are used for the various clock source calculations.

In the SAMD2x, The generic and bus clocks should be enabled to operate the TC and TCC module. TCC0 and TCC1 share a peripheral clock generator. The TC instances are paired (even and odd) starting from TC3 and use the same generic clock.

Differences Between PIC18F Devices without DMA and PIC18F Devices with DMA

The primary difference in the CCP module between legacy PIC18F variants and PIC18F devices with DMA is not directly related to the CCP, but instead, to the timers. Both the Timer1 and Timer2 have differences in them from legacy variants that may affect how the CCP operates, which should be taken into consideration. PIC18F devices with DMA also have the Complimentary Waveform Generator (CWG) module which supports PWM with dead band.

I/O PORTS

PIC24F I/O ports are very similar to the PIC18F ports, but have noteworthy differences. Both families of devices have data PORT, LAT and TRIS registers. Both device families have analog and digital peripherals.

The I/O pin controller of the SAMD2x controls the I/O pins. The I/O pins are organized in a series of groups, collectively referred to as a PORT group. Each PORT group can have up to 32 pins that can be configured and controlled individually or as a group.

The differences between the I/O ports of PIC18F, PIC24F, and SAMD2x devices are provided in Table 15.

TABLE 15: I/O PORTS FEATURE COMPARISON

Features	PIC18F(1)		PIC24F(1)	SAMD2x
	PIC18F without DMA	PIC18F with DMA		
Control Registers: PORTx, LATx and TRISx	Yes	Yes	Yes	DIR, OUT, IN, PULLEN, INEN
Internal Pull-up	Only on PORTB	On All Ports	On All Ports	On All Ports
Configured to Inputs on Reset	Yes	Yes	Yes	Yes
Open-Drain Control	No	Yes	Yes	No
PPS/Multiplexing	Yes(1)	Yes	Yes	Yes
Interrupt-on-Change	Selective Pins	Yes	Yes	EIC(2)

Note 1: Not all devices will have this feature. Refer to the device data sheet to check the availability of the specific features supported.
2: The External Interrupt Controller (EIC) allows the external pins to be configured as interrupt lines. Each interrupt line can be individually masked and can generate an interrupt on rising, falling, or both edges, and on high or low levels.

Unsupported PIC18F Features

The PIC24F port architecture does not permit the port output to drive the peripheral input. The user must either configure the pin as a peripheral input or port output, but not both.

Migration Considerations

- Enabling a digital or analog input or output onto a pin with a configurable open-drain option will not cause the pull-up to be automatically disabled. The pull-up is not disabled if the pin has a configurable open-drain option. It is important to disable the pull-up in software when it is not needed.
- Pins without an analog function can tolerate input voltages up to 5.5V. This can minimize hardware changes when migrating from a PIC18F device. A higher voltage output can be created by adding an external pull-up resistor on the pin and writing a zero to the data latch. Setting the TRISx bit will pull the output up to the supply voltage and clearing the TRISx bit will output a digital zero.
- Drive strength, slew rate and input voltage thresholds can change automatically when a peripheral is enabled. It is important to review the specific data sheets for differences between devices.
- Most of the input buffers for PIC24F devices are Schmitt Triggers (ST). Verify that the output levels of associated components meet the ST input voltage thresholds.
- Making the pins analog or digital can vary from device to device. Some of the PIC18F devices have this control in the ADC registers. Some of the PIC24F devices have a register, called ADxPCFG, to implement the same feature. Some of the PIC18F and PIC24F devices have dedicated registers for each pad to make the pins analog or digital (ANSELx register).
- On SAMD2x, each pin may either be used for general-purpose I/O under direct application control or be assigned to an embedded device peripheral. When used for general purpose I/O, each pin can be configured as input or output, with highly configurable driver and pull settings.
- The I/O pins are assembled in pin groups with up to 32 pins. Group 0 consists of the PA pins, and group 1 is for the PB pins, and so on. Each pin group has its own PORT registers, with a 0x80 address spacing. For example, the register address offset for the Data Direction (DIR) register for group 0 (PA00 to PA31) is0x00, and the register address offset for the DIR register for group 1 (PB00 to PB31) is 0x80. All pin functionality should be accessed using this groups.

- The PMUXx register helps for selecting the embedded device peripheral functionality.

Differences Between PIC18F Devices without DMA and PIC18F Devices with DMA

There are few to no differences between PIC18F devices with DMA and PIC18F devices without DMA in respect to I/O port controls.

OSCILLATOR

The PIC24F oscillator system supports many of the features of the PIC18F and adds several new features. Both architectures support three major clock sources: primary oscillators, internal RC oscillators and 4x PLL frequency multipliers. In addition, both also support features to enhance application robustness, such as software-controlled clock switching, Fail-Safe Clock Monitors (FSCM) and Two-Speed Start-up. PIC24F devices increase the flexibility of initial clock configuration, software-controlled clock switching and the use of the PLL.

The SAMD2x supports external high frequency and 32 kHz Oscillators, Internal 8 MHz, 32 kHz RC Oscillators, and an Internal 48 MHz Digital Frequency Locked Loop Oscillator.

The differences between the oscillator of PIC18, PIC24F, and SAMD2x devices are provided in Table 16.

TABLE 16: OSCILLATOR FEATURE COMPARISON

Features	PIC18F(1)		PIC24F(1)	SAMD2x
	PIC18F without DMA	PIC18F with DMA		
Primary (external) Oscillator modes	HS, XT, EC, LP and External RC(2)	HS, XT, LP and EC	HS, XT and EC (all devices)	XOSC, XOSC32K
Secondary (Timer1) Oscillator	Yes	Yes	Yes	No
8 MHz Internal RC Oscillator	Yes (INTOSC)	Yes (HFINTOSC)	Yes (FRC)	Yes
32 kHz Internal RC Oscillator	Yes (INTRC)	Yes (MFINTOSC/ LFINTOSC)	Yes (LPRC)	Yes, and also supports OSCULP32K (3)
4x PLL Options: • XTPLL (MSPLL) • ECPLL • INTOSCPLL/FRCPLL	 No Select Devices Only Select Devices Only	 No Yes No	 Yes Yes Yes	DFLL, FDPLL
Software Clock Switching	Between Clock Sources Only(1)	Yes	Yes	Yes
Doze Mode	No	Yes	Yes	No
Fail-Safe Clock Monitor	Yes(1)	Yes	Yes	No
Two-Speed Start-up	Yes(1)	Yes	Yes	Programmable start-up time

Note 1: Not all devices will have this feature. Refer to the device data sheet to check the availability of the specific features supported.
2: Not all PIC18F devices have an external RC oscillator, refer to the specific device data sheet.
3: OSCULP32K is referred as 32 kHz Ultra-Low Power Internal Oscillator.

Primary Oscillators (POSC)

In PIC18F devices, the exact oscillator mode to be used is selected during device configuration using the FOSC[3:0] Configuration bits. In some of the newer PIC18F devices, the POSC mode is selected by FEXTOSC[2:0] and the actual boot up oscillator is selected by RSTOSC[2:0]. In PIC24F devices, the Primary Oscillator mode is selected during configuration with a combination of the FNOSC[2:0] and POSCMD[1:0] Configuration bits.

In the SAMD2x, the OSC8M is the default clock source that is used after a power-on reset (POR).The OSC8M is an internal oscillator operating in open-loop mode and generating an 8 MHz frequency. The OSC8M is factory-calibrated under typical voltage and temperature conditions. The OSC8M can be used as a source for the generic clock generators. To enable the OSC8M, the Oscillator Enable bit in the OSC8M Control register (OSC8M.ENABLE) must be written to one.

The user can control the oscillation frequency by writing to the Frequency Range (FRANGE) and Calibration (CALIB) bit groups in the 8 MHz RC Oscillator Control register (OSC8M). It is not recommended to update the FRANGE and CALIB bits when the OSC8M is enabled. As this is in Open-Loop mode, the frequency will be voltage, temperature, and process dependent.

Secondary Oscillator (SOSC)

All PIC18F devices have the option to use the Timer1 oscillator as a secondary clock source. The most typical arrangement for this option is to connect a low-

power, 32 kHz watch crystal across pins, T1OSI and T1OSO. The oscillator is controlled separately from the device clock by the T1OSCEN bit (T1CON[3]).

The PIC24F devices also provide a Secondary Oscillator that is identical in function to the Timer1 oscillator; it only differs in that it is controlled through the OSCCON register with the SOSCEN bit. The crystal input/output pins are renamed SOSCI and SOSCO.

In the SAMD2x, the 32 kHz Ultra-Low Power Internal Oscillator (OSCULP32K) is a form of second oscillator which runs by default after a POR reset. The OSCULP32K provides a tunable, low-speed and ultra-low power clock source. It has a 32.768 kHz output and a 1.024 kHz output that are always running. The frequency of the OSCULP32K oscillator is controlled by the value in the 32 kHz Ultra-Low Power Internal Oscillator Calibration bits (OSCULP32K.CALIB) in the 32 kHz Ultra-Low Power Internal Oscillator Control register. OSCULP32K.CALIB is automatically loaded from Flash Factory Calibration during startup and is used to compensate for process variation in the calibration value, which can be overridden by the user by writing to OSCULP32K.CALIB.

Internal RC Oscillators (INTOSC/FRC and INTRC/LPRC)

Both PIC24F and PIC18F families feature two independent internal oscillators, an efficient 31 kHz oscillator and an accurate, high-speed 8 MHz oscillator. Some of the newer devices have a selectable frequency, from 1 MHz to 64 MHz. Both architectures use a configurable postscaler, driven by the 8 MHz source, to provide a range of clock frequencies, from 31 kHz to 4 MHz (as well as the undivided 8 MHz output). Both architectures allow software selection from the 31 kHz or 8 MHz oscillators to provide the 31 kHz source for various system features.

PIC18F and PIC24F devices both support a 4x PLL frequency multiplier for use with select clock sources. In all cases, the PLL provides a stable output only when the input frequency is between 4 and 10 MHz. For a detailed description of the PLL operation, please refer to the device data sheet.

The SAMD2x supports Internal 8 MHz (OSC8M), 32 kHz RC Oscillators (OSC32K), and a 48 MHz Digital Frequency Locked Loop Oscillator (DFLL48M). The OSC8M has a fast startup, output frequency fine tuning feature, and a 4/2/1 MHz divider output frequency range. The OSC32K is a 32.768 kHz High Accuracy Internal Oscillator. The DFLL48M operates as a standalone high-frequency programmable oscillator in Open-Loop mode, and Operates as an accurate frequency multiplier against a known frequency in Closed-Loop mode providing 48 MHz output frequency.

The oscillators can be used as a source for the generic clock generators. A clock source selected as input to a generator can either be used directly, or it can be prescaled in the generator. The outputs from the generators are used as sources for the Generic Clock Multiplexers, which provide the Generic Clock (GCLK_PERIPHERAL) to the peripheral modules.

Two-Speed Start-up

Two-Speed Start-up is implemented identically in PIC18F and PIC24F devices. In both cases, the feature is controlled by the IESO Configuration bit. Some of the new PIC18F devices will not have the Two-Speed Start-up feature; please check the device data sheet for details.

The SAMD2x's Programmable start-up time options help the user in configuring the start-up time by referring to the electrical characteristics. Start-up time bits are present in respective clock configuration registers.

Fail-Safe Clock Monitor

The Fail-Safe Clock Monitor feature is also available for both the device families. It is controlled, along with run-time clock switching, by the Configuration Word bits. Implementation is very similar in both PIC18F and PIC24F devices, where the system clock automatically switches to the FRC when the primary oscillator stops.

Clock Switching

Clock switching differs significantly between PIC18F and PIC24F devices. Conceptually, both architectures have three categories of oscillators: primary (external components connected to OSC pins), secondary (external crystal connected to T1OSC or SOSC pins) and internal RC.

PIC18F devices permit the definition of one and only one primary oscillator type used during device configuration. This is the oscillator that is always used when on device power-up and Reset. Thereafter, the device can switch between primary, secondary and internal oscillator sources under software control. In the newer PIC18F family devices, the RSTOSC configures which oscillator is used at start-up and the FEXTOSC selects the oscillator type.

Once a start-up oscillator is defined, it cannot be changed unless the device is reprogrammed.

For PIC24F devices, any one of the three major clock sources can be configured as the default start-up oscillator; users are no longer confined to just the primary oscillator sources. During run time, the device can switch between any of the available oscillator modes under software control. This means that, among other things, it is possible to switch between a Primary Clock mode and its PLL. PIC24F devices unlock the high or low byte for one instruction after two specific literals are written to the high or low byte of OSCCON. Please refer to the compiler manual and device data sheet for the specifics of writing to OSCCON and clock switching.

For the SAMD2x devices, changing from one clock source, for example, A to another clock source B, can be done on the fly. If clock source B is not ready, the Generator will continue running with clock source A. As soon as clock source B is ready, however, the generic clock generator will switch to it. During the switching operation, the generator holds clock requests to clock sources A and B and then releases the clock source A request when the switch is done. Enabling the "ONDEMAND" feature of clock source A will ensure a proper transition from clock source A to clock source B.

Migration Considerations

When migrating to a PIC24F microcontroller (or any microcontroller, for that matter), any application that is based on a crystal clock source should be re-evaluated for oscillator operation and stability. It is important to verify that the crystal performance is reliable across the voltage, temperature and process variations anticipated for the application.

Differences Between PIC18F Devices without DMA and PIC18F Devices with DMA

Conceptually, there are few differences in oscillators between PIC18F devices with DMA and PIC18F devices without DMA; there are only a few minor setup/Configuration register changes.

POWER-SAVING FEATURES

PIC24F power-saving features are very similar to the power-saving modes offered in PIC18F XLP Technology devices. Both architectures include run-time switching of system clock sources, Idle and Sleep modes, and hardware invoked exits through Resets and interrupts. PIC24F devices describe these features in a somewhat different manner and support additional features for strategic reduction of power consumption.

The SAMD2x has similar power-saving features to a PIC24F, these features are part of the Power Manager (PM) module, The PM controls the reset, clock generation and sleep modes of the device.

Various sleep modes are provided in order to fit power consumption requirements. This enables the PM to stop unused modules to save power. In active mode, the CPU is executing application code. When the device enters a Sleep mode, program execution is stopped, some modules and clock domains are automatically switched off by the PM according to Sleep mode. The application code decides which Sleep mode to enter and when. Interrupts from enabled peripherals and all enabled reset sources can restore the device from a Sleep mode to Active mode.

Before entering the Stand-by Sleep mode, the user must make sure that a significant number of clocks and peripherals are disabled, thus the voltage regulator is not overloaded. This is due to the internal voltage regulator existing in Low-Power mode during Stand-by Sleep Mode.

Run-Time Clock Switching

PIC18F and PIC24F devices have all the same types of system clock sources (Primary, Secondary and Internal Oscillator). In addition, Sleep and Idle modes are defined in the same manner. The process of how the clock switching is achieved is different between PIC18F and PIC24F families; check the device data sheet for the steps to be followed for clock switching.

The differences between the power-saving features of the PIC18F, PIC24F, and SAMD2x devices are presented in Table 17.

The SAMD2x has two main sleep modes:

- Idle mode: The CPU is stopped. Optionally, some synchronous clock domains are stopped, depending on the IDLE argument. The Regulator operates in normal mode.
- Stand-by mode: All clock sources are stopped, except those where the RUNSTDBY bit is set. The regulator operates in Low-Power mode.

The Sleepwalking feature of the SAMD2x to temporarily wake-up clocks for the peripheral to perform a task without waking-up the CPU in Standby Sleep mode. At the end of the sleepwalking task, the device can either be awakened by an interrupt (from a peripheral involved in Sleepwalking), or enter Standby Sleep mode again.

TABLE 17: POWER-SAVING FEATURE COMPARISON

Features	PIC18F(1)		PIC24F(1)	SAMD2x
	PIC18F without DMA	PIC18F with DMA		
Run-Time Clock Switching	Yes	Yes	Yes	Yes
Idle mode	Yes	Yes	Yes	Yes
Selective Peripheral Idle	No	No	Yes	Yes
Sleep mode	Yes	Yes	Yes	Yes
Low-Voltage Sleep (Retention Sleep)	Yes(1)	Yes	Yes(1)	No
Deep Sleep	Yes(1)	No	Yes(1)	No
Doze Mode	No	Yes	Yes	No
PMD Option	No	Yes	Yes	Yes

Note 1: Not all devices will have this feature. Refer to the device data sheet to check the availability of the specific features supported.

RESETS

The PIC24F Reset system shares most of its features with the PIC18F Reset system. The same legacy Resets are supported in either identical or functionally equivalent methods:

- Power-on Reset (POR)
- Brown-out Reset (BOR)
- External Master Clear Reset ($\overline{\text{MCLR}}$)
- Software Reset (RESET instruction)
- Watchdog Timer (WDT) Reset
- Stack Error Reset (Overflow or Underflow)

The PIC24F devices have some additional Reset sources/states, along with some enhanced reporting. The Reset states for SFRs and start-up timing from Resets also differs slightly. In addition, PIC18F devices with DMA have Reset system enhancements that differ from the ones made in PIC24F.

The SAMD2x supports similar resets, and the reset sources are as follows:

- Power Reset sources: POR, BOD12, BOD33
- User Reset sources: External reset (RESET), Watchdog Timer Reset, software Reset

The Reset Status register can be used to read the reset source from the application code.

The differences between the PIC18, PIC24F, and SAMD2x devices are provided in Table 18.

TABLE 18: RESETS FEATURE COMPARISON

Features	PIC18F		PIC24F	SAMD2x
	PIC18F without DMA	PIC18F with DMA		
Legacy Reset Types	POR, BOR, $\overline{\text{MCLR}}$, RESET Instruction			POR, BOD12, BOD33, External reset (RESET)
Additional Reset Types	Configuration Word Mismatch (PIC18FXXJ Flash devices)	Memory Violation, Watchdog Timer Window Violation	Illegal Opcode/Uninitialized W, Configuration Word Mismatch, Trap Conflict	Watchdog Timer reset, software reset
BOR Configuration	Configurable, Software-Controllable in Many Devices	Configurable, Software-Controllable in Many Devices	Tied to On-Chip Regulator(1)	Tied to System Controller Interface((SYSCTRL)
Stack Underflow/Overflow Reset	Reset	Separate Resets	Unmaskable Trap	No
SFR Reset States	Dependent on Type of Reset	Dependent on Type of Reset	Uniform for All Reset Types	Uniform for All Reset Types
Start-up Timer	Configurable	Configurable	Tied to Regulator Configuration	No
Flag Bits Location	RCON/STKPTR	PCON0/1	RCON/INTCON1	RCAUSE

Note 1: Some of the devices include the feature to enable or disable BOR; refer to the device data sheet to check the availability of the BOR feature.

Migration Considerations

All legacy PIC18F Resets are also supported by the PIC24F devices (in addition to a few additional Reset sources). The primary migration concern is in how the PIC24F handles stack overflow/underflow cases. While these cases trigger a Reset on PIC18F devices, they are instead implemented as traps in the PIC24F architecture. In theory, this leads to more flexibility in handling stack overflow/underflow instances, but applications that expect a Reset on stack overflow will need to take this change into account. The SAMD2x stack is part of RAM memory, therefore the size is configurable providing flexibility. A secondary migration concern is that PIC24F devices do not have a configurable start-up timer, so the timer will need to be accounted for instead of programmed. The SAMD2x has Programmable start-up time options to help the user in configuring the start-up time. Refer to the electrical characteristics for more information. The third major

consideration is that the polling of Resets is different between PIC18F devices and PIC24F devices, with PIC24F Reset flags being active-high instead of PIC18F active-low bits, and the PIC24F Reset bits being more narrowly defined (on PIC18F devices, it is often necessary to read all of the Reset flags to determine the cause of the Reset, while on the PIC24F devices, often only one flag needs to be read). The Reset Status register (RCAUSE) of the SAMD2x can be used to read the reset source from the application code to know the latest reset cause.

Differences Between PIC18F Devices without DMA and PIC18F Devices with DMA

The PIC18F devices with DMA have two additional Reset sources not on legacy PIC18F devices without DMA. The first is a Watchdog Timer Window Violation Reset, which is covered in the **"Watchdog Timer"** section of this document. The second is the Memory Execution Violation Reset, which occurs if the core attempts to execute code from either an address outside implemented program memory or from the specially designated storage area Flash. PIC24F devices do not have equivalents to either of these Resets. Other than these two additional sources, Resets on PIC18F devices with DMA behave the same as PIC18F devices without DMA.

A/D CONVERTER (ADC)

The PIC24F ADC has significant improvements in performance and features over the PIC18F implementation. Improvements include higher conversion rate (samples per second), Automatic Channel Scan mode, 16-bit conversion result buffer, and so on.

The SAMD2x has the following multiple features compared to PIC24F:

- Up to 350,000 samples per second (350 ksps)
- Differential and single-ended inputs
- Five internal inputs
- 1/2x to 16x gain
- Single, continuous, and pin-scan conversion options
- Windowing monitor with selectable channel
- Built-in internal reference and external reference options
- Event-triggered conversion for accurate timing (one event input)
- Optional DMA transfer of conversion result
- Hardware gain and offset compensation
- Averaging and oversampling with decimation to support, up to 16-bit result
- Selectable sampling time

The major features are provided in Table 19.

TABLE 19: A/D CONVERTER FEATURE COMPARISON

Features	PIC18F		PIC24F	SAMD2x
	PIC18F without DMA	PIC18F with DMA		
Resolution	10/12-bit	12-bit	10/12-bit	8/10/12-bit
Conversion Throughput (ksps)	100 ksps	—	500 ksps	350 ksps
Available Voltage Reference Sources	Internal/External	Internal/External	Internal/External	Internal/External
Selectable A/D Clock Divider	Yes	Yes	Yes	Yes
A/D RC Oscillator	Yes	Yes	Yes	Yes
Auto-Sample	Yes	Yes	Yes	Yes
Programmable Sample Time	Yes	Yes	Yes	Yes
Individually Selectable Analog Inputs	No	Yes	Yes	Yes
Special Event Trigger	No	Yes	Yes	Yes
Multiple Channel Scan	No	Yes	Yes	Single
FIFO Buffer	No	Yes, 2-Level	Yes	No
Multiple Result Formats	No	Yes	Yes	No
Differential Channel (comparative) Conversion	No	No	Yes	Yes

The PIC24F and PIC18F A/D Converter modules have similar features. Both have a 10-bit, Successive Approximation Register (SAR) A/D, capable of using a combination of reference pins (V_{REF}+ and V_{REF}-) and analog power pins (AV_{DD} and AV_{SS}) for the reference voltages. Both product lines feature an A/D conversion status bit, selectable A/D clock divider, dedicated A/D RC, auto-sampling with configurable sample time, analog/digital input selection and run-time selectable A/D input. Conversions can be initiated by software, an external interrupt or an output compare event.

Migration Considerations

- The source impedance for the PIC24F module is 2.5 kOhm. Many PIC18F devices are 10 kOhm, although 2.5 kOhm is recommended.
- For the PIC24F module, the module's internal sampling capacitor is 4.4 pF, typical; for the PIC18F module, it is 25 pF, typical. The reduced capacitance increases the affect of the external capacitance on the analog input.
- When configuring the A/D to use the conversion clock, several factors will affect the PIC24F divider selection. These include the reduced T_{AD} and the instruction rate. The PIC24F conversion clock is based on the instruction clock, $T_{CY}/2$, where the PIC18F is based on $F_{OSC}/2$. Due to different instruction rates for a given system clock frequency, the smallest period for the PIC24F A/D clock divider is one F_{OSC} period and two F_{OSC} periods for PIC18F.

- In the SAMD2x, the ADC is clocked by GCLK_ADC. There is also a prescaler in the ADC to enable conversion at lower clock rates. Propagation delay of an ADC depends on resolution, mode (single shot or free running), clock frequency and delay gain. Refer to the product data sheet for the relation of these components.

Differences Between PIC18F Devices without DMA and PIC18F Devices with DMA

PIC18F devices with DMA add a few additional features to the PIC18F ADC module. First, there are hardware CVD controls, which allow for better use of the ADC module for capacitive touch applications. Second, there is a hardware calculation engine (ADC features) that allows for core-independent hardware averaging and low-pass filtering of ADC results.

WATCHDOG TIMER

The Watchdog Timer (WDT) module for the PIC24F is nearly identical to both the WDT on PIC18F devices without DMA and the WDT on PIC18F devices with DMA. All have similar controls (both in Configuration bits and software) and affects (WDT can also be a Reset to be used to exit power-managed modes). The PIC24F WDT has a few unique features, as well as some features missing from the legacy PIC18F devices, but added on PIC18F devices with DMA.

The SAMD2x WDT can be configured to a predefined time-out period and is constantly running when enabled. If the WDT is not cleared within the time-out period, it will issue a system reset. An early-warning interrupt feature is available to indicate an upcoming watchdog time-out condition.

One more feature, the window mode makes it possible to define a time slot (or window) inside the total time-out period during which the WDT must be cleared. If the WDT is cleared outside this window, either too early or too late, a system reset will be issued. Compared to the normal mode, this can also catch situations where a code error causes the WDT to be cleared frequently.

The comparison of the PIC18, PIC24F, and SAMD2x devices are presented in Table 20.

TABLE 20: WATCHDOG TIMER FEATURE COMPARISON

Features	PIC18F		PIC24F	SAMD2x
	PIC18F without DMA	PIC18F with DMA		
Configurable Time-out Period	Yes (through post-scaler)	Yes (through pres-caler)	Yes (through pres-caler and postscaler)	Time-Out Period in Config register
Software Enable	Yes	Yes	Yes	Yes
Exit Power-Managed modes	Yes	Yes	Yes	Yes
Time-out Range	4 ms to 131s	1 ms to 256s	1 ms to 131s	8 to 16k clock cycles
Windowed WDT Option	No	Yes	Yes	Yes
Selectable Input Clock	No	Yes	No	Yes

Migration Considerations

The first migration consideration is that the PIC24F WDT counter resets on any clock source switch of the main clock. The PIC18F WDT counter resets on a variety of conditions, which are outlined in the **"Watchdog Timer (WDT)"** section of the data sheet for the PIC18F device in question. The second consideration is that the WDT Reset flag in PIC18F devices is active-low, while the one on PIC24F devices is active-high, and these bits will need to be initialized to the inactive state at POR or BOR to properly detect WDT Resets. When migrating a legacy PIC18F device, ensure to use the 1:128 prescaler setting on the PIC24F device to allow for the same postscaler settings to be used between the two devices. When migrating a PIC18F device with DMA, the period must be manually calculated using the prescaler/postscaler on the PIC24F device to match the one on the PIC18F device. In addition, when migrating a Windowed Watchdog Timer application from a PIC18F device with DMA to PIC24F devices, bear in mind that the PIC24F window is non-programmable and fixed at a 75% window delay (window setting, '0b001', on PIC18F Windowed Watchdog Timers).

The SAMD2x WDT is asynchronous and runs from a CPU-independent clock source. The WDT will continue operation and issue a system reset or interrupt even if the main clocks fail. After a Power-on Reset, some registers will be loaded with initial values from the NVM User Row, this should be considered while configuring the WDT.

Writing 0xA5 to this register will clear the Watchdog Timer and the watchdog time-out period is restarted. Writing any other value will issue an immediate system reset.

Differences Between PIC18F Devices without DMA and PIC18F Devices with DMA

PIC18F devices with DMA have additional features on the WDT, as well as some slight differences in setup. The primary setup difference is that the period is configured using a prescaler instead of a postscaler, and the prescaler allows for 1 ms to 256s periods, scaling logarithmically (1 ms, 2 ms, 4 ms, up to 256s). This means that a 131s period is not possible on PIC18F devices with DMA. In addition, PIC18F devices with DMA have Windowed Watchdog Timer features, much like the PIC24F devices, which makes the two Watchdog Timers even more similar between PIC18F devices with DMA and PIC24F families.

COMPARATOR AND COMPARATOR VOLTAGE REFERENCE MODULES

The comparator modules on the PIC18F and PIC24F devices share many of the same features. Each has two comparators with various configuration selections. The PIC18F version has only eight selections, one of which is disabling comparators. The PIC24F version is more configurable, allowing individual control over many of the options that are fixed on PIC18F. In addition to the comparator module, both PIC18F and PIC24F offer a comparator voltage reference based on a resistor ladder circuit.

The Analog Comparator module in the SAMD2x MCUs implements four individual comparators. Each comparator compares the voltage levels on two inputs and provides a digital output based on the comparison. Each comparator may be configured to generate interrupt requests and peripheral events upon several different combinations of input change.

The comparators are always grouped in pairs on each port. The AC module may implement two pairs. The first pair is called Comparator 0 (COMP0) and Comparator 1 (COMP1), second pair is of Comparator 2 (COMP2) and Comparator 3 (COMP3). They have identical behaviors but have separate control registers. Each comparator has one positive and one negative input. Each pair can be set in window mode to compare a signal to a voltage range instead of a single voltage level.

Table 21 provides the feature comparison of the PIC18F, PIC24F and SAMD2x devices.

TABLE 21: COMPARATOR FEATURE COMPARISON

Features	PIC18F[1]		PIC24F[1]	SAMD2x
	PIC18F without DMA	PIC18F with DMA		
Comparators	2	2	2/3	4
Output Inversion Control	Yes	Yes	Yes	No
Separate Comparator Enables	Yes[2]	Yes	Yes	Yes
Comparator Output on I/O Pin	Yes	Yes	Yes	Yes
Multiple Input Selections	Yes	Yes	Yes	Yes
Detecting Individual Comparator Output Changed States	Tracked in Firmware by User	Hardware	Hardware	No

Note 1: Refer to the device data sheet to check the availability of the specific features supported.
2: Some of the PIC18FJ family devices have a comparator similar to PIC24F devices, please refer to the specific device data sheet for more details.

Migration Considerations

The PIC18F devices with DMA have more options as compared to older PIC18F devices without DMA. They have more input options, as well as the interrupt to be generated on the positive or negative comparator output transitions. The devices also have dedicated register selection for the inverting and non-inverting inputs of the comparator. The status of the output pin is also mirrored in the register as a read-only status bit. This is different in the internal CV_{REF} option as there are no CV_{REF} pins used. Alternatively, a dedicated DAC output can be used to connect to the input pins.

Some of the PIC18FJ devices have the comparator control bits implemented similar to the PIC24F devices, where each comparator has its own dedicated Comparator Control register instead of controlling both comparators from one Comparator Control register. Please refer to the device data sheet for specifics on the implementation of these control bits.

The SAMD2x devices support more features, compared to the PIC24F device. It contains four individual comparators with separate enable capability with flexible input selection, such as bandgap reference voltage, VDD scalar and DAC and so on, providing the outputs on the pins.

Another feature, the Window function mode helps to compare a signal to a voltage range instead of a single voltage level.

Hysteresis can be adjusted to achieve the optimal operation and optional digital filter option available on comparator output.

Comparator Voltage Reference Module

The comparator voltage reference module is used along with the comparator to provide internally controlled voltage reference to the comparator input. This helps the user to control the reference voltage using software. The module is compatible between the PIC24F and PIC18F family devices. Table 22 provides the feature comparison of PIC18F and PIC24F devices.

TABLE 22: COMPARATOR VOLTAGE REFERENCE FEATURE COMPARISON

Features	PIC18F		PIC24F
	PIC18F without DMA	PIC18F with DMA	
Resistor Ladder	16-Tap	N/A(1)	16-Tap
Two Selectable Ranges	Yes	N/A(1)	Yes
Selectable Reference from Analog Power or MCU Power	Yes	N/A(1)	Yes
Voltage Reference Output Enable	Yes	N/A(1)	Yes

Note 1: In the PIC18F devices with DMA, the CVREF module is not used; the devices have a dedicated 5-bit DAC to provide reference to the comparator input.

Note: The SAMD2x does not contain a comparator voltage reference module. However, it provides a 64-level programmable VDD scaler per comparator, which be configured in the SCALER n register.

General Considerations for the SAMD2x devices:

The Main clock is asynchronous to the peripheral interface clock. Due to this asynchronicity, accessing certain registers will require synchronization between the clock domains. Refer to “**Synchronization”** chapter in the data sheet while migrating. Synchronization can be monitored using the Synchronization Busy bit in the Status register (STATUS.SYNCBUSY). When executing an operation that requires synchronization, the STATUS.SYNCBUSY will be set immediately and cleared when synchronization is complete.

Registers with write-access can be optionally write-protected by the Peripheral Access Controller (PAC). Optional write-protection by the PAC is denoted by the "PAC Write-Protection" property in each individual register description.

Some registers are enable-protected, meaning they can only be written when the module is disabled. Enable-protection is denoted by the "Enable-Protected" property in each individual register description.

APPENDIX A: REVISION HISTORY

Revision A (March 2019)

This is the initial version of this document.

Revision B (August 2019)

Added the SAMD2x family of devices throughout the document.

NOTES:

Note the following details of the code protection feature on Microchip devices:

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