

Evaluation of a Low Frequency Clock Oscillation Circuit

SSP-T7-FL 4.4pF ATMEGA128A1-100P [TQFP(14x14) 0.5mm pitch]

Measurement conditions : Vdd=1.6V to 3.6V



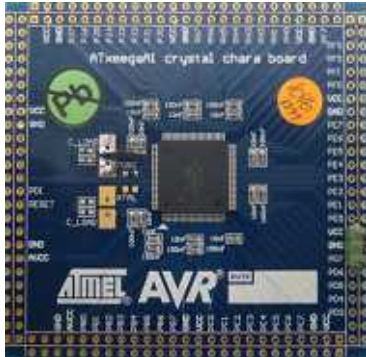
Ultra Low power consumption MCU

XMEGA oscillation circuit and recommended load capacitance

AVR XMEGA : Ultra Low Power 32 kHz Crystal Oscillator

AVR XMEGA's Real Time Counter consumes only 500 nA while running from a 32.768 kHz Crystal Oscillator.

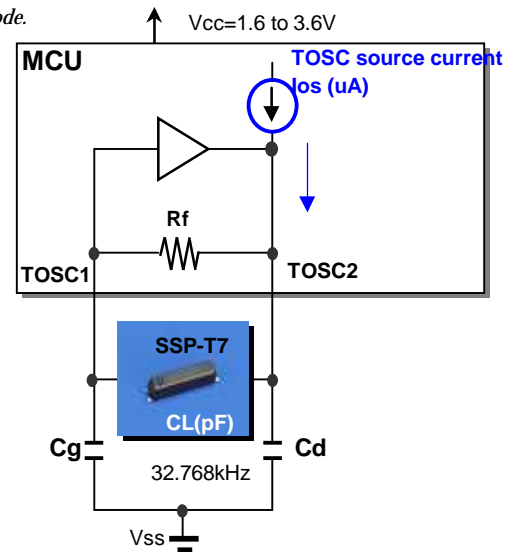
Minimize power consumption by clocking the RTC at 1kHz with an external crystal in low power mode.



SSP-T7 and VT-200 series

SSP-T7-FL CL=3.7pF, 4.4pF, 6.0pF and SSP-T7-F CL=7.0pF, 9.0pF, 12.5pF

VT-200-FL CL=3.7pF, 4.4pF, 6.0pF and VT-200-F CL=12.5pF



Recommended CL resonator

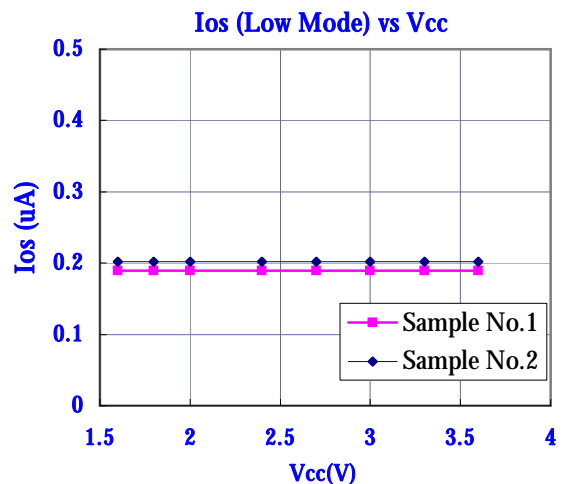
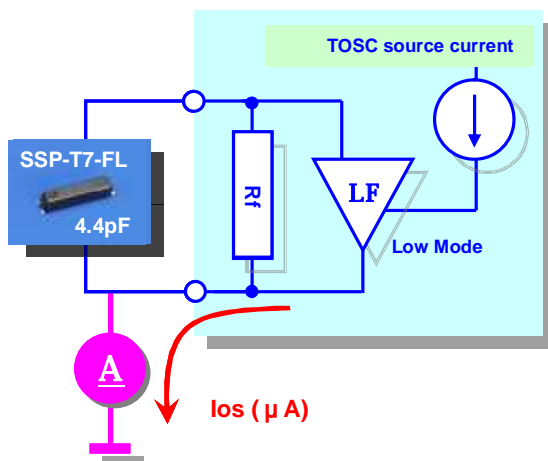
As a result of our evaluation, our recommended resonators are CL=4.4pF as best, and CL=6.0pF as 2nd best, Low CL resonator for ATXMEGA128A1 Low Mode. Table 1 shows that CL=4.4pF surpasses CL=6.0pF in all Osc.charactersitics.

Table 1 Osc.charactersitics CL=4.4pF and CL=6.0pF, Low CL resonator.

Mode	XTL	Vcc (V)	Ios (μA)	CL (pF)	Cg (pF) Cd (pF)	dF/Total*1 (*10 ⁻⁶)	Ts (sec.)	-RL (kΩ)	Osc. allowance
Low	SSP-T7-FL VT-200-FL	3.0	0.189	4.4	2 2	2.57	0.72	775	11.9
				6.0	5 5	2.86	1.22	480	7.4
		1.8	0.189	4.4	2 2	2.72	0.76	735	11.3
				6.0	5 5	2.92	1.27	460	7.1

*1 dF/Total=dF/Vcc(±10%)+dF/Cext(±5%)

Ultra Low Power consumption ATXMEGA128A1 and SSP-T7-FL



Evaluation of Subsystem Clock Oscillation Circuit

SSP-T7-FL 4.4pF ATMEGA128A1-100P [TQFP(14x14) 0.5mm pitch]

Measurement conditions : Vcc=3.0V, 1.8V



New

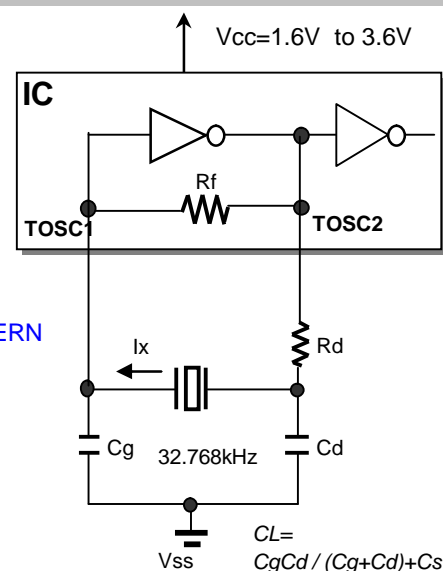
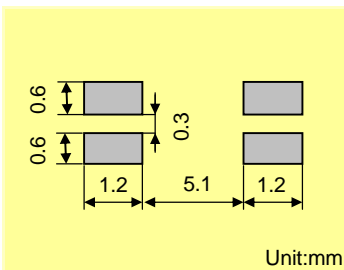
SSP-T7-FL

4.4pF

Model	:SSP-T7-FL
Frequency	:Fo=32.768kHz
Frequency tolerance	:dF/Fo= +/-20x10 ⁻⁶
Load capacitance	:CL=4.4pF
Equivalent series resistance	:R1=65kohm max
Max. drive level	:DL=1x10 ⁻⁶ W max
Level of drive	:DL=0.01x10 ⁻⁶ W typ

FEATURES

- 1.Ultra thin type with 1.4mm Max.
- 2.SMD type suitable for automatic & high density surface mounting.
- 3.Plastic mold package containing highly reliable tubular type quartz crystal.
- 4.Excellent shock and heat resistance.
- 5.Cellular phones,PDA,Radio communication equipment, Portable applications etc.

RECOMMENDED SOLDERING PATTERN

Remark) Ix : current through crystal

MODEL:SSP-T7-FL 4.4pF with ATXMEGA128A1 at 25°C

Key specifications	Low Mode		Remarks
	Vcc=3.0V	Vcc=1.8V	
Current control resistance : Rd (k ohm)	0	0	Control drive level & secure phase margin
Capacitance at gate : Cg (pF)	2	2	Optimal capacitance in response to CL
Capacitance at drain : Cd (pF)	2	2	(CL = Cd // Cg + stray capacitance)

Circuit characteristics (at 25°C)	Vcc=3.0V	Vcc=1.8V	Remarks
Matching Accuracy : df / f (x10 ⁻⁶)	2.6	-3.4	Frequency offset volume at specified Vcc
Voltage Fluctuation : +/-df / V (x10 ⁻⁶)	1.1	1.1	Vcc +/-10% (Standard operating voltage range)
Drive Level : DL (nW)	4.81	5.26	DL=Ix ² Re < 1x10 ⁻⁶ W, Re=R1(1 + Co / CL) ²
Negative resistance : - RL (kohm)	775	735	5 times larger than R1MAX
Oscillation allowance : M (times)	12	11	Judgemental standard of oscillation stability
Low consumption current : Id (nA)	126	131	Cd charge current, Id = f*Cd*Vd
Voltage of oscillation start : Vstrat (V)	1.67	1.67	
Voltage of oscillation stop : Vstop (V)	1.01	1.01	
Oscillation start up time : Ts (sec.)	0.72	0.76	Time to reach 90% of output level

Temperature characteristics of circuit		Vcc=3.0V	Vcc=1.8V	Remarks
at -40°C	Variation : df / T (x10 ⁻⁶)	-116	-116	Typ.Tp=25°C (K = -3.5x10 ⁻⁸ / °C ²)
at +85°C	Variation : df / T (x10 ⁻⁶)	-139	-139	Typ.Tp=25°C (K = -3.5x10 ⁻⁸ / °C ²)

The above mentioned value is only for your reference. The value is for the arbitrary samples and does not guarantee the product's characteristics. Please review and check above parameters at customer's end.

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We value the "takumi" spirit.

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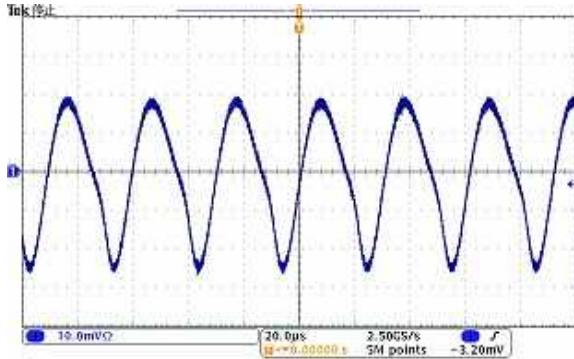
Measurement conditions : $V_{CC}=3.0V, 1.8V$



Test Data at 25°C

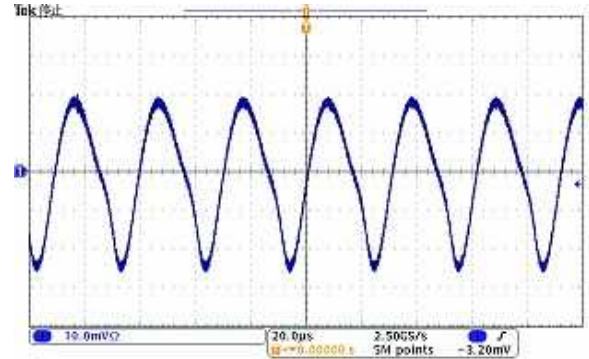
Signal wave from the oscillator

$V_{CC}=3.0V$



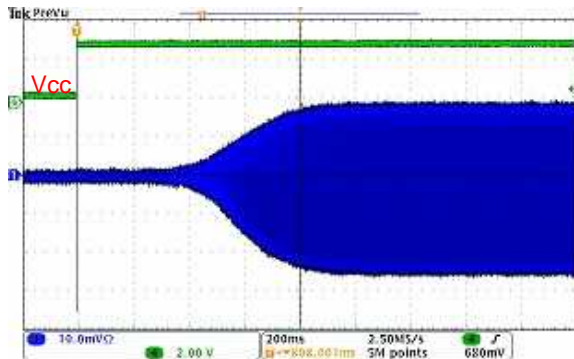
Signal wave from the oscillator

$V_{CC}=1.8V$



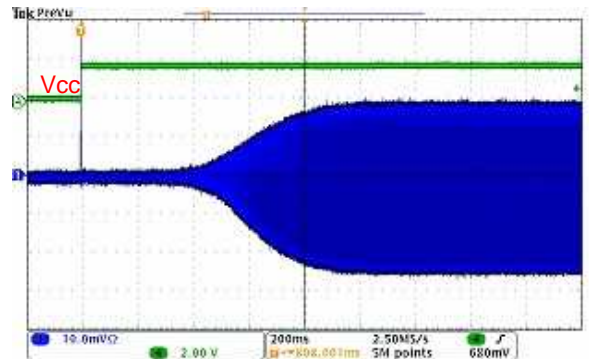
Start up time of SUB_Vout

$V_{CC}=3.0V$

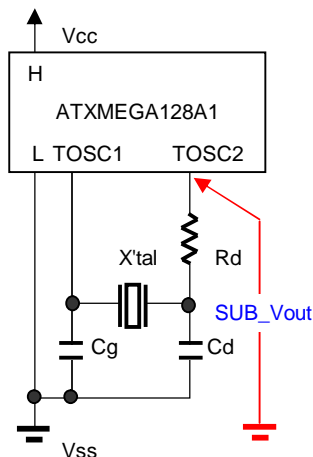


Start up time of SUB_Vout

$V_{CC}=1.8V$

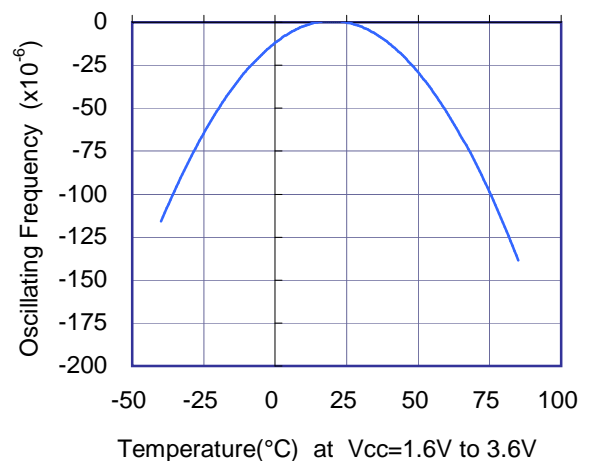


Test Circuit



H : 34
L : 33
TOSC1 : 85
TOSC2 : 86
Fosc : 32

Temperature characteristics of oscillating frequency



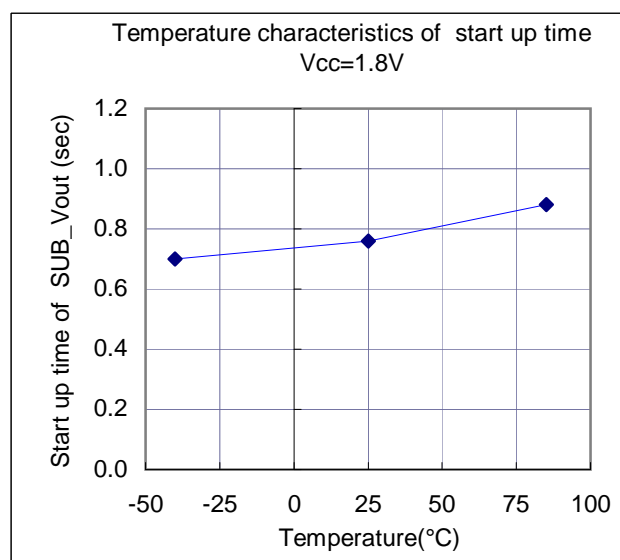
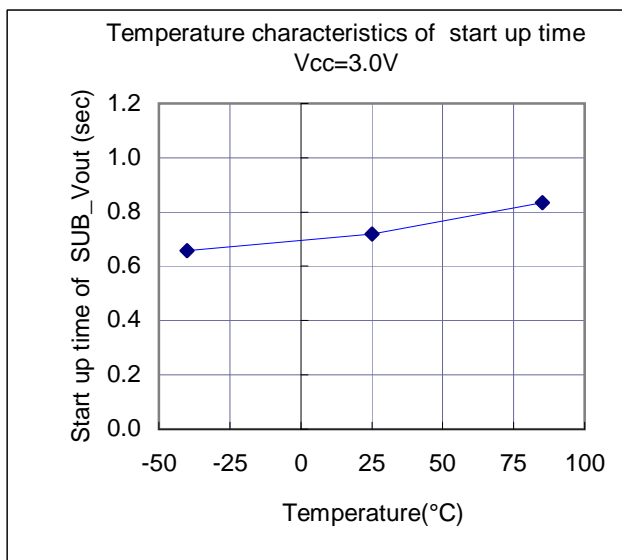
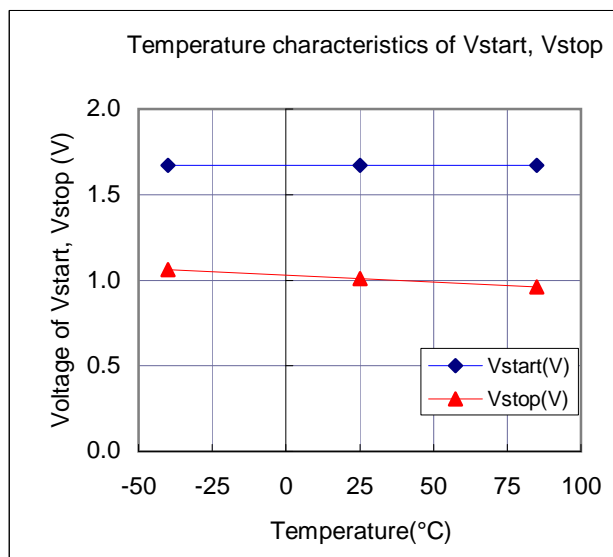
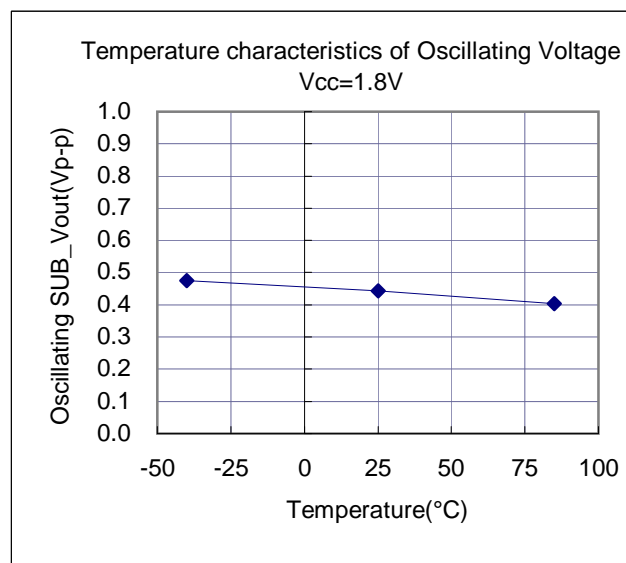
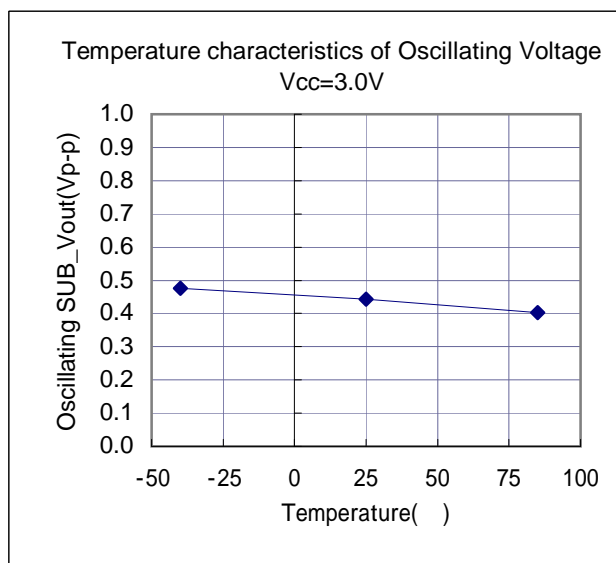
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Measurement conditions : Vcc=3.0V, 1.8V



Test Data : Temperature characteristics



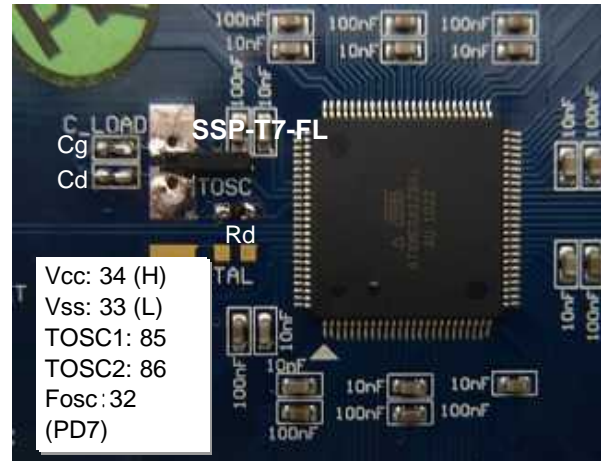
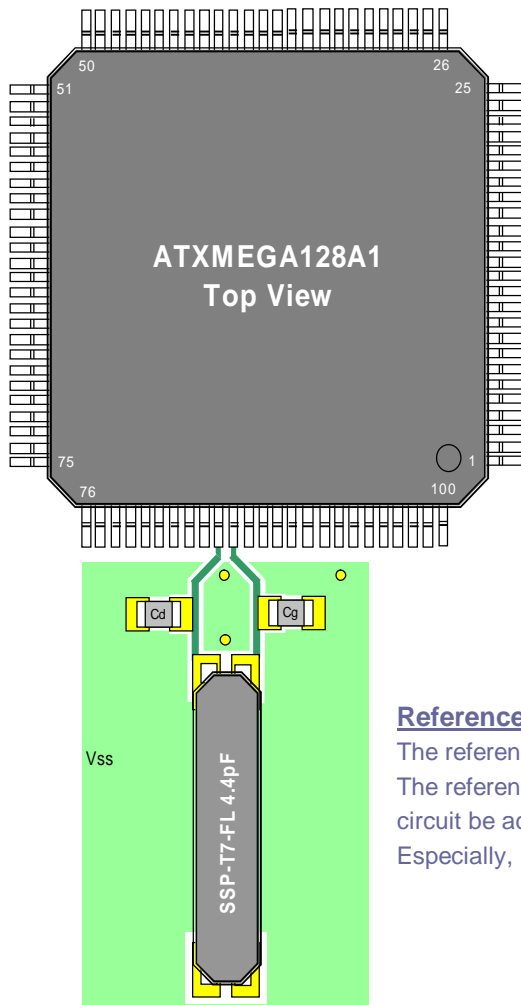
Evaluation of Subsystem Clock Oscillation Circuit

SSP-T7-FL 4.4pF ATMEGA128A1-100P [TQFP(14x14) 0.5mm pitch]

Measurement conditions : Vcc=3.0V, 1.8V



Referential components layout(see Figure 1)



Reference land pattern that SII recommends

The reference pattern can decrease stray capacity C_{os} between terminals TOSC.
The reference pattern can be excellent in the noise-proof, and an efficient oscillation circuit be achieved.
Especially, it is a composition that is appropriate for the low CL oscillation circuit.

Figure 1 Referential components layout

Notes for Board Design

When using a crystal resonator, place the resonator and its load capacitors as close as possible to SUB_in and SUB_out pins.

Other signal lines should be routed away from the resonator circuit to prevent induction from interfering with correct oscillation (see figure 2).

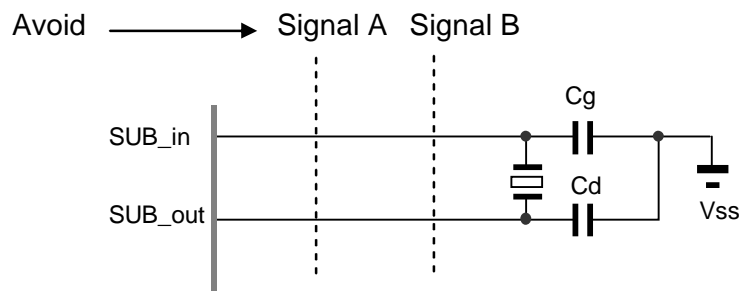


Figure 2 Example of Incorrect Board Design

Remark When using the subsystem clock, insert resistors R_d in series on the SUB_out side.



Evaluation of Subsystem Clock Oscillation Circuit

SSP-T7-FL 4.4pF ATMEGA128A1-100P [TQFP(14x14) 0.5mm pitch]

Measurement conditions : Vcc=3.0V, 1.8V

**[Evaluation Sample at 25°C]**

SAMPLE	No.	CL(pF)	Fo(Hz)	fr(Hz)	R1(kohm)	Co(pF)	C1(fF)	Q(k)
SSP-T7-FL	1	4.4	32767.82	32761.59	40.8	0.89	2.012	59.2
	2	4.4	32768.08	32761.69	37.7	0.90	2.067	62.4
	3	4.4	32767.74	32761.49	38.4	0.91	2.026	62.5

[IC Test Data : IC sample Rd=0k ohm,Cg=2pF, Cd=2pF at 25°C]

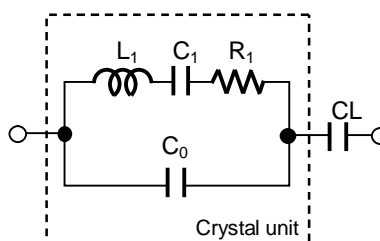
Vcc (V)	IC sample	Fosc(Hz)	df / f(x10 ⁻⁶)	DL(x10 ⁻⁶ W)	-RL (kohm)	Vstart(V)	Ts(sec)
3.0	1	32768.164	2.56	4.81	775	1.67	0.72
	2	32768.169	2.72	4.62	805	1.68	0.70

[IC Test Data : IC sample Rd=0k ohm, Cg=2pF, Cd=2pF at 25°C]

Vcc (V)	IC sample	Fosc(Hz)	df / f(x10 ⁻⁶)	DL(x10 ⁻⁶ W)	-RL (kohm)	Vstart(V)	Ts(sec)
1.8	1	32767.968	-3.42	5.26	735	1.67	0.76
	2	32767.969	-3.39	5.06	775	1.68	0.74

Remark (see figure 3)

$$F_o = f_r \times \{ C_1 / (2 \times (C_o + C_L)) + 1 \} \quad (\text{Hz})$$



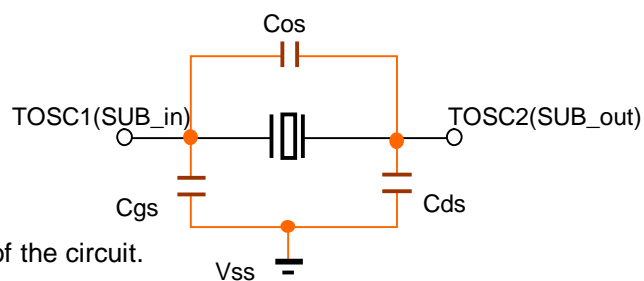
Fo : Load resonance frequency
 fr : Resonance frequency
 R1 : Motional resistance
 C1 : Motional capacitance
 Co : Shunt capacitance
 CL : Load Capacitance

Figure 3 Equivalent circuit of crystal unit, and CL**Remark (see figure 4)**

Approximate formula of the load capacitance of the circuit CL.

$$CL = C_g \times C_d / (C_g + C_d) + C_s \quad (\text{pF})$$

Where Cs(=3.4 to 3.6pF) Stands for stray capacitance of the circuit.



Cos : TOSC1_TOSC2 Stray capacitance
 Cgs : TOSC1_Vss Stray capacitance
 Cds : TOSC2_Vss Stray capacitance

Figure 4 Stray capacitance Cos,Cgs,Cds of the circuit

Resonator circuit constants will differ depending on the resonator element, stray capacitance in its interconnecting circuit, and other factors. Suitable constants should be determined in consultation with the resonator element manufacturer.

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Measurement conditions : $V_{CC}=1.6V$ to $3.6V$ at $25^{\circ}C$



Referential Data : Voltage characteristics

