

Evaluation of a Low Frequency Clock Oscillation Circuit

SSP-T7-F 7.0pF ATMEGA64A1-100P [TQFP(14x14) 0.5mm pitch]

Measurement conditions : Vdd=1.6V to 3.6V



Ultra Low power consumption MCU

XMEGA oscillation circuit and recommended load capacitance

AVR XMEGA : Ultra Low Power 32 kHz Crystal Oscillator

Minimize power consumption by clocking the RTC at 1kHz with an external crystal in low power mode.



SSP-T7 and VT-200 series

SSP-T7-FL CL=3.7pF, 4.4pF, 6.0pF and SSP-T7-F CL=7.0pF, 9.0pF, 12.5pF

VT-200-FL CL=3.7pF, 4.4pF, 6.0pF and VT-200-F CL=12.5pF

Recommended CL resonator

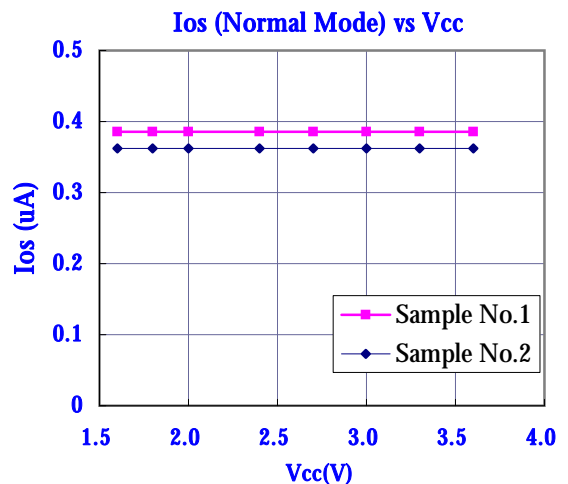
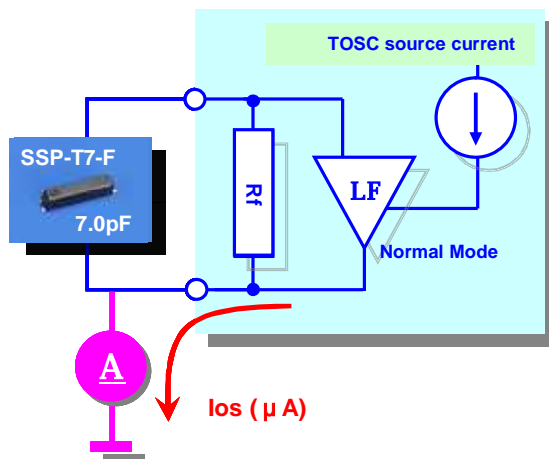
As a result of our evaluation, our recommended resonators are CL=7.0pF as best, and CL=9.0pF as 2nd best, Standard CL resonator for ATXMEGA64A1 Normal Mode. Table 1 shows Osc.charactersitics at CL=7.0pF and CL=9.0pF.

Table 1 Osc.charactersitics CL=7.0pF and CL=9.0pF, Standard CL resonator.

Mode	XTL	Vcc (V)	Ios (μA)	CL (pF)	Cg (pF) Cd (pF)	dF/Total*1 (*10 ⁻⁶)	Ts (sec.)	-RL (kΩ)	Osc. allowance
Normal	SSP-T7-F	3.0	0.386	7.0	8 8	4.00	0.69	797	12.3
				9.0	12 12	3.62	1.03	480	7.4
		1.8	0.386	7.0	8 8	4.28	0.74	727	11.2
				9.0	12 12	3.67	1.10	440	6.8

*1 dF/Total=dF/Vcc(±10%)+dF/Cext(±5%)

Ultra Low Power consumption ATXMEGA64A1 and SSP-T7-F



Evaluation of Subsystem Clock Oscillation Circuit

SSP-T7-F 7.0pF ATMEGA64A1-100P [TQFP(14x14) 0.5mm pitch]

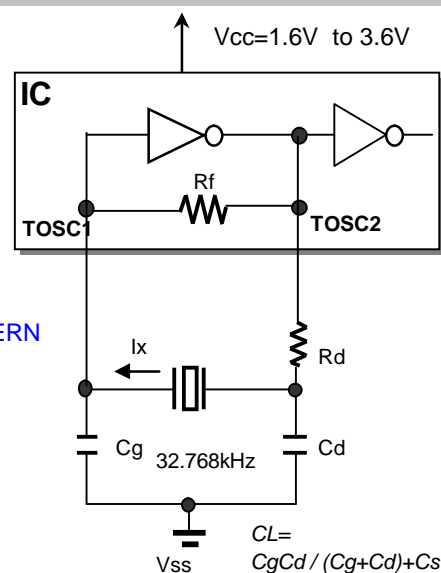
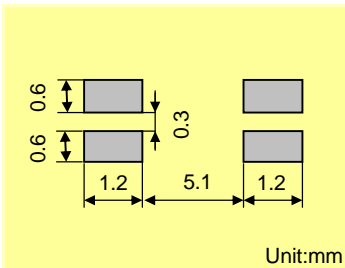
Measurement conditions : Vcc=3.0V, 1.8V

**SSP-T7-F****7.0pF**

Model	:SSP-T7-F
Frequency	:Fo=32.768kHz
Frequency tolerance	:dF/Fo= +/-20x10 ⁻⁶
Load capacitance	:CL=7.0pF
Equivalent series resistance	:R1=65kohm max
Max. drive level	:DL=1x10 ⁻⁶ W max
Level of drive	:DL=0.1x10 ⁻⁶ W typ

FEATURES

- 1.Ultra thin type with 1.4mm Max.
- 2.SMD type suitable for automatic & high density surface mounting.
- 3.Plastic mold package containing highly reliable tubular type quartz crystal.
- 4.Excellent shock and heat resistance.
- 5.Cellular phones,PDA,Radio communication equipment, Portable applications etc.

RECOMMENDED SOLDERING PATTERN

Remark) Ix : current through crystal

MODEL:SSP-T7-F 7.0pF with ATXMEGA64A1 at 25°C

Key specifications	Normal Mode		Remarks
	Vcc=3.0V	Vcc=1.8V	
Current control resistance : Rd (k ohm)	0	0	Control drive level & secure phase margin
Capacitance at gate : Cg (pF)	8	8	Optimal capacitance in response to CL
Capacitance at drain : Cd (pF)	8	8	(CL = Cd // Cg + stray capacitance)

Circuit characteristics (at 25°C)	Vcc=3.0V	Vcc=1.8V	Remarks
Matching Accuracy : df / f (x10 ⁻⁶)	-0.3	-4.1	Frequency offset volume at specified Vcc
Voltage Fluctuation : +/-df / V (x10 ⁻⁶)	0.6	1.1	Vcc +/-10% (Standard operating voltage range)
Drive Level : DL (nW)	15.32	16.46	DL=Ix ² Re < 1x10 ⁻⁶ W, Re=R1(1 + Co / CL) ²
Negative resistance : - RL (kohm)	797	727	5 times larger than R1MAX
Oscillation allowance : M (times)	12	11	Judgemental standard of oscillation stability
Low consumption current : Id (nA)	292	300	Cd charge current, Id = f*Cd*Vd
Voltage of oscillation start : Vstrat (V)	1.67	1.67	
Voltage of oscillation stop : Vstop (V)	1.00	1.00	
Oscillation start up time : Ts (sec.)	0.69	0.74	Time to reach 90% of output level

Temperature characteristics of circuit		Vcc=3.0V	Vcc=1.8V	Remarks
at -40°C	Variation : df / T (x10 ⁻⁶)	-121	-121	Typ.Tp=25°C (K = -3.5x10 ⁻⁸ / °C ²)
at +85°C	Variation : df / T (x10 ⁻⁶)	-135	-135	Typ.Tp=25°C (K = -3.5x10 ⁻⁸ / °C ²)

The above mentioned value is only for your reference. The value is for the arbitrary samples and does not guarantee the product's characteristics. Please review and check above parameters at customer's end.

Seiko Instruments USA Inc.

2990,West Lomita Blvd., Torrance, CA 90505, U.S.A
 Telephone :+1 310-517-7771 Facsimile :+1 310-517-7792
 Email :info@siu-la.com

Seiko Instruments GmbH

Siemensstrasse 9,D-63263 Neu-Isenburg,Germany
 Telephone :+49-6102-297-0 Facsimile :+49-6102-297-320

Email :info@seiko-instruments.de

Seiko Instruments Inc.

1-8,Nakase,Mihama-ku,Chiba-shi,Chiba 261-8507,Japan
 Facsimile :+81-43-211-8030
 E-mail :component@sii.co.jp



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Seiko Instruments Inc.
 Phone:+81-43-211-1207(Direct)

Evaluation of Subsystem Clock Oscillation Circuit

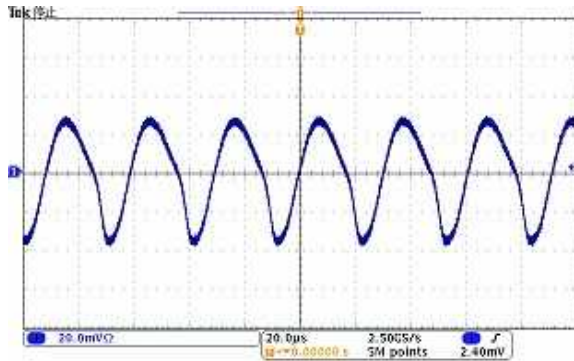
SSP-T7-F 7.0pF ATMEGA64A1-100P [TQFP(14x14) 0.5mm pitch]

Measurement conditions : $V_{CC}=3.0V$, $1.8V$

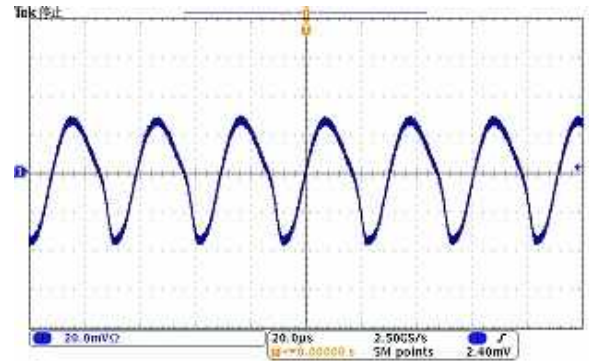


Test Data at 25°C

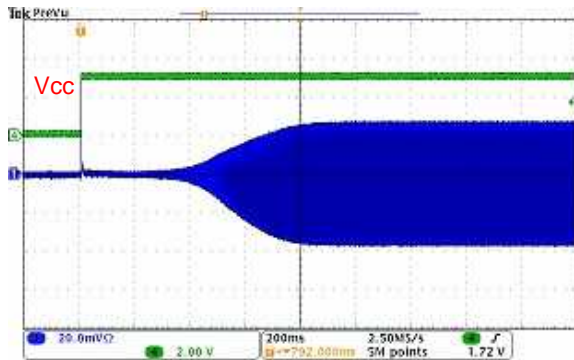
Signal wave from the oscillator
 $V_{CC} = 3.0V$



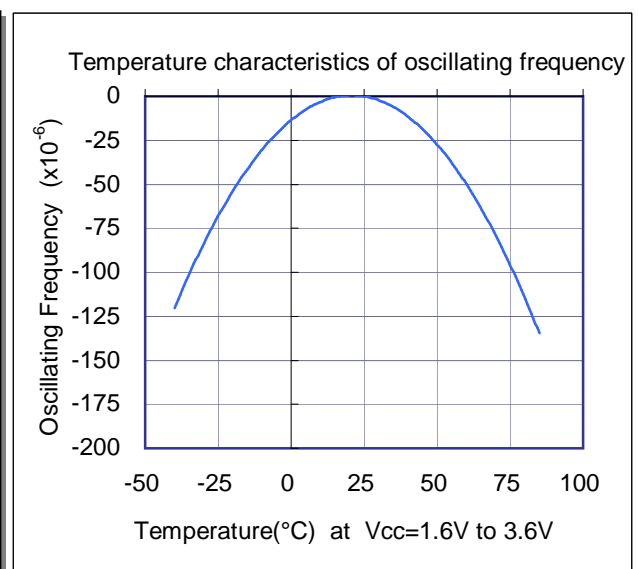
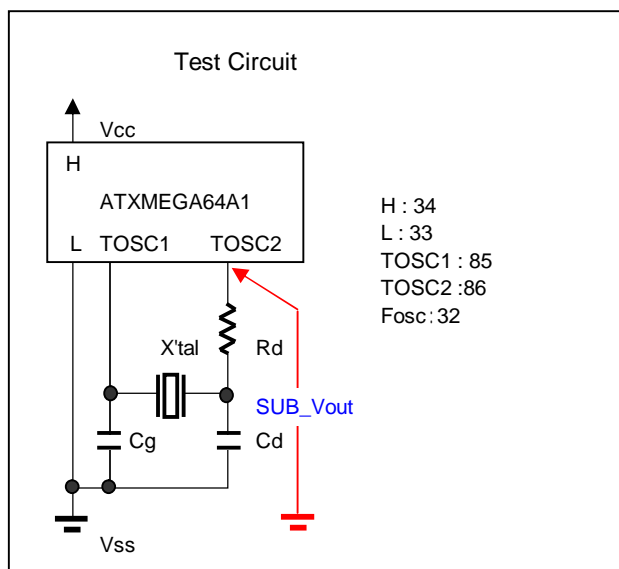
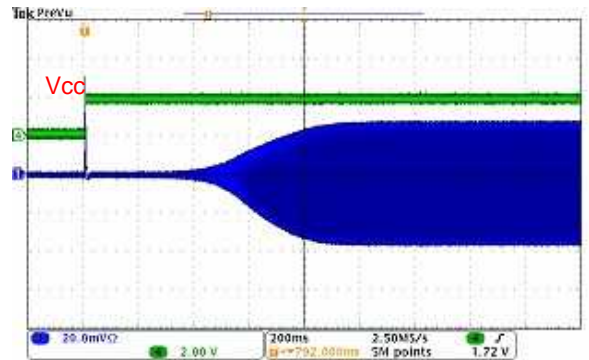
Signal wave from the oscillator
 $V_{CC}=1.8V$



Start up time of SUB_Vout
 $V_{CC}=3.0V$



Start up time of SUB_Vout
 $V_{CC}=1.8V$



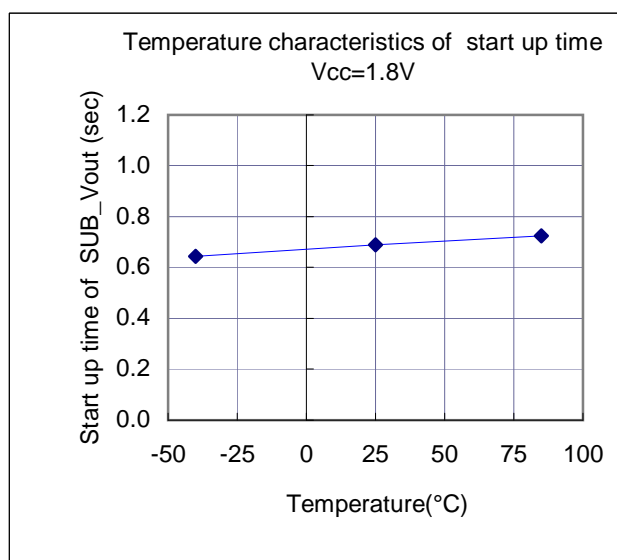
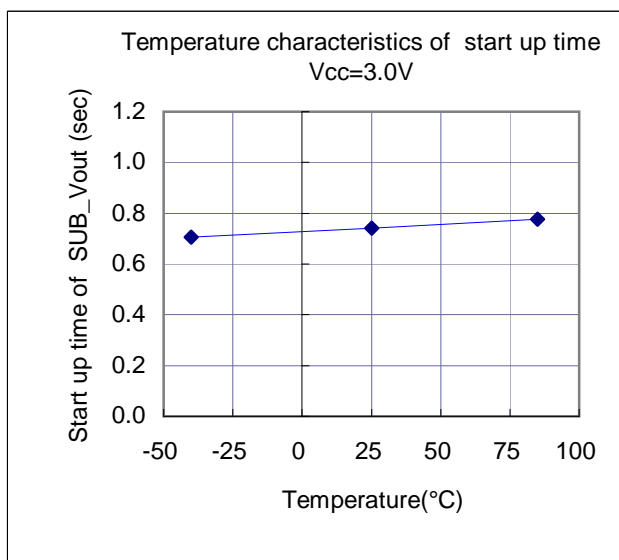
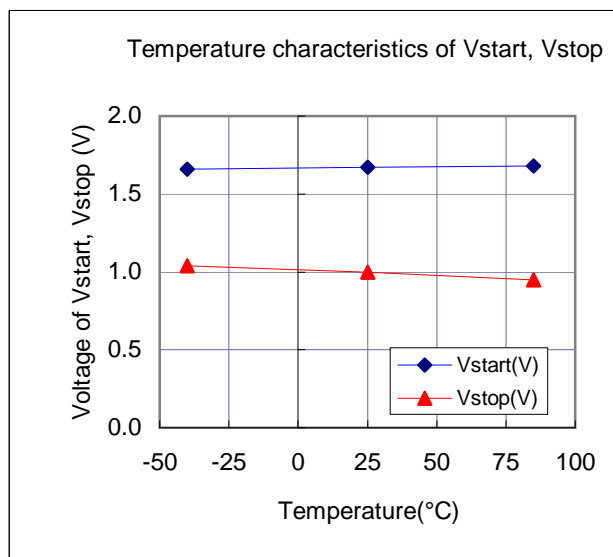
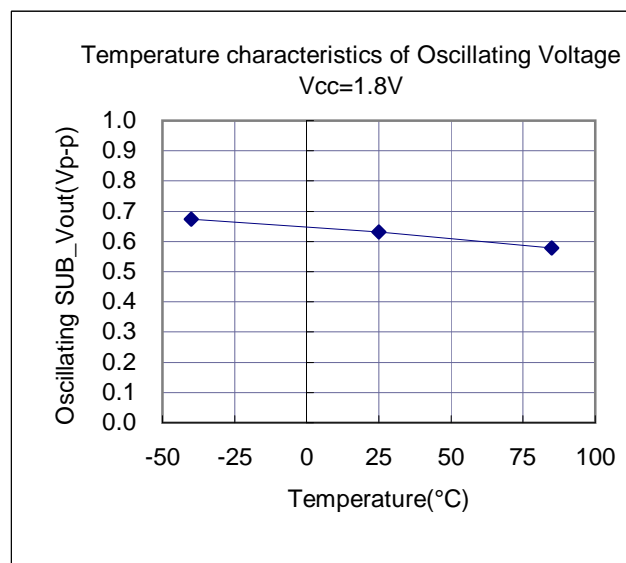
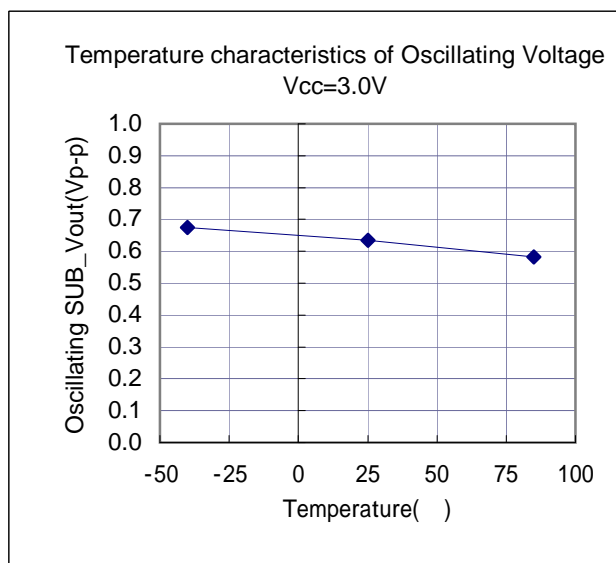
Evaluation of Subsystem Clock Oscillation Circuit

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Measurement conditions : $V_{CC}=3.0V, 1.8V$



Test Data : Temperature characteristics



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SSP-T7-F 7.0pF ATMEGA64A1-100P [TQFP(14x14) 0.5mm pitch]

Measurement conditions : Vcc=3.0V, 1.8V

Referential components layout(see Figure 1)

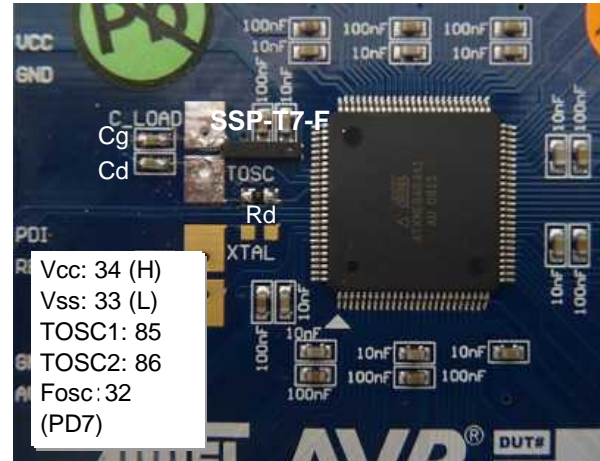
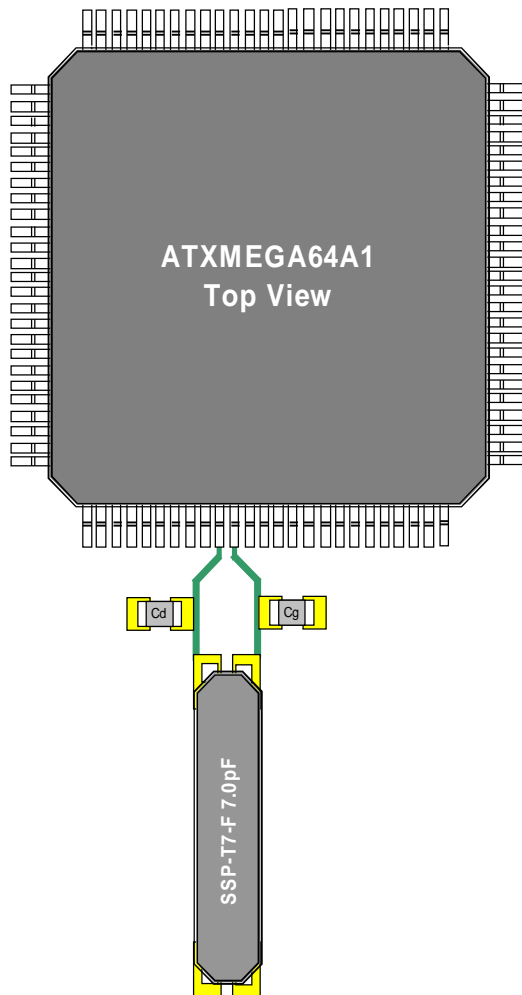


Figure 1 Referential components layout

Notes for Board Design

When using a crystal resonator, place the resonator and its load capacitors as close as possible to SUB_in and SUB_out pins.

Other signal lines should be routed away from the resonator circuit to prevent induction from interfering with correct oscillation (see figure 2).

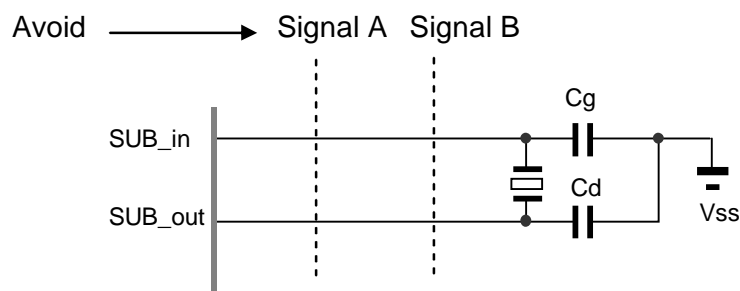


Figure 2 Example of Incorrect Board Design

Remark When using the subsystem clock, insert resistors Rd in series on the SUB_out side.

Evaluation of Subsystem Clock Oscillation Circuit

SSP-T7-F 7.0pF ATMEGA64A1-100P [TQFP(14x14) 0.5mm pitch]

Measurement conditions : Vcc=3.0V, 1.8V

[Evaluation Sample at 25°C]

SAMPLE	No.	CL(pF)	Fo(Hz)	fr(Hz)	R1(kohm)	Co(pF)	C1(fF)	Q(k)
SSP-T7-F	1	7.0	32768.31	32763.88	36.9	0.90	2.137	61.6
	2	7.0	32767.84	32763.42	36.9	0.94	2.142	61.5
	3	7.0	32767.74	32763.34	36.1	0.90	2.121	63.5

[IC Test Data : IC sample Rd=0k ohm, Cg=8pF, Cd=8pF at 25°C]

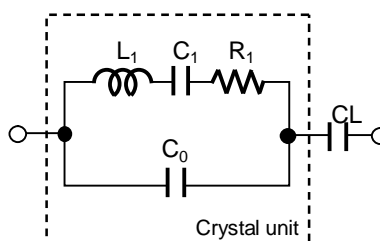
Vcc (V)	IC sample	Fosc(Hz)	df / f(x10 ⁻⁶)	DL(x10 ⁻⁶ W)	-RL (kohm)	Vstart(V)	Ts(sec)
3.0	1	32767.830	-0.31	15.32	797	1.67	0.69
	2	32767.812	-0.85	14.77	727	1.67	0.73

[IC Test Data : IC sample Rd=0k ohm, Cg=8pF, Cd=8pF at 25°C]

Vcc (V)	IC sample	Fosc(Hz)	df / f(x10 ⁻⁶)	DL(x10 ⁻⁶ W)	-RL (kohm)	Vstart(V)	Ts(sec)
1.8	1	32767.707	-4.06	16.46	727	1.67	0.74
	2	32767.695	-4.43	15.99	667	1.67	0.78

Remark (see figure 3)

$$F_o = f_r \times \{ C_1 / (2 \times (C_o + C_L)) + 1 \} \quad (\text{Hz})$$



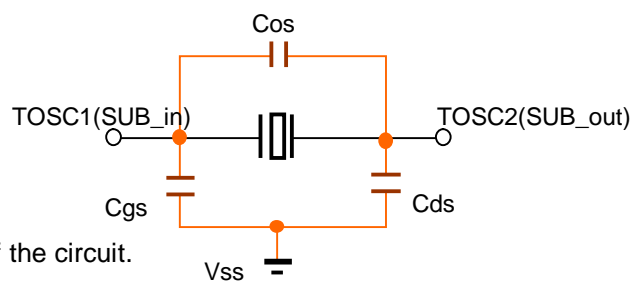
Fo : Load resonance frequency
 fr : Resonance frequency
 R1 : Motional resistance
 C1 : Motional capacitance
 Co : Shunt capacitance
 CL : Load Capacitance

Figure 3 Equivalent circuit of crystal unit, and CL**Remark (see figure 4)**

Approximate formula of the load capacitance of the circuit CL.

$$C_L = C_g \times C_d / (C_g + C_d) + C_s \quad (\text{pF})$$

Where Cs(=3.0 to 3.2pF) Stands for stray capacitance of the circuit.



Cos : TOSC1_TOSC2 Stray capacitance
 Cgs : TOSC1_Vss Stray capacitance
 Cds : TOSC2_Vss Stray capacitance

Figure 4 Stray capacitance Cos,Cgs,Cds of the circuit

Resonator circuit constants will differ depending on the resonator element, stray capacitance in its interconnecting circuit, and other factors. Suitable constants should be determined in consultation with the resonator element manufacturer.

Evaluation of Subsystem Clock Oscillation Circuit

SSP-T7-F 7.0pF ATMEGA64A1-100P [TQFP(14x14) 0.5mm pitch]

Measurement conditions : Vcc=1.6V to 3.6V at 25°C



Referential Data : Voltage characteristics

