

Evaluation of Subsystem Clock Oscillation Circuit

SSP-T7-F 12.5pF ATMEGA16L-44P [TQFP(10x10) 0.8mm pitch]

Measurement conditions : Vcc=3.0V, 5.0V at 25°C

**[Comments from SII engineer]****1 Too large Cs to tune CL=12.5pF**

Fig 1 shows Atmega 16L without external capacitance. Because Atmega 16L has stray capacitance around 20pF, matching test with CL=12.5pF resulted in the matching accuracy of around -30×10^{-6} .

2 Oscillation Allowance

Negative Resistance value is 341kΩ, and oscillation allowance is **5.2** times.

So it satisfies our recommended value of "Oscillation allowance larger than 5 times of R1 max."

Fig. 1: Cs and Osc. characteristics without external capacitance

ATMEGA 16L	Vcc(V)	Cs (pF)	df/f ($\times 10^{-6}$)	Ts (sec.)	RL (kΩ)	M (times)
No.1	5.0	19.6	-27.8	1.00	401	6.2
	3.0	20.4	-29.8	1.36	341	5.2
No.2	5.0	19.2	-26.8	0.98	446	6.9
	3.0	20.0	-28.9	1.30	386	5.9

Stray Capacitance : Cs

Matching Accuracy : df / f

Oscillation start up time : Ts

Negative resistance : | - RL |

Oscillation allowance : M