

Evaluation of Subsystem Clock Oscillation Circuit**SSP-T7-FL 12.5pF ATMEGA169-64P [TQFP(14x14) 0.8mm pitch]**

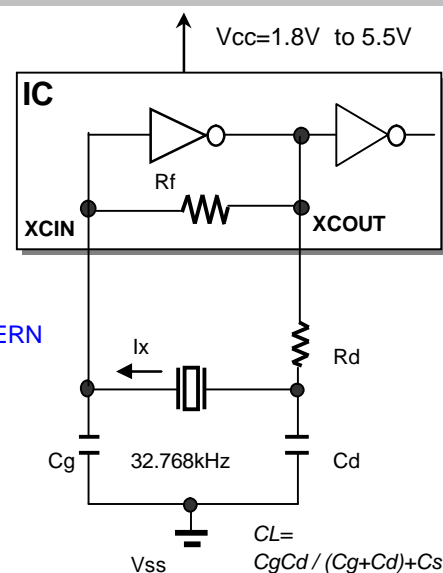
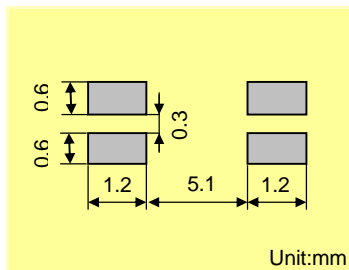
Measurement conditions : Vcc=3.0V, 5.0V

**SSP-T7-F****12.5pF**

Model	:SSP-T7-F
Frequency	:Fo=32.768kHz
Frequency tolerance	:dF/Fo= +/-20x10 ⁻⁶
Load capacitance	:CL=12.5pF
Equivalent series resistance	:R1=65kohm max
Max. drive level	:DL=1x10 ⁻⁶ W max
Level of drive	:DL=0.1x10 ⁻⁶ W typ

FEATURES

- 1.Ultra thin type with 1.4mm Max.
- 2.SMD type suitable for automatic & high density surface mounting.
- 3.Plastic mold package containing highly reliable tubular type quartz crystal.
- 4.Excellent shock and heat resistance.
- 5.Cellular phones,PDA,Radio communication equipment, Portable applications etc.

RECOMMENDED SOLDERING PATTERNRemark) I_x : current through crystal

MODEL:SSP-T7-F 12.5pF with ATMEGA169 at 25°C

Key specifications	Vcc=3.0V	Vcc=5.0V	Remarks
Current control resistance : Rd (k ohm)	0	0	Control drive level & secure phase margin
Capacitance at gate : Cg (pF)	10	10	Optimal capacitance in response to CL
Capacitance at drain : Cd (pF)	10	12	(CL = Cd // Cg + stray capacitance)

Circuit characteristics (at 25°C)	Vcc=3.0V	Vcc=5.0V	Remarks
Matching Accuracy : df/f ($\times 10^{-6}$)	1.0	1.7	Frequency offset volume at specified Vcc
Voltage Fluctuation : $\pm df/V$ ($\times 10^{-6}$)	1.3	1.3	Vcc +/-10% (Standard operating voltage range)
Drive Level : DL ($\times 10^{-6}$ W)	0.09	0.09	$DL = I_x^2 R_e < 1 \times 10^{-6}$ W, $R_e = R_1 / (1 + C_o / CL)^2$
Negative resistance : $ -R_L $ (kohm)	861	861	5 times larger than R_{1MAX}
Oscillation allowance : M (times)	13	13	Judgemental standard of oscillation stability
Low consumption current : Id (nA)	1002	1092	Cd charge current, $I_d = f \cdot C_d \cdot V_d$
Voltage of oscillation start : Vstrat (V)	1.02	1.02	
Voltage of oscillation stop : Vstop (V)	1.01	1.01	
Oscillation start up time : Ts (sec)	0.64	0.50	Time to reach 90% of output level

Temperature characteristics of circuit	Vcc=3.0V	Vcc=5.0V	Remarks
at -40°C	Variation : df/T ($\times 10^{-6}$)	-126	Typ.Tp=25°C (K = $-3.5 \times 10^{-8} / ^\circ C^2$)
at +85°C	Variation : df/T ($\times 10^{-6}$)	-135	Typ.Tp=25°C (K = $-3.5 \times 10^{-8} / ^\circ C^2$)

The above mentioned value is only for your reference. The value is for the arbitrary samples and does not guarantee the product's characteristics. Please review and check above parameters at customer's end.

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We value the "takumi" spirit.

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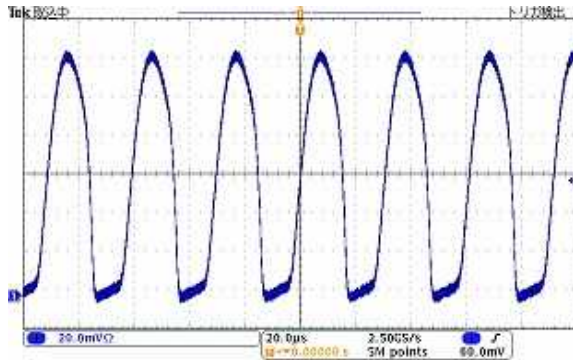
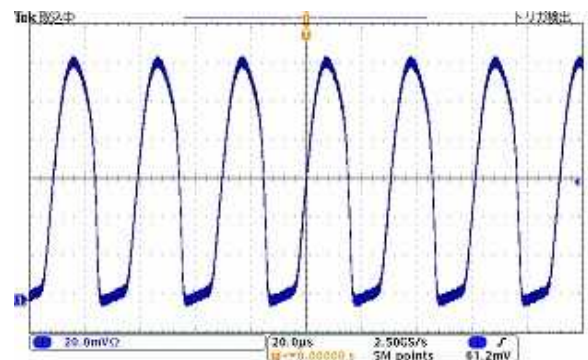
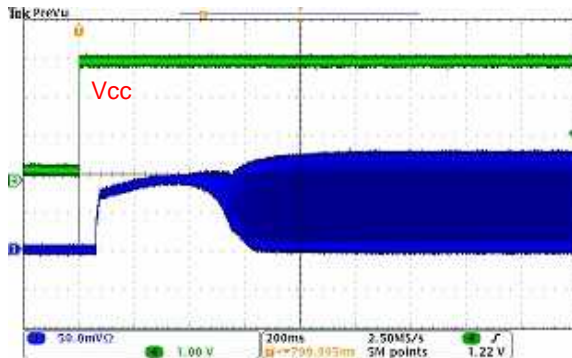
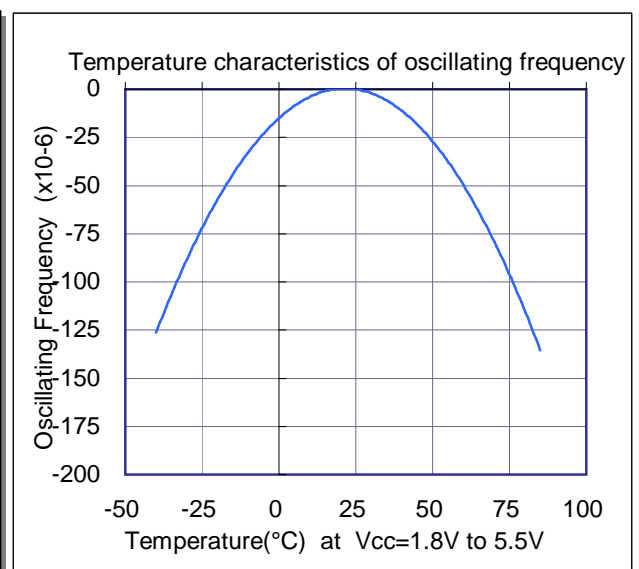
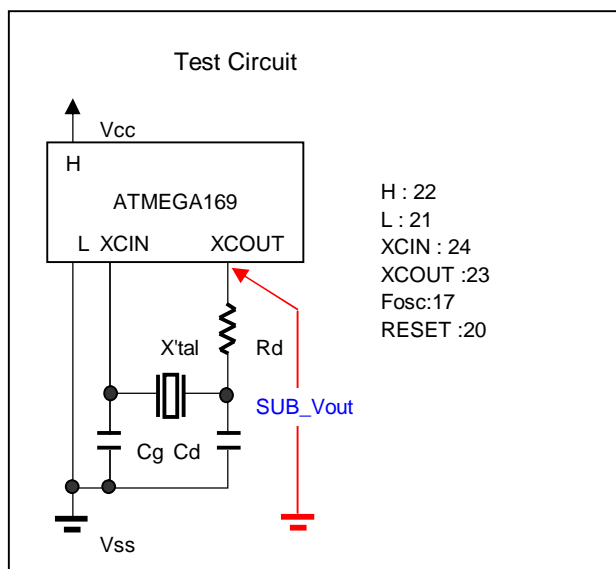
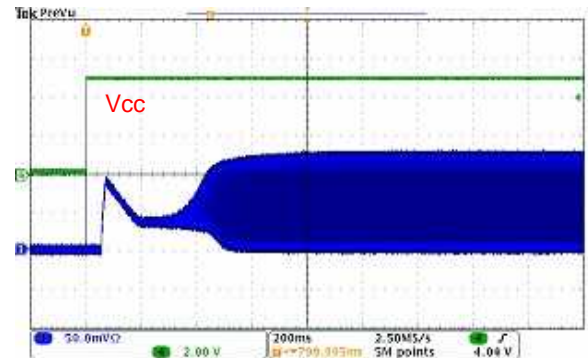
Evaluation of Subsystem Clock Oscillation Circuit

SSP-T7-FL 12.5pF ATMEGA169-64P [TQFP(14x14) 0.8mm pitch]

Measurement conditions : Vcc=3.0V, 5.0V



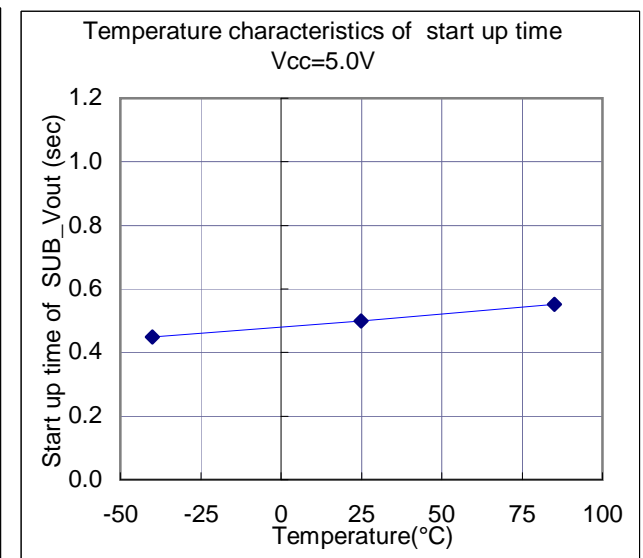
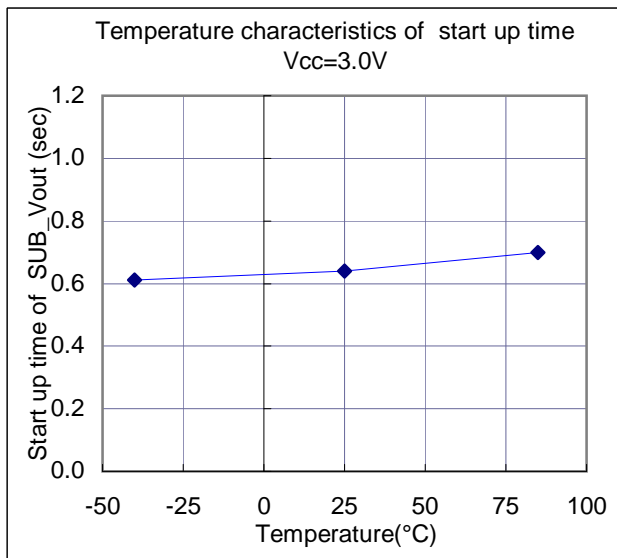
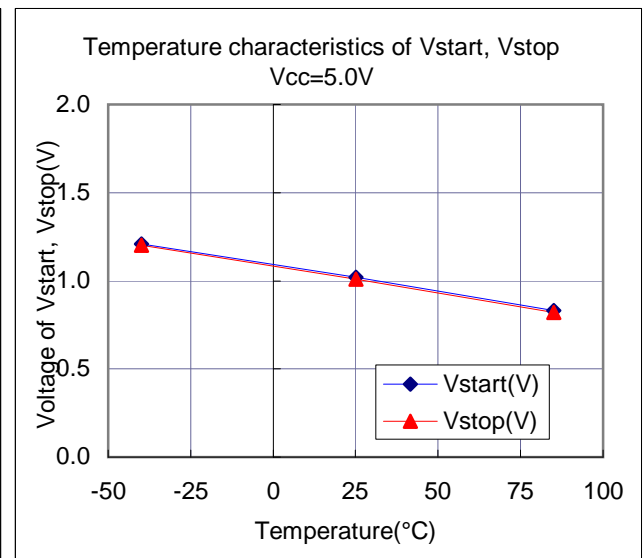
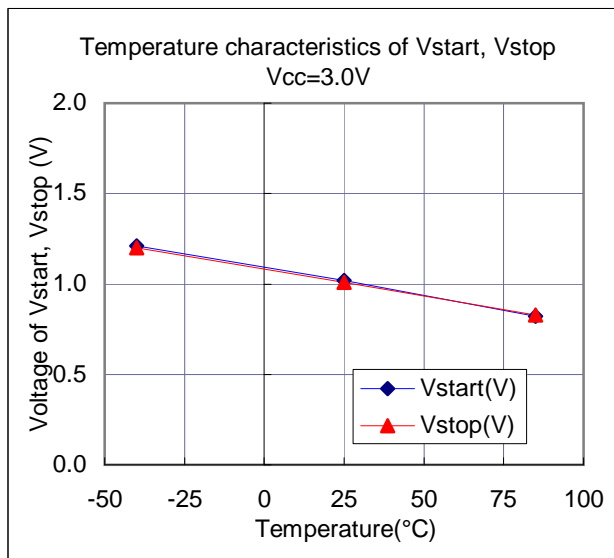
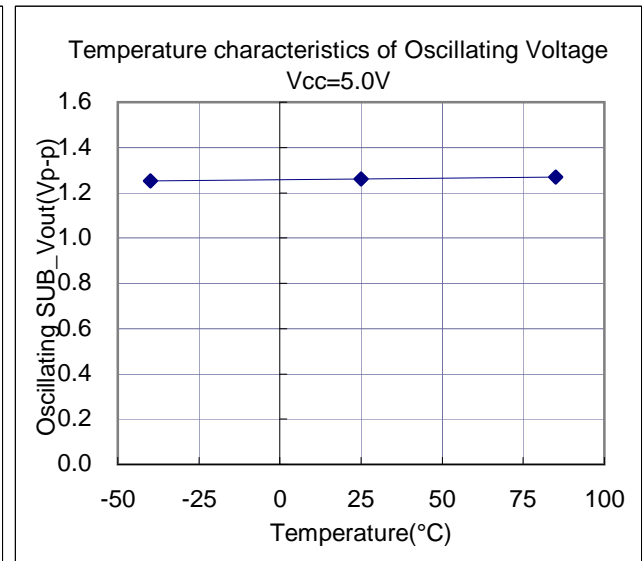
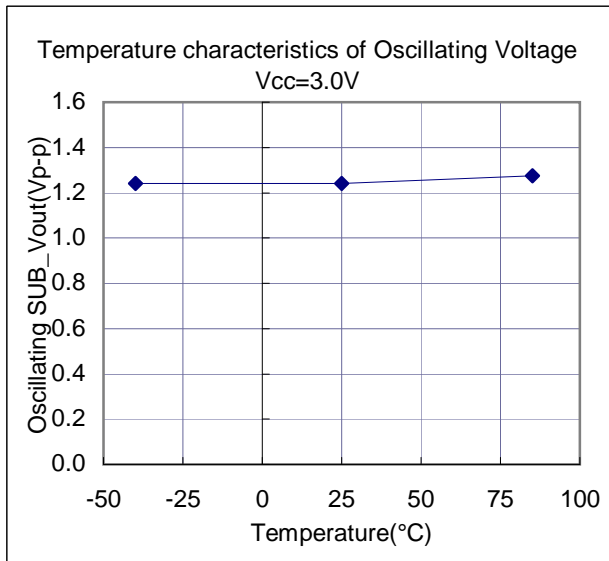
Test Data at 25°C

Signal wave from the oscillator
Vcc=3.0VSignal wave from the oscillator
Vcc=5.0VStart up time of SUB_Vout
Vcc=3.0VStart up time of SUB_Vout
Vcc=5.0V

Evaluation of Subsystem Clock Oscillation Circuit

SSP-T7-FL 12.5pF ATMEGA169-64P [TQFP(14x14) 0.8mm pitch]

Measurement conditions : Vcc=3.0V, 5.0V

**Test Data : Temperature characteristics**

Evaluation of Subsystem Clock Oscillation Circuit

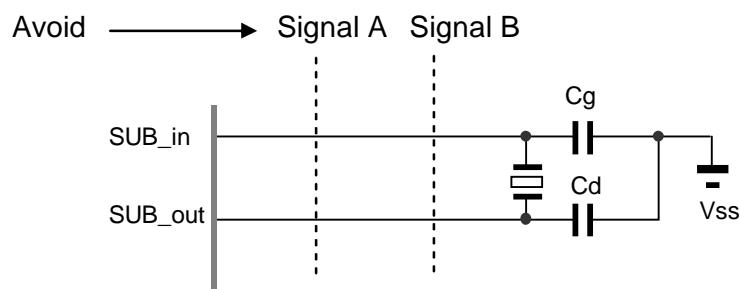
SSP-T7-FL 12.5pF ATMEGA169-64P [TQFP(14x14) 0.8mm pitch]

Measurement conditions : Vcc=3.0V, 5.0V

Referential components layout(see Figure 1)**Figure 1 Referential components layout****Notes for Board Design**

When using a crystal resonator, place the resonator and its load capacitors as close as possible to SUB_in and SUB_out pins.

Other signal lines should be routed away from the resonator circuit to prevent induction from interfering with correct oscillation (see figure 2).

**Figure 2 Example of Incorrect Board Design**

Remark When using the subsystem clock, insert resistors R_d in series on the SUB_out side.

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SSP-T7-FL 12.5pF ATMEGA169-64P [TQFP(14x14) 0.8mm pitch]

Measurement conditions : Vcc=3.0V, 5.0V

[Evaluation Sample at 25°C]

SAMPLE	No.	CL (pF)	Fo (Hz)	fr (Hz)	R1 (kohm)	Co (pF)	C1 (fF)	Q (k)
SSP-T7	1	12.5	32767.87	32765.27	35.4	0.90	2.126	64.6
	2	12.5	32768.15	32765.51	35.6	0.93	2.164	63.1
	3	12.5	32767.99	32765.36	35.5	0.93	2.157	63.5

[IC Test Data : IC sample Rd=0k ohm,Cg=10pF,Cd=10pF at 25°C]

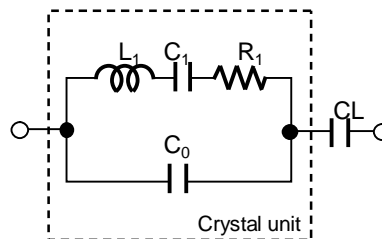
Vcc (V)	IC sample	Fosc (Hz)	df / f (x10 ⁻⁶)	DL(x10 ⁻⁶ W)	-RL (kohm)	Vstart (V)	Ts(sec)
3.0	1	16384.092	1.04	0.09	861	1.02	0.64
	2	16384.076	0.06	0.09	791	1.02	0.66

[IC Test Data : IC sample Rd=0k ohm,Cg=10pF,Cd=12pF at 25°C]

Vcc (V)	IC sample	Fosc (Hz)	df / f (x10 ⁻⁶)	DL(x10 ⁻⁶ W)	-RL (kohm)	Vstart (V)	Ts(sec)
5.0	1	16384.103	1.71	0.09	861	1.02	0.50
	2	16384.090	0.92	0.09	861	1.02	0.50

Remark (see figure 3)

$$F_o = f_r \times \{ C_1 / (2 \times (C_o + C_L)) + 1 \} \quad (\text{Hz})$$



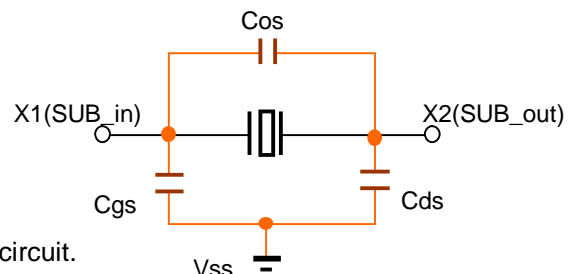
Fo : Load resonance frequency
 fr : Resonance frequency
 R1 : Motional resistance
 C1 : Motional capacitance
 Co : Shunt capacitance
 CL : Load Capacitance

Figure 3 Equivalent circuit of crystal unit, and CL**Remark (see figure 4)**

Approximate formula of the load capacitance of the circuit CL.

$$C_L = C_g \times C_d / (C_g + C_d) + C_s \quad (\text{pF})$$

Where Cs(=2 to 3pF) Stands for stray capacitance of the circuit.



Cos : X1_X2 Stray capacitance
 Cgs : X1_Vss Stray capacitance
 Cds : X2_Vss Stray capacitance

ATMEGA164PA

IC sample	Cs (pF)
1	4.5 ~ 8.3
2	4.3 ~ 8.1

Vcc=5.5~1.8V

Figure 4 Stray capacitance Cos,Cgs,Cds of the circuit

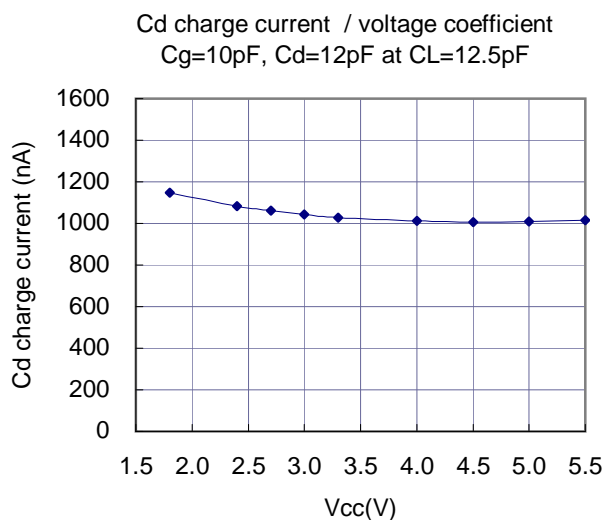
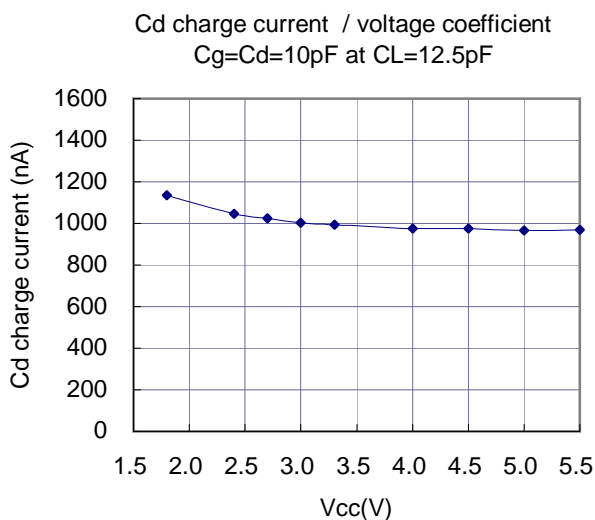
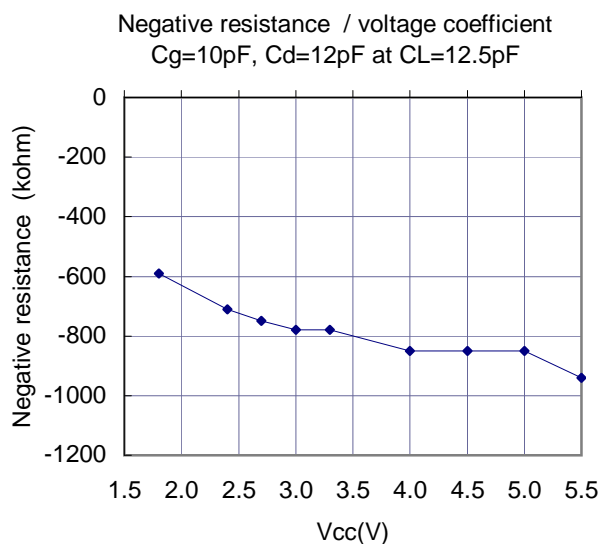
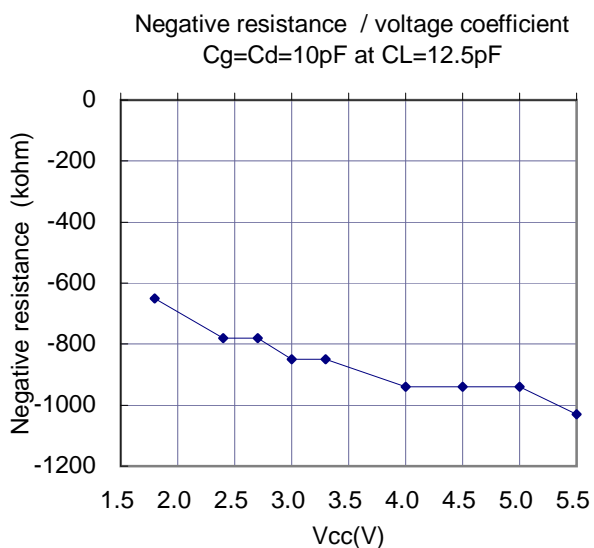
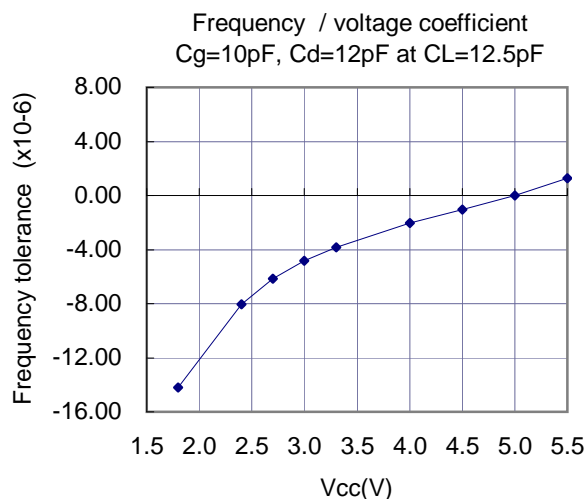
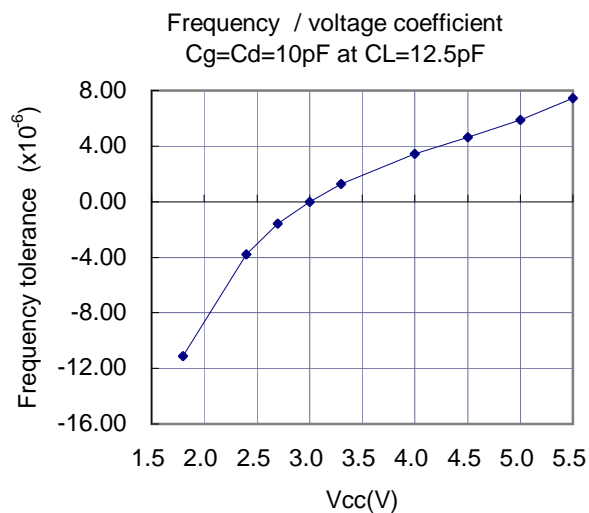
Resonator circuit constants will differ depending on the resonator element, stray capacitance in its interconnecting circuit, and other factors. Suitable constants should be determined in consultation with the resonator element manufacturer.

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Measurement conditions : $V_{CC}=1.8V$ to $5.5V$ at $25^{\circ}C$ 

Referential Data(1) : Voltage characteristics

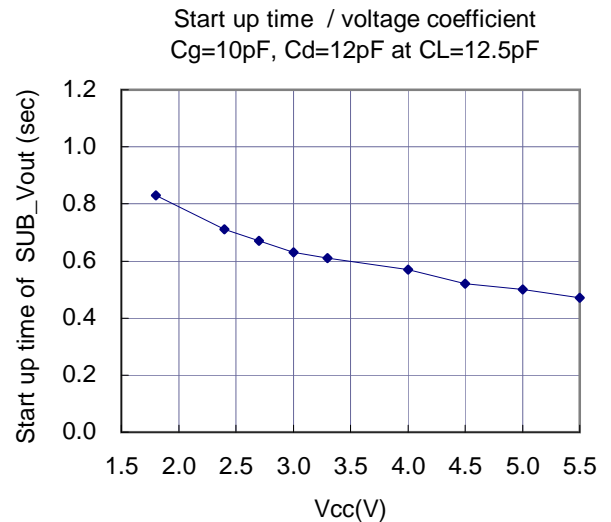
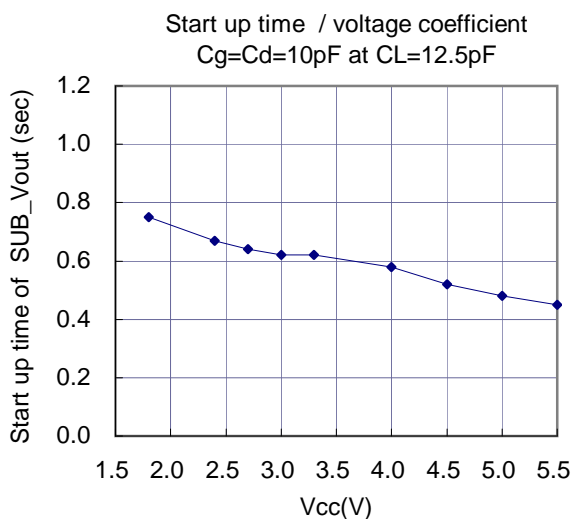
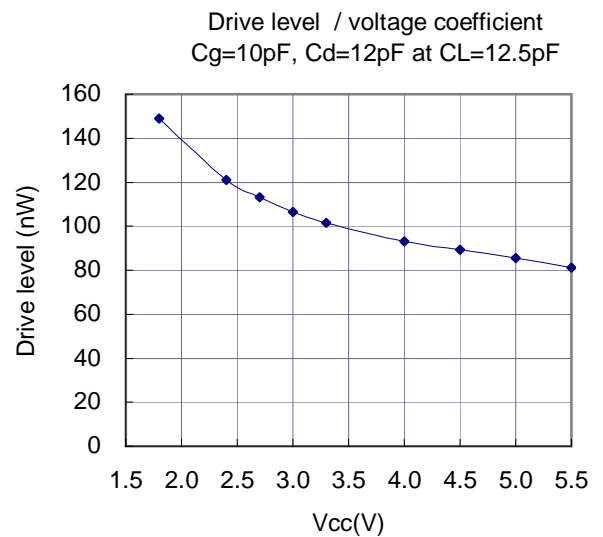
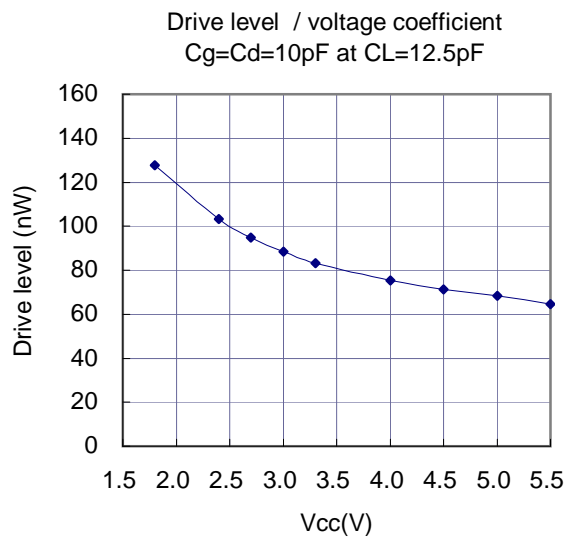
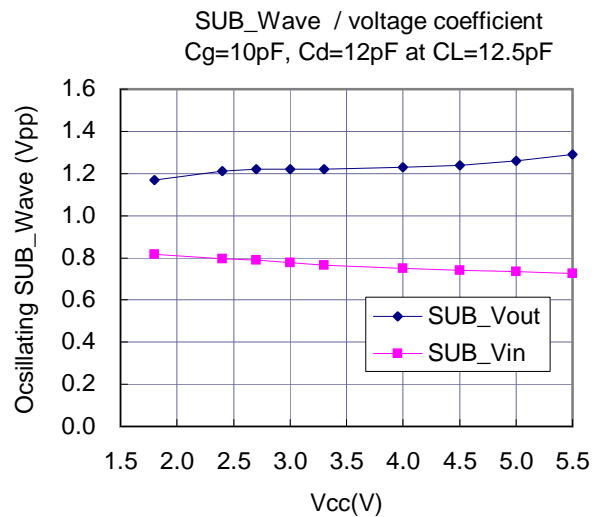
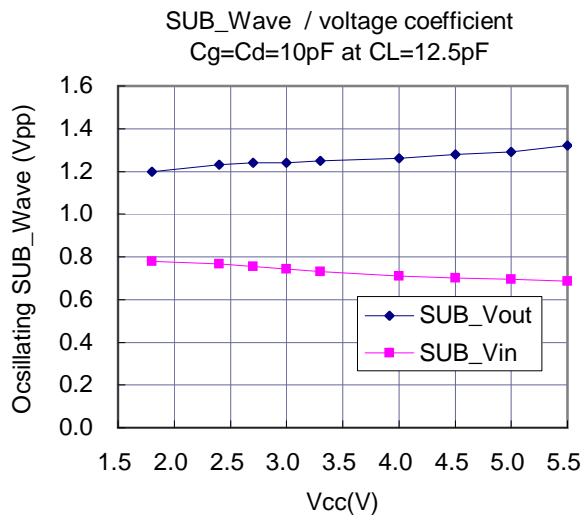


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Referential Data(2) : Voltage characteristics

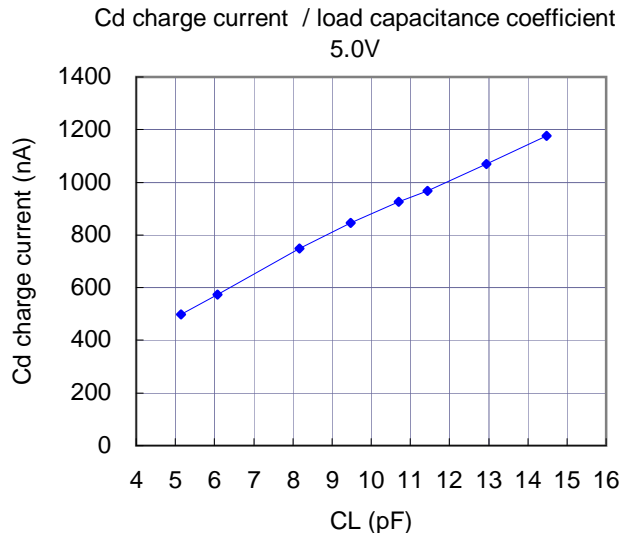
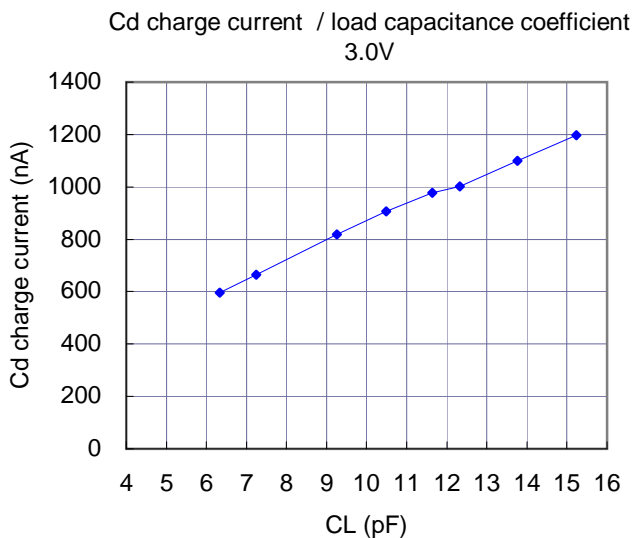
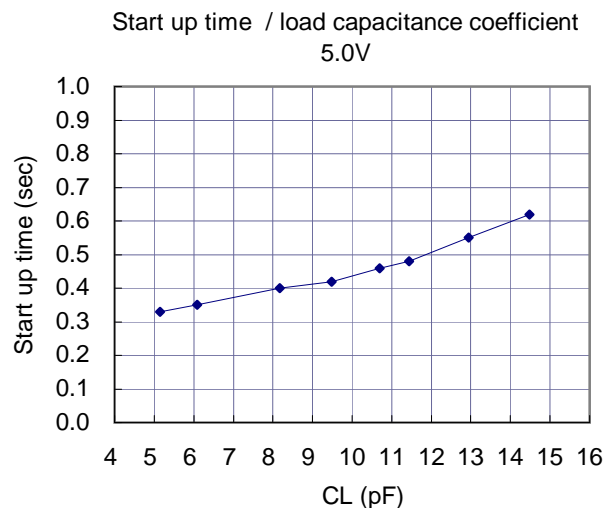
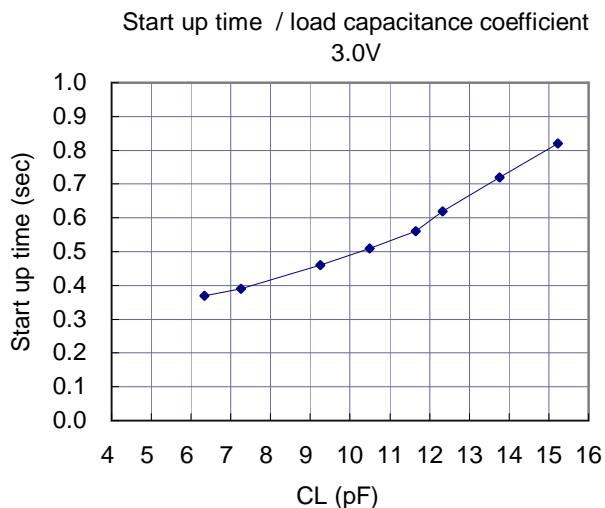
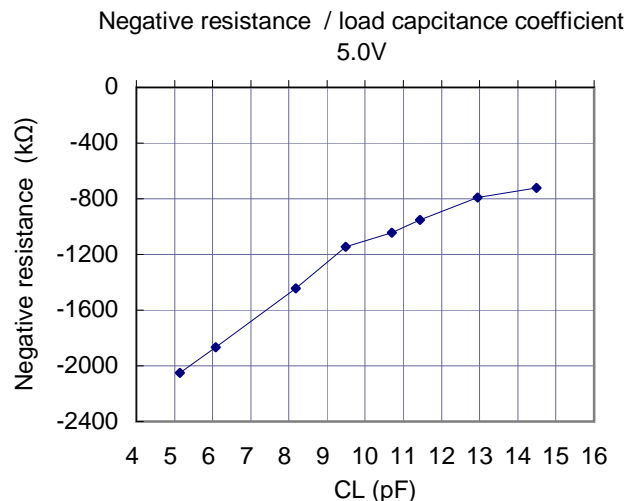
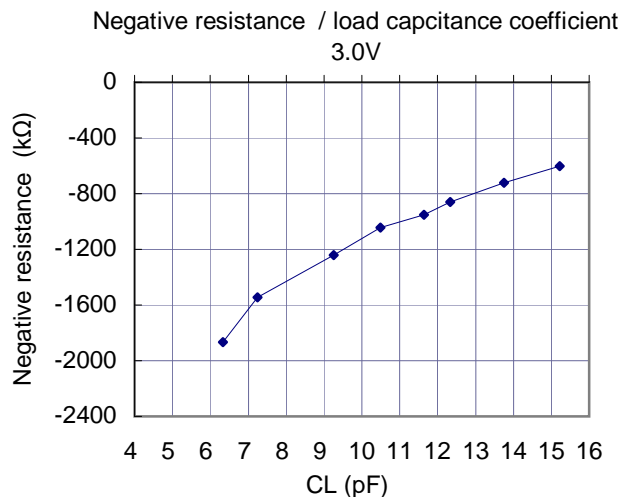


Evaluation of Subsystem Clock Oscillation Circuit

SSP-T7-FL 12.5pF ATMEGA169-64P [TQFP(14x14) 0.8mm pitch]

Measurement conditions : $V_{CC}=3.0V, 5.0V$ at $25^{\circ}C$ 

Referential Data(3) : Load capacitance characteristics



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SSP-T7-FL 12.5pF ATMEGA169-64P [TQFP(14x14) 0.8mm pitch]

Measurement conditions : Vcc=3.0V, 5.0V at 25°C



[Comments from SII engineer]

- 1 According to the referential data (3): Load capacitance characteristics, because Negative Resistance is too High at CL=9.0pF and lower, possibilities of oscillation troubles are high in various operation environments such as temperature, humidity, IC lot variations and so on. As a result, we recommend CL=12.5pF.

Our recommended negative resistance is 5 times larger than R1 max. and less than 1200kohm.
(Rf=5M is assumed)