Synopsys® Synplify® Pro for Microchip Release Notes
Version W-2025.03M-SP1-1
November 2025

This W-2025.03M-SP1-1 release includes software improvements and enhancements for the Synopsys® FPGA synthesis and Identify® tools. Synopsys recommends that you download this version to obtain the latest software improvements.

These release notes present the latest information about the Synplify® FPGA Design tool in the following sections:

About This Release

This W-2025.03M-SP1-1 release includes software improvements and enhancements for the Synopsys® FPGA synthesis tool.

Synopsys recommends that you download this version to obtain the latest software improvements.

Feature and Enhancement Highlights

The following table summarizes the features and enhancements included in this release.

W-2025.03M-SP1-1 Features	
Feature	**Description**
SystemVerilog Enhancements	SystemVerilog supports simple immediate compile time assertion statements inside initial blocks. Supports severity system tasks (*$fatal, $error, $warning, $info*) and the *$display* task. Use *set option disable_sv_assertion_support 1* to disable the support. **Language Support Reference Manual → SystemVerilog Language Support → System Tasks and System Functions → Assertion System Tasks**

Update to Operating System Support for W-Foundation Releases

Starting with Synplify® FPGA Design version W-2024.09-SP1, December 2024, CentOS 7.3 is the primary OS platform for the Synplify® FPGA Design tool.

All Synopsys tools now ship a single executable built on CentOS 7.3 that also works on AlmaLinux 8.4+ in binary compatible mode. There is no change to any other specification of QSC-W such as the compiler version, which remains the same as GNU GCC 12.3.

For more information, see the Release Specific Support web page.

IEEE 1735 Partial File Encryption Support

Starting with the T-2022.09 release, IEEE 1735 partial file encryption only with single envelope, is supported in the Synopsys FPGA synthesis products. Synplify tools with standard compiler do not support multiple encryption envelopes in a file.

Recommended Versions of Compatible Tools

The FPGA design tools are tested with specific versions of other compatible Synopsys and third-party tools. The recommended versions of these tools are listed in the following sections:

Compatible Versions of Synopsys Tools

The table lists the recommended versions for compatible Synopsys tools:

Tool	Recommended Version
VCS®	W-2024.09-SP2

Microchip Supported Devices

The following technologies are supported:

FPGAs	Technology Families
Mixed-Signal	SmartFusion2
Low-Power	• PolarFireSoC • PolarFire • IGLOO2
Rad-Tolerant	RTG4

Identify Tool Supported Devices

The Identify tool supports the device families shown in the table below. You must select devices from the synthesis tool, which get passed to the Identify instrumentor in the synthesis project file. If you specify a library from the synthesis tool that is not supported in the Identify tool, then this results in a Device not supported message when the Identify instrumentor is launched.

Microchip
IGLOO2
PolarFire
PolarFireSoC
RTG4
SmartFusion2

Platforms

The software is supported on the platforms listed below:

Windows	• Windows 10, 11 Professional or Enterprise (64-bit) • Server 2019, Server 2022 (64-bit)
Linux	• CentOS 7.3+ • Red Hat Enterprise Linux 7.3+, 8+ • SUSE Linux Enterprise 12 SP5+, 15 SP2+ (64-bit) • AlmaLinux 8.4+ • Rocky Linux 8.4+ • Ubuntu 20.04, 22.04, and 24.04

Documentation

The following product documents are included with the Synopsys FPGA design tool. Documents can be accessed through the Online help (HTML) and as PDF documents.

Document	Access
User Guide	Online Help, PDF
Reference Manual	
Attribute Reference Manual	
Command Reference Manual	
Language Support Reference Manual	
Messages Reference Manual	

Known Problems and Solutions

The current known problems in the tool are divided into the following categories:

- FPGA Synthesis Known Problems and Solutions
- FPGA and Identify Platform-Specific Known Problems and Solutions
- Identify Tool Known Problems and Solutions

FPGA Synthesis Known Problems and Solutions

The following problems apply to supported features in the Synplify products:

Browser Displays Blank Page When Webhelp is Invoked

When Webhelp is launched for the first time from the Synplify tool, you might view a blank browser window. This is usually noticed with the Red Hat Enterprise Linux or AlmaLinux OS. This issue is due to the **`libfreetype`** variable.

As a workaround, set the **`LD_PRELOAD`** environment variable before starting the Synplify tool:

1. Before setting the environment variable, close all instances of the FireFox browser including instances in all work spaces.
2. Set the environment variable, `LD_PRELOAD /usr/lib64/libfreetype.so.6`

Software Errors Out on Red Hat 8.6

The Synplify tool stops with the following error message, during compilation on Red Hat 8.6:

```
Job: "compiler" terminated with error status: 127
```

Solution: The libnsl.so.1 library is required in the RHEL installation. Run the following command to check if the library is missing:

```
ldd <install>/linux_a_64/c_hdl
```

Undefined Macro Error When Using Microchip PolarFire Technology

Using Microchip PolarFire Libero SoC technology for synthesis might cause an undefined macro error for instantiated device macros. As a workaround with this flow, additional steps are necessary to synthesize and implement a design.

Solution: Make sure the /data/aPA5M/polarfire_syn_comps.v is added as a source file in the Synplify Base or Elite project. This file contains module declarations with timing information for Microchip PolarFire technology primitives which are unavailable in a

Synplify Base or Elite project. For projects created using an earlier Libero SoC version, update the location of this file in the Synplify Base or Elite project.

Handling Constraints on Cores Configured Using Libero SoC Technology

Libero SoC cores might exhibit sub-optimal performance.

Solution: For optimal performance and place-and-route results, import the constraint files generated by the configured cores into the Libero SoC devices, along with the synthesis gate-level netlist. The tool writes the modified constraints on cores to match the instance/net names as per the gate-level netlist.

Windows Certificate Installer Message

If you get a Windows certificate message during installation, it is because of a Synopsys Common Licensing (SCL) change, issued in December 2018. The change introduced Tamper Resistant Licensing (TRL) cryptography, implemented as part of the ongoing enhancement of the security of the Synopsys software. The installer checks if the required certificates are installed and issues a message if an update is needed.

Solution: Contact Synopsys support for the licensing certificate.

Software Does Not Open After Installation

If your software does not open after installation, check if you need to update your Synopsys Common Licensing (SCL) certificates. A SCL change was issued by Synopsys in December 2018, that contained TRL cryptography. This change was implemented as part of the ongoing process of enhancing the security of the Synopsys software.

Solution: To find out if you are missing any required certificates, go to the /bin directory of your installation and run the following:

```
whatscl.exe  --check-cert
```

If certificates are listed as missing, contact the Synopsys support to update the required licensing certificates.

SpyGlass® Tool might not Translate FPGA Constraints Properly

The SpyGlass tool might not translate specific FPGA constraints properly and might generate an error message.

Solution: You must manually create constraints using the SpyGlass format in the SpyGlass design constraint file (SGDC). You must edit the SGDC file to add the SDC constraints.

FPGA and Identify Platform-Specific Known Problems and Solutions

The following platform-specific problems apply to supported features in the Synplify Elite Synplify Base, Synplify, and Identify tools.

False Flagging of Product Executables as Malware

On Microsoft Windows, some endpoint protection systems could flag executables as similar to malware threats. These are false positives, as Synopsys thoroughly scans all released files.

Solution: If your endpoint system blocks a Synopsys file, white-list it so that it is not flagged. Also, open a CASE so that Synopsys can investigate.

The encryptP1735.pl script is Incompatible With Windows DOS or PowerShell

If the encryptP1735.pl encryption script is run on Windows from DOS or PowerShell, it might fail.

Solution: Run the script on Linux. To run it on Windows, use a UNIX-like environment such as Cygwin.

Adobe Reader Error About Opening PDF Files (Linux)

Random links in the document PDFs on the Linux platform do not work. Adobe Reader generates an error message about not being able to find the appropriate PDF file. This does not happen on Windows platforms.

Solution: This is a problem with Adobe Reader on Linux. Work around it by first opening all the PDFs, and then trying the link again.

Identify Tool Known Problems and Solutions

The following problems are specific to the Identify tools:

Instrumentor UI Displays Memory Type as BRAM Instead of Unset

In this release, the Instrumentor UI for Microchip devices displays Memory Type as *BRAM* instead of *Unset* in the *Edit IICE Settings window -> IICE Sampler* tab.

Solution: This issue will be rectified in a future release.

No DRC Check for Technology-Specific Primitive Instances

If instantiated technology-specific primitives have instrumented ports or signals, the tool adds a fanout to that port or signal and does not run DRC (design rule check) for that technology. This might result in a rule violation and an error during synthesis, placement, or routing.

Solution: Avoid the error by ensuring that the design is instrumented in accordance with the DRC rules for that technology.

Context-Sensitive Help might not Display Correct Help Page on Linux

When using context-sensitive help (F1) for the Identify tool on Linux, help might not open the expected page.

Solution: Use the table of contents, or the online help search mechanism to access the correct help page.

Limitations

The current limitations in the tool are divided into the following categories:

- FPGA Synthesis Limitations
- Identify Tool Limitations

FPGA Synthesis Limitations

The following limitations apply to supported features in Synplify Pro.

- Limitations of URAM feature
- Limitations to the Fault Injection Feature
- Page Could Not Be Found Message When Invoking Online Help
- Crossprobing Source Code Files Created with Third-Party Editors

Limitations of URAM feature

The following are not supported:

- SinglePort_URAM_ByteWideWriteEnable: Write First2 mode
- SinglePort_URAM_ByteWideWriteEnable: Read First mode with read enable

Limitations to the Fault Injection Feature

- When using fault injection techniques for mixed HDL designs, RTL instrumentation is not supported. Only SRS instrumentation is supported for mixed HDL designs.
- Only SRS instrumentation is supported for fault injection on signals within the for-generate instantiation.

Page Could Not Be Found Message When Invoking Online Help

When online help is first invoked, it creates a cached version of the compiled help file in a local hierarchy to allow you to save preferences, bookmarks, and full-text search information. This cached version records the path to the installed version. If the same product version is subsequently re-installed in a new directory, invoking online help displays a message, "*The page could not be found*," because the cached version does not recognize the path to the re- installed product.

Solution: Go to the platform-specific directory and clear the cached help files:

Windows:

C:\Users*username*\AppData\Local\assistant\Synopsys*product*

Linux:

~/.local/share/data/assistant/Synopsys/*product*/

- Delete any/all directories named “online*” from the cache directory.
- Restart help. This creates a new cache and correctly displays the online help.

Crossprobing Source Code Files Created with Third-Party Editors

When using source code files created with third-party editors, you sometimes cannot crossprobe to the correct line number in the source file.

Solution: Open the file in the FPGA synthesis tool text editor.

Identify Tool Limitations

The following limitations are specific to the Identify tools.

Verilog/SystemVerilog Limitations With Imported Verdi Signals

There are some Verilog/SystemVerilog limitations when signals are imported directly from the Verdi® platform:

- Enums with *syn_enum_encoding* attribute are not supported for debug selection. If present, they can affect data expansion.
- Conditional expression settings for unions are represented either as a serialized bit vector or as hexadecimal/integer, with the bit width representing the maximum available bit width among all union members. A future enhancement might make it possible for expressions to target individual union members.
- SystemVerilog interface constructs are not supported.

VHDL Limitations With Imported Verdi Signals

There are some VHDL limitations when the essential signals are imported from the Verdi platform:

- Boolean vector representation in the Identify-generated FSDB is different from the VCS-generated FSDB, but does not have any known impact during the data expansion.
- Record elements are represented in reverse order in the Identify-generated FSDB. This reversal does not have any known impact during data expansion.
- Generate statements are not supported.

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