



G4M-PCIe Verification and Validation Results DRAFT

Revision: 0.7

Date: November 10th, 2014

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Revision History

Version	Date	Modified by	Changes
0.4	Nov 13,2013	NT	L2P2 use case results are added. Revision history table is added.
0.5	Aug 25, 2014	SW	Detailed SAR table Formatting and editing Updated Results
0.6	Sept 8, 2014	SW	Design Use Models Incorporated
0.7	Nov 10 2014	SW	Customer Package Complete with Engineering Feedback

1. Introduction

This document describes the results obtained, and issues faced in the validation and verification of the PCIe. The tools used and the use-model environment are also described.

2. Standards and Requirements

The Design team and the Verification and Validation Team have different reporting structures that are independent of one another.

3. PCIe Reference Design

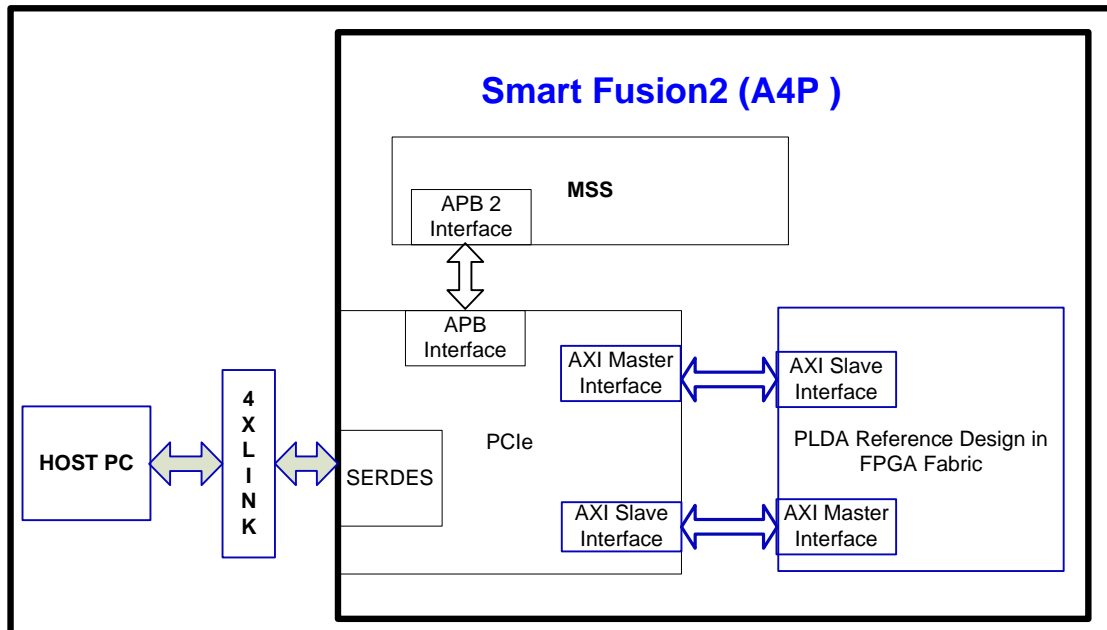


Figure 1: PCIe Reference Design

In the G4 Fabric the following test cases have been implemented

- 1) LED accessing on AXI Master interface
- 2) Read write 1KB of SRAM which is hooked to AXI Master interface
- 3) DMA Read on AXI Slave Interface
- 4) DMA Write on AXI Slave Interface
- 5) DMA Write-Read on AXI Slave Interface

4. Use Models Design

4.1 Use Model 1: Configuration Space accessing

Use case 1a: (Exercising Configuration Space through Link):

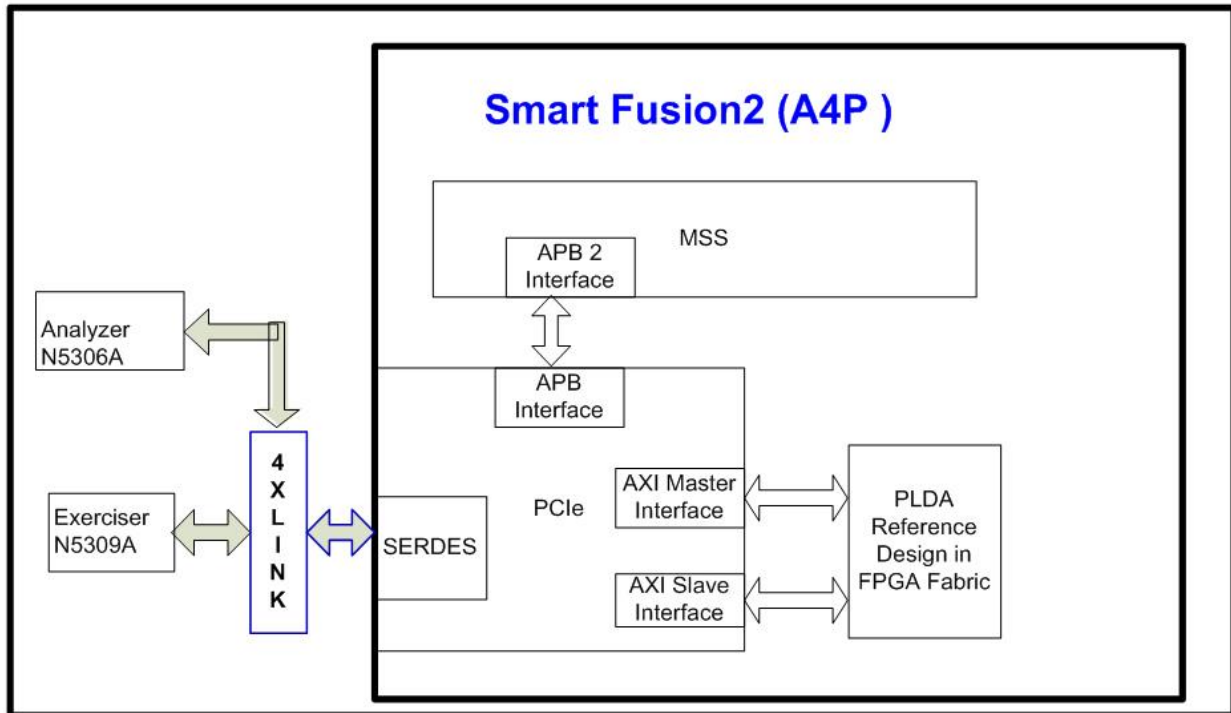


Figure 1 : Exercising Configuration Space through link

Use case 1b: (Exercising Configuration Space through APB interface):

In this Use case G4Main MSS shall access the PCIe configuration space through APB interface.

As the configuration space will be exercised through Link, from APB interface only few registers will be exercised.

SERDES is also configured through the APB interface

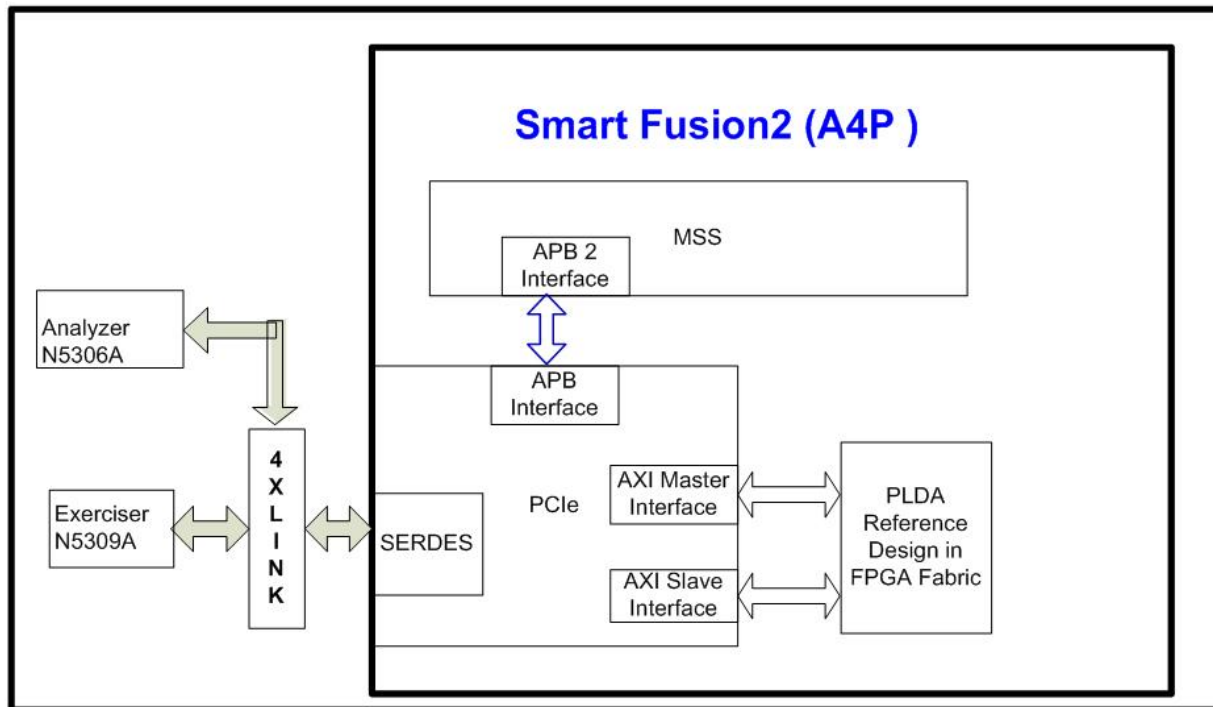


Figure 2 : Exercising Configuration Space through APB interface

4.2 Use Model 2: AXI interface (PLDA reference Design)

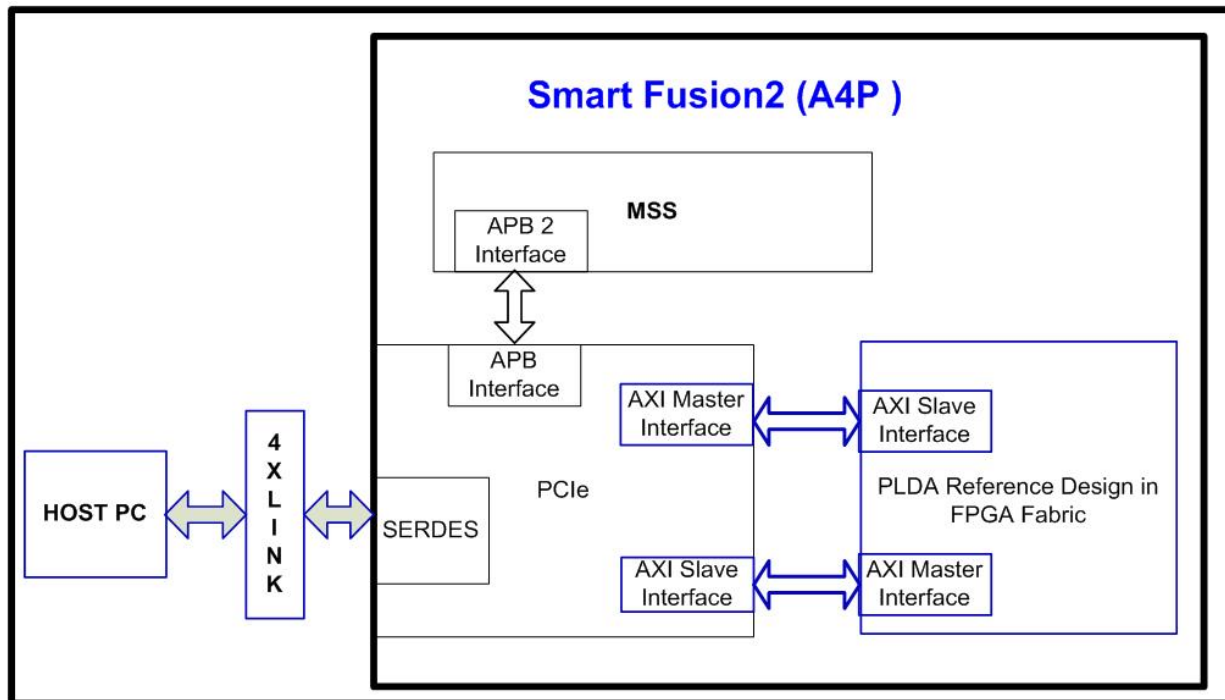


Figure 3 : Exercising AXI Master and Slave Interface

The PLDA reference design the following tests

- 6) Config Space accessing
- 7) LED accessing on AXI Master interface
- 8) Read write 1KB of SRAM which is hooked to AXI Master interface
- 9) DMA Read on AXI Slave Interface
- 10) DMA Write on AXI Slave Interface
- 11) DMA Write-Read on AXI Slave Interface

4.3 Use Model 3: AHB Interface (PLDA reference Design)

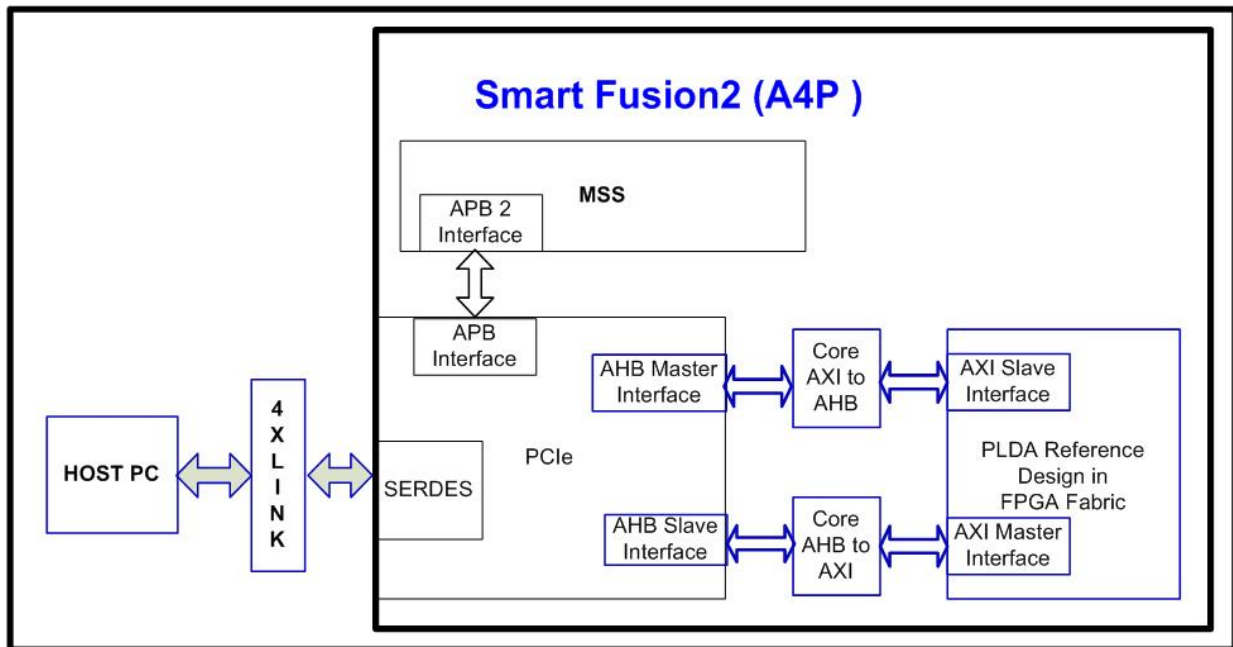


Figure 4 : Exercising AHB Master and Slave Interface

- 1) Config Space accessing
- 2) LED accessing on AXI Master interface
- 3) Read write 1KB of SRAM which is hooked to AXI Master interface
- 4) DMA Read on AXI Slave Interface
- 5) DMA Write on AXI Slave Interface
- 6) DMA Write-Read on AXI Slave Interface

4.4 Use Model 4: PCIe Compliance test

Run the PCIe compliance test cases using the Agilent Exerciser.

The test cases are broadly classified into:

1. PTC (Protocol Test compliance) suite
2. Config Space access

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3. DLLP test cases
4. TLP test cases.
5. LTSSM states testing.

4.5 Use Model 5: PCIe L2/P2 State

L2/P2 Entry:

Only the RP/Switch can make the Endpoint (EP) to enter into L2/P2 state. This can be done by sending the PM_Turn_OFF DLLP packet to the Endpoint.

Exit from L2/P2:

Exit can be initiated by the RP/Switch or from EP.

L2-Exit Sequence initiated by RP :

Note : This case of exit is valid only in case of PCIe-connector using the PERST# side band signal. (PERST# is PERST_N input signal on G4M_SERDESIF – active low signal)

1. RP/Switch need to wake the EP, it asserts the PERST# (PERST_N) side band signal.
2. Once the PERST# signals is asserted, a1DDQ is de-asserted and fundamental reset is asserted to PCIe-Core and SERDES. Link starts training in a normal way.

L2-Exit Sequence initiated by EP:

1. When an EP wants to EXIT L2, then application layer/fabric asserts “wake_req” (Active high signal) input signal to G4M_SERDESIF.
2. Then G4M_SERDESIF (l2_p2_ctrl logic) in L2 state detects “wake_req”, (G4M_SERDESIF) EP can request exit from L2 state, by asserting WAKE_N (WAKE#) output signal.
3. Once (WAKE_N) WAKE# is asserted, a1DDQ is deasserted and fundamental RESET is applied to PLDA-PCIe Core and PHY(SERDES) and released. Link training starts again.

5. Tools Used

PC used: San Jose - wxp-toofan3, HYD- wxp-svglab-01

Application software: Windows_Driver_v2.00_compiled and 2.1.1

IAR Version: 6.4

Silicon Revisions:

REV A: Chip Label (Labeled as G8): M2S050, FGG896 1225, SYA757 ENG

REV B: Chip Label (Labeled as 65): M2S050, FGG896 1235, SA1A8 B

REV C: Chip Label (Labeled as 115):M2S050, FGG896 1250, SK1P7 ENG

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M2S025 SILICON:

Chip Label: M2S025, FGG484 1326 SW3C2

PC used: San Jose – W7-SVGLAB5, WXP-TOOFAN3

Application software: Windows_Driver_v2.00_compiled and 2.1.1

Libero Version: Libero-SOC 11.1.2.16/Libero-SOC 11.2.0.15

6. Use Models Testing

6.1 Use Model 1

This use model is inherently tested in all use models. Use Model 1 is the basic pre-requisite for all use models.

6.2 Use Model 2 AXI Use Cases

6.2.1 *Hardware information:*

The design is configured as: AXI, GEN2, Lane X4, and SERDES 0. Validation board is used for PCIe validation.

Hardware database is at

svn://hoppin/IP/PDV/G4_MAIN/G4M_SERDES/PCIe/tags/1.0.103/design/hw/AXI/Ref_design/GEN1/AXI_X4_VBRD_GEN2.zip

Fabric design is running at 125MHz.

More information on the hardware can be found in the readme file which is at

svn://hoppin/IP/PDV/G4_MAIN/G4M_SERDES/PCIe/tags/1.0.103/readme.txt

6.2.2 *Software information:*

We have two software databases for the PCIe design:

- 1) Reference Design software: Responsible for generating transactions from the Host Machine. Required to be installed on a Windows XP machine.
- 2) IAR firmware: Developed to access register interface of SERDES and PCIe Controller. APB interface provided to access controller register space via CM3 interface.

IAR firmware design database is at

svn://hoppin/IP/PDV/G4_MAIN/G4M_SERDES/PCIe/tags/1.0.103/design/fw/GRL/serdes_config.zip

UART1 is used in this design. UART is configured at 57600.

Please select option 4 to configure the AXI master and slave windows.

The below figures shows the snapshots of the reference design GUI:

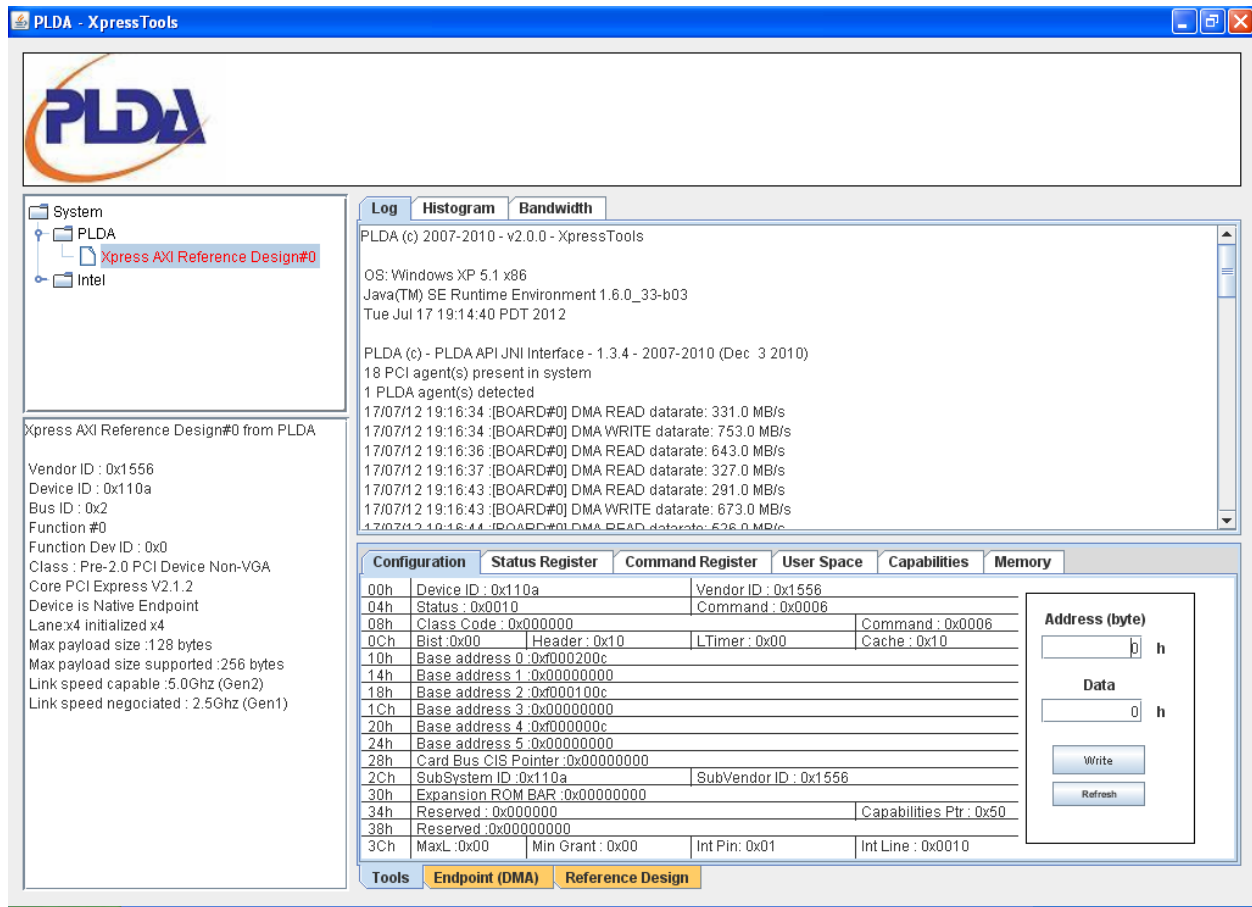


Figure 5 PLDA GUI 01

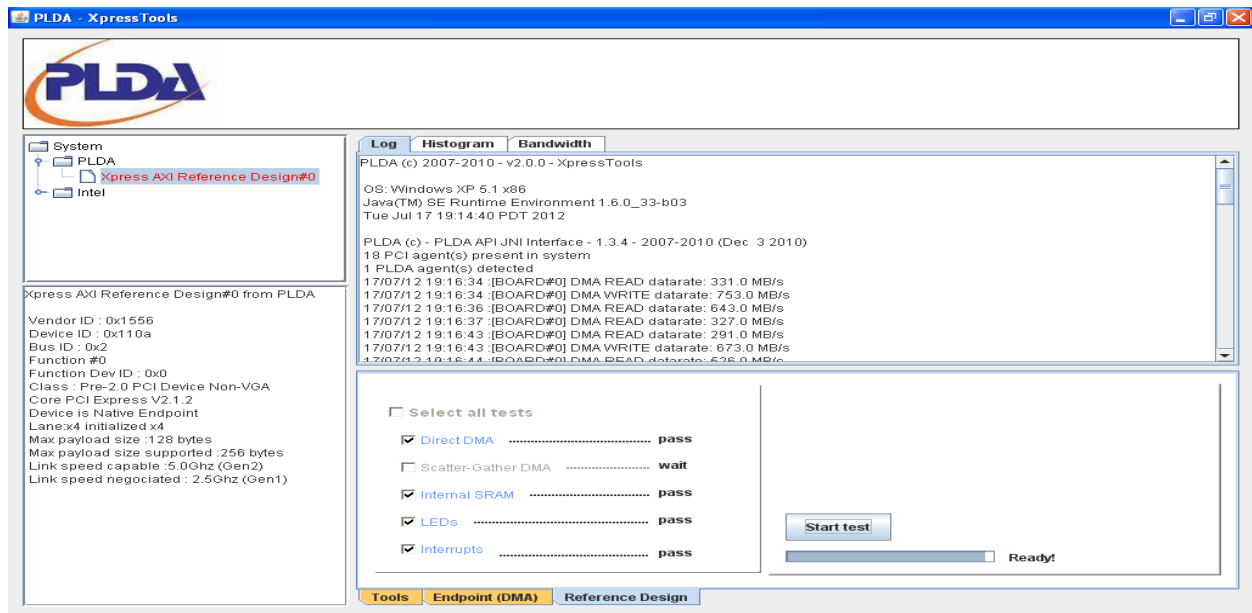


Figure 6 PLDA GUI 02

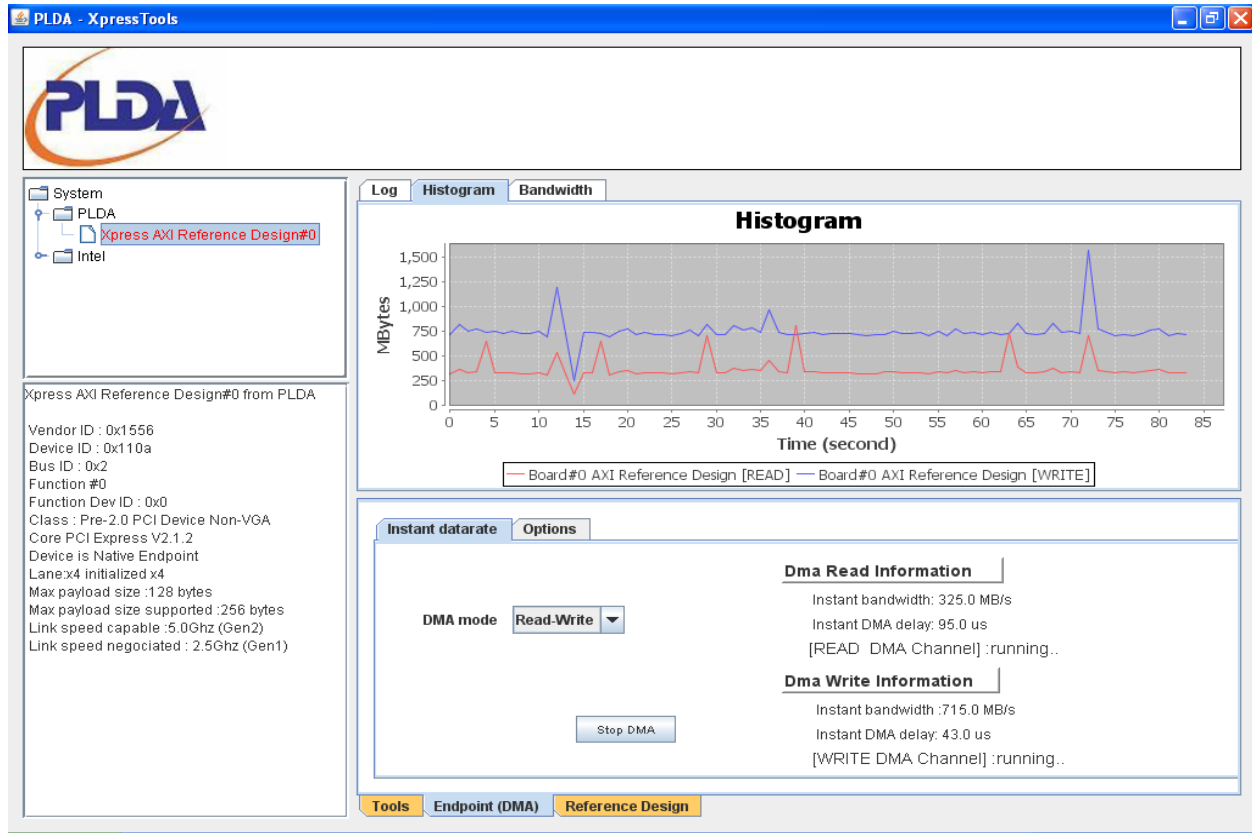


Figure 7 PLDA GUI 03

SERDES0 test cases:

S.No	SERDES	Gen	Lanes	Fabric IF	Board	PCIe Version	Silicon
1	SERDES 0	GEN2	X4	AXI	Validation Board	2.0	REV A,C
2	SERDES 1	GEN2	X4	AXI	SI board	2.0	REV A
3	SERDES 0	GEN1	X1	AXI	Validation Board	2.0	REV A,B
4	SERDES 0	GEN1	X2	AXI	Validation Board	2.0	REV B
5	SERDES 0	GEN1	X4	AXI	SI board	2.0	REV A
6	SERDES0	GEN2	X4	AXI	SI board	2.0	REV A
7	SERDES0	GEN1	X4	AXI	Validation Board	2.0	REV A,B

Design database for

S.No 1 is at:

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For REV A

svn://hoppin/IP/PDV/G4_MAIN/G4M_SERDES/PCIe/tags/1.0.103/design/hw/AXI/Ref_design/GEN1/AXI_X4_VBRD_GEN2.zip

For REV C

svn://hoppin/IP/PDV/G4_MAIN/G4M_SERDES/PCIe/tags/1.0.110/design/hw/AXI/Ref_design/GEN2/AXI_X4_VBRD_GEN2.zip

S.No2 is at:

svn://hoppin/IP/PDV/G4_MAIN/G4M_SERDES/PCIe/tags/1.0.103/design/hw/AXI/Ref_design/GEN1/AXI_X4_SI_GEN2.zip

S.No3 is at:

svn://hoppin/IP/PDV/G4_MAIN/G4M_SERDES/PCIe/tags/1.0.104/design/hw/AXI/Ref_design/GEN1/AXI_X1_VBRD_GEN1.zip

S.No4 is at:

svn://hoppin/IP/PDV/G4_MAIN/G4M_SERDES/PCIe/tags/1.0.104/design/hw/AXI/Ref_design/GEN1/AXI_X2_VBRD_GEN1.zip

S.No5 is at:

svn://hoppin/IP/PDV/G4_MAIN/G4M_SERDES/PCIe/tags/1.0.104/design/hw/AXI/Ref_design/GEN1/AXI_X4_SI_GEN1.zip

S.No6 is at:

svn://hoppin/IP/PDV/G4_MAIN/G4M_SERDES/PCIe/tags/1.0.104/design/hw/AXI/Ref_design/GEN1/AXI_X4_SI_GEN2.zip

S.No7 is at

svn://hoppin/IP/PDV/G4_MAIN/G4M_SERDES/PCIe/tags/1.0.104/design/hw/AXI/Ref_design/GEN1/AXI_X4_VBRD_GEN1.zip

SERDES 1 test cases:

S.No	SERDES	Gen	Lanes	Fabric IF	Board	PCIe Version	Silicon
1	SERDES 1	GEN2	X4	AXI	Validation Board	2.0	REVB
2	SERDES 1	GEN1	X2	AXI	Validation Board	2.0	REVB

Note: In order to validate the SERDES1 on board we need to connect the PCIe daughter board to P1 on the board. The daughter board has the male PCIe edge connector, this edge connector is hooked to PC via the PCIe cable.

Design database for GEN2 is at:

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svn://hoppin/IP/PDV/G4_MAIN/G4M_SERDES/PCIe/tags/1.0.114/design/hw/AXI/Ref_design/GEN2/SERDES1

Design database for GEN1 is at:

svn://hoppin/IP/PDV/G4_MAIN/G4M_SERDES/PCIe/tags/1.0.114/design/hw/AXI/Ref_design/GEN1/SERDES1

6.2.3 Hardware Information (M2S025):

The design is configured as: AXI, GEN2, Lane X4, and SERDES 0. Validation board is used for PCIe validation.

Hardware database is at:

svn://hoppin/IP/PDV/G4_MAIN/G4M_SERDES/PCIe/trunk/design/hw/AXI/Ref_design/GEN2/REVC/AXI_X1_GEN2_11_1_2_16_Eval_Kit.zip

Database with CoreResetP_0 v5.0.103 is at:

svn://hoppin/IP/PDV/G4_MAIN/G4M_SERDES/PCIe/trunk/design/hw/AXI/Ref_design/GEN2/REVC/AXI_X1_GEN2_11_2_0_15.zip

Fabric design is running at 125MHz.

6.2.4 Software Information (M2S025):

We have the following software databases for PCIe design:

- 1) IAR firmware: This firmware is developed to access the register interface of SERDES and PCIe controller. APB interface is provided to access the controller register space via CM3 interface. The software design database is in the IAR folder of the zipped folder of the project. i.e. \$Project/AXI_X1_GEN2_11_1_2_16/IAR/

UART1 is used in this design. UART is configured at 57600.

Notable changes in the modules used are:

- SERDES Version 1.1.108 (to validate the ECPS_RSTN_SEL default value fix)
- CoreResetP_0 Version 5.0.1 (To validate the core reset and power sequence fix)
- CoreResetP_0 Version 5.0.103 (latest version of the Core, project database #2)

6.3 Use Model 3 AHB Use Cases:

All the designs are validated on validation board.

SERDES 0:

S.No	SERDES	Gen	Lanes	Fabric IF	Board	PCIe Version	Silicon
------	--------	-----	-------	-----------	-------	--------------	---------

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1	SERDES0	GEN2	X4	AHB	Validation Board	2.0	REV B
2	SERDES0	GEN1	X2	AHB	Validation Board	2.0	REV B

The soft IPs which are used in the above designs are

COREAXITOAHL: Version 2.0.112,

COREAHLTOAXI: Version 2.0.110 but the RTLs are copied from the tag 2.0.105

Though the version says 2.0.110 for AHLTOAXI, the RTLs are copied from the Tag 2.0.105 because of the issues with soft IPs ([SAR 43332](#))

SERDES 1:

S.No	SERDES	Gen	Lanes	Fabric IF	Board	PCIe Version	Silicon
1	SERDES1	GEN2	X1	AHB	Validation Board	2.0	REV C
2	SERDES1	GEN1	X4	AHB	Validation Board	2.0	REV C

For SERDES 0 and SERDES1 the designs are at:

GEN2: Hardware project is at design

svn://hoppin/IP/PDV/G4_MAIN/G4M_SERDES/PCIe/tags/1.0.113/design/hw/AHB/Ref_design/GEN2

GEN1: Hardware project is at design

svn://hoppin/IP/PDV/G4_MAIN/G4M_SERDES/PCIe/tags/1.0.113/design/hw/AHB/Ref_design/GEN1

Firmware for both projects is at design\fw\IAR.zip

Results are in the results with the respective names.

```

COM3:57600baud - Tera Term VT
File Edit Setup Control Window Help
Welcome to SERDES Configurator CLI 3.4a
*****
Version: Change (Author)
3.4c: Changed the Deemphasis Sequence (PS)
3.4b: Added Enable FLR and force GEN1 custom functions (PS)
3.4a: Support only xl for PMA_READY and SoftReset (PS)
3.4: Lane access bug fix for the Run Mesoloopback GEN1/2 (PS)
3.3: Lane access bug fix, lane0-3 dump (PS)
3.2: Old CMSIS with Work-Around for new CMSIS (PS)
3.1: Added Menu items 7&8 (PS)
*****
Reading the Device Status
Reading the Factory bit for GENERATION Status
Factory and Design both are set to GEN2
Waiting for the PMA ready of all lanes
Checking for only Lane 0 as this desing in configured in Lane 0 Only
PMA is ready
Work-around for SAR 47003 - Documentation update required for FLR support in th
Disabling Function Level reset ...
re-setting bit17 in POWER_MGT_CAPABILITY register
AND MASK = 0xffffdfff
POWER_MGT_CAPABILITY = 0x48018001
Work-around for SAR 46675 - TX De-emphasis default values for PCIe Gen2 do not
Lane0: After swapping De-emphasis levels for GEN2 ...
reg20 : Tx Post-Cursor ratio with TxDeemp=0, Full swing (RW) : 0x20
reg22 : Tx Post-Cursor ratio with TxDeemp=1, Full swing (RW) : 0x15
reg36 : Tx Post-Cursor ratio with TxDeemp=0, Half swing (RW) : 0x20
reg38 : Tx Post-Cursor ratio with TxDeemp=1, Half swing (RW) : 0x15
Increase the rx_idle_max from 0x4 to 0xF
p_pcie_regs->lane[0].RXIDLE_MAX_ERRCNT_THR = 0x48
p_pcie_regs->lane[0].RXIDLE_MAX_ERRCNT_THR = 0xf8
1. Configure the registers manually
2. Auto configure the registers
3. Reading Lane registers
4. Reading Core space Registers and configuring AXI Window registers
5. PHY and Core Reset Assert
6. PHY and Core Reset Deassert
7. Run Mesoloopback GEN1
8. Run Mesoloopback GEN2
9. Read Systems space, LANE and Core Reggisters
10. Enable Function Level Reset
11. Force GEN1
13. Enable DebugKey

```

6.4 Use Model 4 PCIe Compliance Tests and Other Tests:

6.4.1 PCIe Use Model Results:

svn://hoppin/IP/PDV/G4_MAIN/G4M_SERDES/PCIe/tags/1.0.111/results

6.4.2 PCIe Compliance Results:

svn://hoppin/IP/PDV/G4_MAIN/G4M_SERDES/PCIe/tags/1.0.104/results/Compliance_results

6.4.3 PCIe Details and Additional Results:

PTC golden test suite passed for both GEN1 and GEN2. Exhaustive test cases are failing.

PCIe CV test cases are passing after doing a fix in the Fabric logic.

Hot reset issue Fix: Implemented the code in the Fabric logic which asserts the reset to the PCIe core by sniffing the LTSSM signals from PRDATA bus.

Introduced 5 cycles (125MHz) of reset when the LTSSM is changed to Detect. Quite state after the Hot reset state. This fix is validated for both GEN1 and GEN2 PCIECV test cases.

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Link Enable/Disable: The same logic which is implemented for the hot reset is implanted for Link Enable/Disable. Here also the reset is applied in Detect. Quite state but the entry to the Detect. Quite state is from the Link Enable/Disable state. With this fix we still see 3 test cases are failing.

After tuning the PHY register02 (RX_IDLE) all the PCIE CV test cases are passing in GEN2 mode without any issues. The register value is set to 0xF8

The default value is 0x48.

The design database for the hot reset and Link Enable/disable issue is at

svn://hoppin/IP/PDV/G4_MAIN/G4M_SERDES/PCIe/tags/1.0.111/design/hw/AXI/Ref_design/GEN2/REV_C/AXI_X1_G2_11_0_0_23_SB_PClcCoreResetFix6.zip

svn://hoppin/IP/PDV/G4_MAIN/G4M_SERDES/PCIe/tags/1.0.111/design/hw/AXI/Ref_design/GEN2/REV_C/AXI_X1_G2_11_0_0_23_SB_PClc_DLUPExit_01.zip

IAR project is in the same Hardware project with the name "IAR". These designs are configured with ACTEL Device ID.

Both the designs are working fine, all the PCIE CV compliance test cases are passing in X1 and X4. Also verified the PTCII golden suite with the modified design.

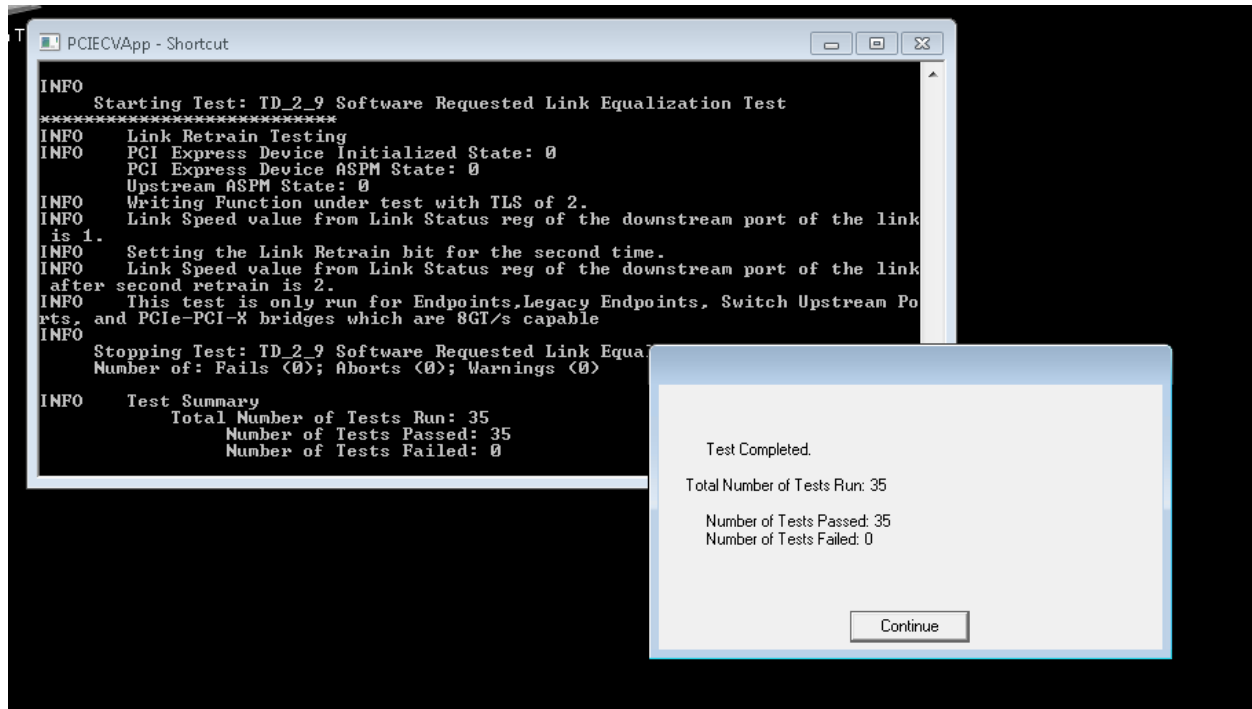
All the Golden suite test cases are passing.

For hot reset and Link enable/Disable Libero Canvas looks:

The screenshot displays a digital design tool interface with the following components and panels:

- Design Hierarchy:** Shows a tree structure with 'work' as the root, containing 'XTL0SC_FAB (osc_comps.v)', 'RCOSC_1MHZ_FAB (osc_comps.v)', 'AXI_SB_top', and 'COREAPP3_LIB'.
- Design Flow:** Lists steps such as 'Create Design', 'System Builder', 'Configure MSS', 'Create SmartDesign', 'Create HDL', 'Create SmartDesign Testbench', 'Create HDL TestBench', 'View/Configure Firmware Cores', 'Verify Pre-Synthesized Design', 'Simulate', 'Create Constraints', 'I/O Constraints', and 'Timing Constraints'.
- Schematic Diagram:** Features three main blocks:
 - SERDES_IF_0:** Inputs include CORE_RESET_N, PHY_RESET_N, APB_S_PRESET_N, CLK_BASE, APB_S_PCLK, POE_INTERRUPT[3:0], and PADs_IN. Outputs include POE_SYSTEM_INT, PLL_LOCK_INT, PLL_LOCKLOST_INT, SPLL_LOCK, POE_EV_IUS, APB_S_PRDATA[31:0], APB_S_PRDATA[30:28], and PADs_OUT.
 - Reset_assertion_0:** Inputs include CLK, RST_N, PSELx, PWRITE, and PULSE_WIDTH[31:0]. Outputs include PCIe_coreset_n.
 - AXI_SB_top_debug_0:** Inputs include CLK, RST_N, PSELx, PWRITE, and PRDATA[31:0]. Outputs include PLLs_Locked_entry_p, LTSSM_L0_entry_p, LTSSM_HotReset_entry_p, LTSSM_DetectQuiet_entry_p, PLLs_Locked_ext_p, LTSSM_L0_ext_p, LTSSM_HotReset_ext_p, LTSSM_DetectQuiet_ext_p, LTSSM_Disabled_entry_p, LTSSM_Disabled_ext_p, hotrst_exit_sync_pulse_extend_f, and dlpul_exit_pulse_extend_f.
- Log Panel:** Contains messages such as 'Reading file 'dcrambe_upper32bit.v'', 'Reading file 'testbench.v'', 'Reading file 'dcrambe_upper32bit_dcrambe_upper32bit_0_IFSRAM.v'', 'Reading file 'axi_direct_mm_ma.v'', 'Reading file 'AXI_SB_top_debugmodule.v'', and 'Reading file 'dma_mgt.v''. It also includes search options like 'Find:', 'Next', 'Previous', 'Find All', and 'Search in:'.
- Status Bar:** Shows 'Fam: SmartFusion2', 'Die: M2050T', 'Pkg: 896 FBGA', and 'Verilog'.

6.4.4 PCI-CV Test Results:



NOTE: while configuring the PCI-CV test, the option for running “Test against 2.0 or 2.1 Spec” must be chosen to ensure that all 35 test cases are run. If the option for just 2.0 is selected, only 29 test cases will be executed.

Database for results:

[PCI-CV TEST RESULTS M2S025](#)

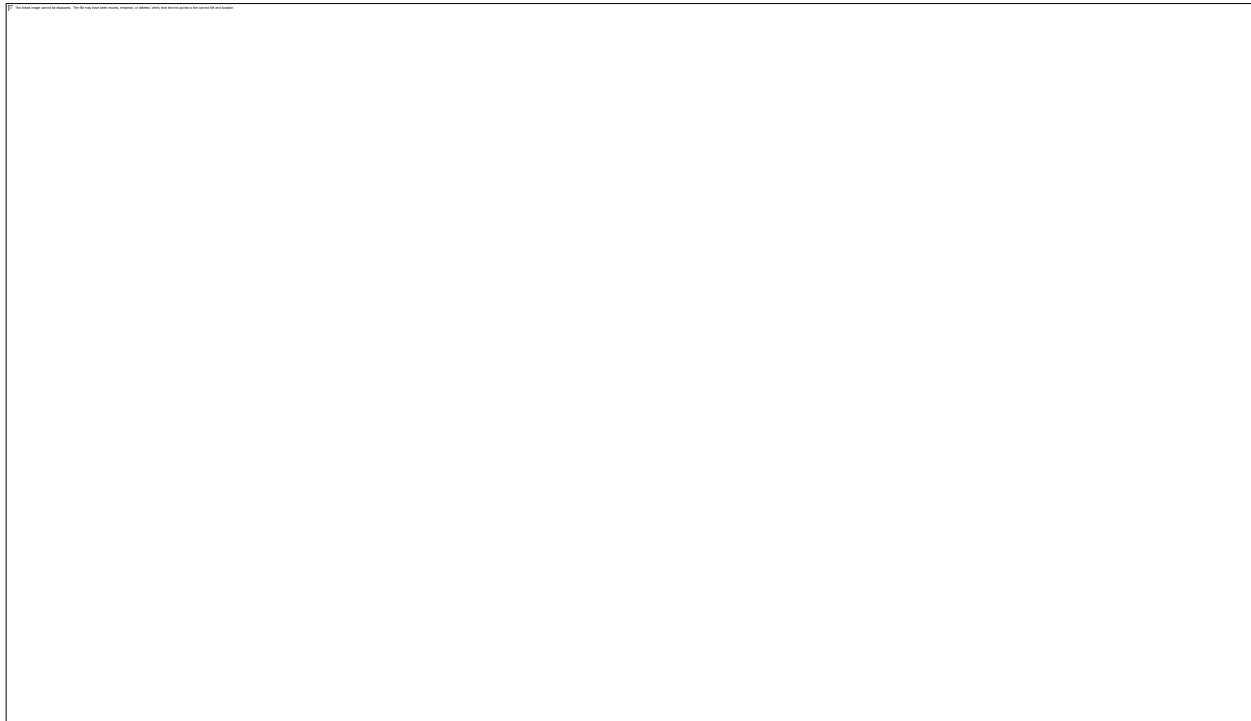
PTC-II:

The document generated by the Agilent Exerciser is stored in Livelink that can be accessible from the link below:

[PTC PCIe GEN2 REVC M2S025 10 23 2013 PASS](#)

6.4.5 Arbor Results (M2S025):

Arbor is a tool by Mindshare that we use to detect the peripherals that we have in the system and we can use it to read/write values onto the PCIe-End Point.



Arbor Results with CoreResetP_0 v5.0.103:

PCI				
B.D.F	Class	Device Description	Device Type	Capabilities
0:0:0	Host bridge	Intel Corporation 2nd Generation Core Processor Family DRAM Contro...		VndrSptc (09h).
0:1:0 (0,1,1)	PCI/PCI bridge	Intel Corporation Xeon E3-1200/2nd Generation Core Processor Famil...	Root Port	PwrMgmt (01h), SubVID (0Dh), MSI (05h), PCIe (10h), VC (0002h), RC...
0:2:0	VGA controller	Intel Corporation 2nd Generation Core Processor Family Integrated Gr...		MSI (05h), AdvFtrs (13h), PwrMgmt (01h).
0:6:0 (0,2,2)	PCI/PCI bridge	Intel Corporation Xeon E3-1200/2nd Generation Core Processor Famil...	Root Port	PwrMgmt (01h), SubVID (0Dh), MSI (05h), PCIe (10h), VC (0002h), RC...
0:22:0	Communications device	Intel Corporation 6 Series/C200 Series Chipset Family MEI Controller ...		PwrMgmt (01h), MSI (05h).
0:22:2	Mass storage controller	Intel Corporation 6 Series/C200 Series Chipset Family IDE-r Controller		PwrMgmt (01h), MSI (05h).
0:22:3	16850 serial controller	Intel Corporation 6 Series/C200 Series Chipset Family KT Controller		PwrMgmt (01h), MSI (05h).
0:25:0	Ethernet controller	Intel Corporation 82579LM Gigabit Network Connection		PwrMgmt (01h), MSI (05h), AdvFtrs (13h).
0:28:0	USB EHCI	Intel Corporation 6 Series/C200 Series Chipset Family USB Enhanced...		PwrMgmt (01h), Debug (0Ah), AdvFtrs (13h).
0:27:0	Mixed mode device	Intel Corporation 6 Series/C200 Series Chipset Family High Definition...	RC Integrated Endpoint	PwrMgmt (01h), MSI (05h), PCIe (10h), VC (0002h), RCLnID (0005h).
1! 0:28:0 (0,3,3)	PCI/PCI bridge	Intel Corporation 6 Series/C200 Series Chipset Family PCI Express Ro...	Root Port	PCIe (10h), MSI (05h), SubVID (0Dh), PwrMgmt (01h).
1! 3:0:0	Non-VGA compat device	PLD APPLICATIONS Unknown	PCIe Endpoint	MSI (05h), PwrMgmt (01h), PCIe (10h), VC (0002h), AdvErr (0001h).
0:28:4 (0,4,4)	PCI/PCI bridge	Intel Corporation 6 Series/C200 Series Chipset Family PCI Express Ro...	Root Port	PCIe (10h), MSI (05h), SubVID (0Dh), PwrMgmt (01h).
0:28:6 (0,5,5)	PCI/PCI bridge	Intel Corporation 6 Series/C200 Series Chipset Family PCI Express Ro...	Root Port	PCIe (10h), MSI (05h), SubVID (0Dh), PwrMgmt (01h).
0:29:0	USB EHCI	Intel Corporation 6 Series/C200 Series Chipset Family USB Enhanced...		PwrMgmt (01h), Debug (0Ah), AdvFtrs (13h).
0:30:0 (0,6,6)	Sub PCI/PCI bridge	Intel Corporation 82801 PCI Bridge		SubVID (0Dh).
0:31:0	ISA bridge	Intel Corporation C200 Chipset Family LPC Controller		VndrSptc (09h).

6.4.6 1V Test Cases:

There are several test cases executed for 1.0V operation. The detailed report is

svn://hoppin/IP/PDV/G4_MAIN/G4M_SERDES/PCIe/tags/1.0.113/design/hw/AXI/1V_testcases/SERDES_1.0vs1.2V.xlsx

Summary: It has been observed that GEN1 designs are passing without any issues in 1.0V mode of operation. GEN2 SERDES does not operate at 1.0V.

Please see the SAR also for more details: [SAR 48031](#)

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Please refer to the document which is at:

PCIE_PERSTN_L2P2_workarounds_results.docx**7. Results Summary****SERDES0 Validation Summary:**

S.No	Use Model	Use case	Target date	Current	Actual	Comments
1	PCIE Compliance test cases	GEN1 TX compliance test cases	6/27/12	8/28/12	8/28/12	Done
2		GEN1 RX loopback TX test cases	6/27/12	8/28/12	8/28/12	Done
3		GEN2 TX compliance test cases	6/27/12	8/28/12	8/28/12	Done
4		GEN2 RX loopback TX test cases	6/27/12	8/28/12	8/28/12	Done
5		GEN1 Protocol compliance test cases (Golden Suite)	6/27/12	8/28/12	8/28/12	Done
6		GEN2 Protocol compliance test cases (Golden Suite)	6/27/12	8/28/12	8/28/12	
7		GEN1 Protocol compliance exhaustive test cases	12/20/12	04/22/14 -> 04/29/2014	04/29/2014	Done – TLP passes; DLP passes, Config Space passes

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8		GEN2 Protocol compliance exhaustive test cases	12/20/12	04/22/14 -> 04/29/2014	04/29/2014	Done– TLP passes; DLP passes, Config Space passes
9	Reference Design test cases	SERDES Space accessing via APB interface			Phase I	Done
10		Config space accessing via Link			Phase I	Done
11		GEN1 AXI_X4			Phase I	Done
12		GEN1 AXI_X4_revers e			Phase I	Done
13		GEN1 AXI_X2			Phase I	Done
14		GEN1 AXI_X1			Phase I	Done
15		GEN1 AXI_X1_revers e	11/14/12	12/5/12	03/07/14	DONE- Leverage UC19
16		GEN2 AXI_X4	11/14/12	12/5/12	11/26/12	Done
17		GEN2 AXI_X2_revers e	11/14/12	12/5/12	03/07/14	DONE- on M2S090 Silicon !
18		GEN2 AXI_X1	11/14/12	12/5/12	11/26/12	Done
19		GEN2 AXI_X1_revers e	11/14/12	12/5/12	03/07/14	DONE- on M2S090 Silicon !
20		GEN1 AHB_X4	11/14/12	12/5/12	12/7/12	Done
21		GEN2 AHB_X2	11/14/12	12/5/12	12/7/12	Done

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22	PCIe Advanced Use Models	L2/P2 Power Entry and exit with F*F	3/20/2013	4/8/2013	03/01/14	<p>DONE on M2S090 Silicon – DONE (Seen ext table)</p> <p>L2P2 Use model.docx</p>

SERDES1 Validation Summary

S.No	Use Model	Use case	PHASE	Target date	Current	Actual	Comments
1	PCIe Use cases	GEN2 AXI_X4	Phase II	1/7/13	1/29/2013	1/29/2013	SI Done
2		GEN2 AHB_X1	Phase II	1/7/13	1/29/2013	1/29/2013	Libero Design is Done
3		GEN1 AXI_X2	Phase II	1/7/13	1/29/2013	1/29/2013	SI Done
4		GEN1 AHB_X4	Phase II	1/7/13	1/29/2013	1/29/2013	Libero Design is Done

SERDES Mixed Mode Validation Summary

S.No	Use Model	Use case	PHASE	Target date	Current	Actual	Comments
1	SERDES Multiprotocol Mode	PCIe GEN1 in X2 and SGMII	Phase II	12/24/2013	2/1/2013	29/1/13	Pass
2		PCIe GEN2 X1 and SGMII	Phase II	12/24/2013	2/1/2013	30/1/13	Pass

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SAR	Description	Version Found	Version Resolved
36853	Auto connect option is not enabled for SERDES_IF and FDDR Interface	10.8.0.15	Duplicate of 37053
37045	SERDES IF: Reference clock selection for PCIe	10.8.0	10.8.1.2
37051	SERDES: Need to revisit the PCIe Speed Tab selections	10.8.0	11.0 Beta (10.9.1.26)
37053	SYSBLD:: Support DirectConnections for AXI Bus Interfaces	10.8.0	Duplicate of 33504
37716	Few registers are missing in the pcie_regs.h	3.3.0	Version 0.6.1 of G4Main PCIe firmware package
37778	SERDES: PERI_INIT: EPCS mode needs extensive APB initialization of entire X register from scratch	10.8.1.3	Duplicate of 48265
37870	SERDES: Selection of the SERDES location must be given to USER	10.8.1.3	11.0 Beta (10.9.1.26)
38214	SERDES: REF_CLOCK port is missing in the GUI	10.9.0.3	11.0 Beta (10.9.1.26)
38241	SERDES: Ground FAB_PLL_LOCK Input	10.9.0.3	11.0 Beta (10.9.1.26)
38575	SERDES: Remove PM_AUX_PWR option from GUI	10.9.0.4	11.0 Beta (10.9.1.26)
38808	G4M:SERDES Timing violations	10.9.0.10	11.0 Beta (10.9.1.26)
39061	G4M:SERDES:Simulation issues: Receive RAM is not working	10.9.1.6	Not Reproduced
39062	SERDES:Simulation models: Few signals are not driven properly in the simulation model	10.9.1.6	Not Reproduced
39078	SERDES: Need to double check the INIT string for BAR Configurations	10.9.1.6	11.0 Beta (10.9.1.26)
39098	G4M:SERDES:Simulation delay model issues	10.9.1.6	11.0 Beta (10.9.1.26)
39252	G4M:SERDES: Unable to read the PCIe core registers from APB interface	10.9.1.8	11.0 Beta (10.9.1.26)
39521	PCIe is not set in GEN2 mode	0	Refer to SAR 36494
42981	SERDES designs are not working when migrated to the latest Libero versions	10.9.2	10.9.3.5
43040	MSS CCC incorrect setting for FACC_SRC_SEL	10.9.2.10	11.0.0.5
43332	PCIe AHB design simulations are not working	0	ECN Release v2.0.112

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45028	SERDES: Looks like BAR configurations are wrong	10.9.3.15	11.0.0.15
47414	SynplifyPro ME G2012.09MSP1 does not synthesize code correctly	Test Build	Obsolete Version
48414	SERDES: Changes in the EPCS_RSTN_SEL INIT string for M2S010T	11.1.0	11.1.0.14

Against Silicon

SAR	Description	Detected Phase	Issue Revision Number
39521	PCIe is not set in GEN2 mode	Pre-ES Post-Mask Making	Rev A
45548	PCIe BAR setting shifted by 1 bit in the RTL	Pre-MRR Post-C or B QuaL	Rev C
45581	32-bit BAR SIZE reduced from 2GB to 1GB !	Pre-MRR Post-C or B QuaL	Rev C
46675	TX De-emphasis default values for PCIE Gen2 do not comply with PIPE	Pre-ES Post-Mask Making	Rev D
46880	PCIE-CV Test Failures	Pre-C or B QuaL Post-ES	Rev C
47003	Documentation update required for FLR support in the PCIe core.	Pre-C or B QuaL Post-ES	Rev D
47796	SERDES_IF2: Increase the default rx_idle_max from 0x4 to 0xF	Pre-release	Rev D
48031	SERDES does not work in 1.0V	Pre-MRR Post-C or B QuaL	Rev D
48032	Live probe issues when we press the press button(DEVRST) on the board	Pre-C or B QuaL Post-ES	Rev D
48468	G4M SERDES PCIE: PERST work arounds	Pre-C or B QuaL Post-ES	Rev D