



# **G4M-MDDR Verification and Validation Report**

Revision: 1.0

Date: September 12<sup>th</sup>, 2014

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### Revision History

Version	Date	Modified by	Changes
0.1	9 <sup>th</sup> October 2012	SM	Initial Version
0.2	31 <sup>st</sup> Jan 2013	SM	Added validation result of A4P5000 Phase-II
0.3	6 <sup>th</sup> Feb 2014	SM	Added validation results of M2S090 in Chapter 4
0.4	14 <sup>th</sup> Feb 2014	SM	Added Dev-Kit board restriction note to chapter 2.1
0.5	19 <sup>th</sup> Feb 2014	SM	Added validation results of LPDDR of M2S090 in chapter 4.2(i.e: added 4.2.5 till chapter 4.2.8)
0.6	12 <sup>th</sup> Sep 2014	SW	Created Report version
1.0	12 <sup>th</sup> Sep 2014	Mktg SW KO	Finalized for customer distribution

## Glossary

Term	Description
LIN	Local Interconnect Network
Use Case	A specific configuration of a use model.
Use Model	A reference platform designed from configurable h/w and s/w components, which is targeted at a focused application. The use model demonstrates one of several possible ways of integrating IPs to build a system and one of several ways in which it could be used by the customer.
ISR	Interrupt Service Routine – Subroutine executed as a result of an IRQ
MMUART	Multi-Mode Universal Asynchronous Receiver Transmitter
G4	4th Generation Flash chip from Microsemi
Frame	All LIN information is transmitted packed as frames; a frame consists of a header and a response

## REFERENCES

1. [G4M MDDR PDV PLAN.docx](#)
2. [G4M MDDR PDV Results.docx](#)

## 1 Introduction

This document explains the design of and execution of validation result of various A4P5000 MDDR PDV Phase-I usecases executed on Validation Board.

### *1.1 Purpose and Scope*

The purpose of this document is to describe the G4 MDDR as well as its plans and tests that are performed as a part of silicon validation and verification. All UseCases are elaborated upon and reports of issues during verification are documented. This document is to provide a holistic view of the verification and validation process.

### *1.2 Standards and Requirements*

The Design team and the Verification and Validation Team have different reporting structures that are independent of one another.

## 2 G4M MDDR SubSystem back ground

The DDR Interface encapsulates the DDR Controller IP from VirageLogic with an AXI Wrapper that allows it to be attached to an AXI Interconnect at the core side.

The AXI Interface receives read and write requests from an AXI Interconnect and schedules them to the Memory Controller that in turn drives the DDR. The Interface supports transactions in accordance with the standard AXI protocol. There are two AXI slave ports one for the Bridge block (i.e. MSS) and one for the Fabric each supporting up-to 4 outstanding transactions.

There is an additional APB Interface that is used to program the DDR Register-Set. Majority of the registers of the DDR Controller need to be programmed when the controller is in reset and hence do not require any special handling. Few of the registers can be programmed dynamically i.e. when the controller is in operation and these are synchronized to the controller clock domain.

It is assumed that AXI and APB clocks can run asynchronous to each other and CDC has been implemented accordingly.

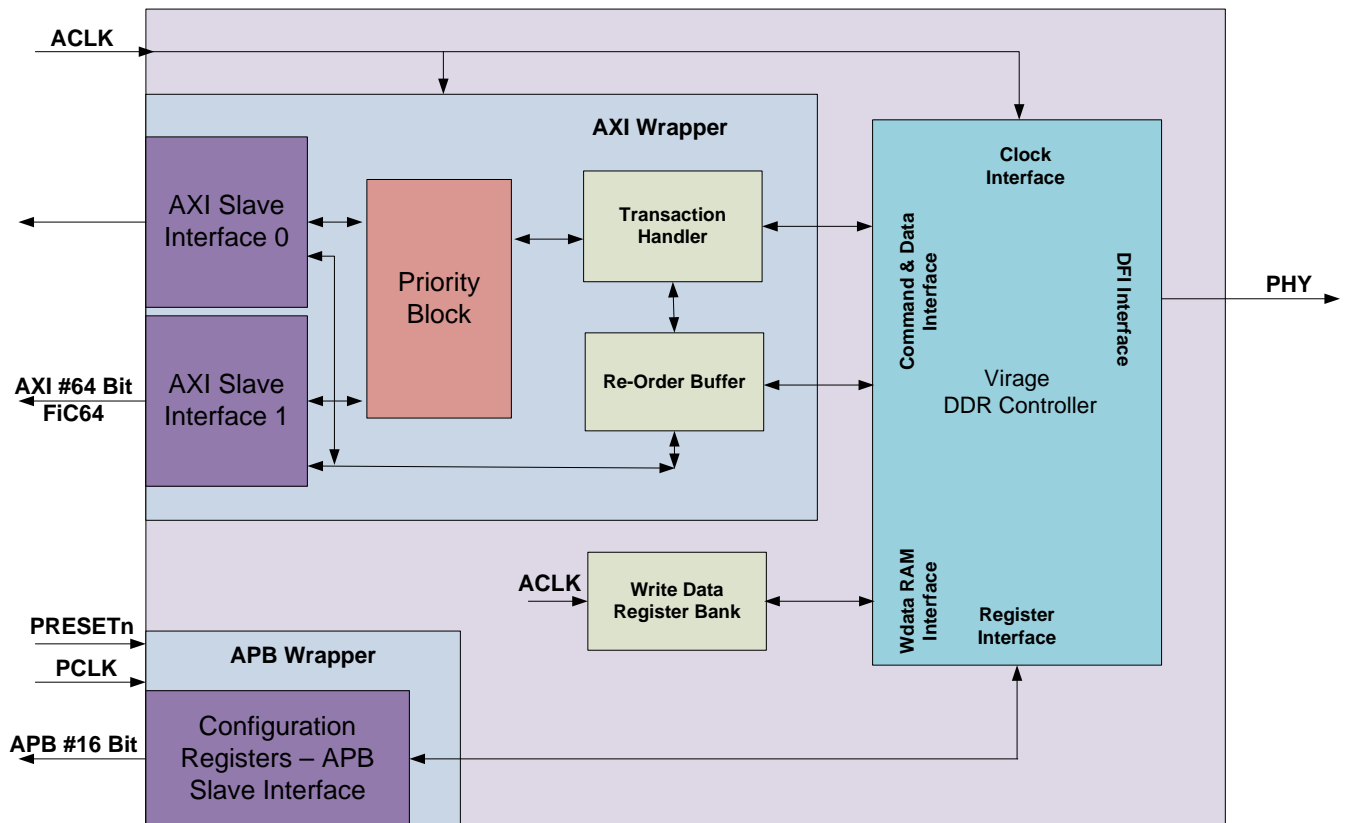


Figure 1 : DDR Interface Block Diagram

### 3 Use Models & Use Cases Design Phase

#### 3.1 MDDR Validation Setup

In order to validate the MDDR interface following DDR parts are planned to be used

LPDDR	MT46H32M16LFBF-6 IT:C TR	x 36	512M	166Mhz	32M x 16	1.8V	2 ICs + 1 IC for ECC
DDR1	MT46V64M8P-6T:F TR	x 36	512M	166MHz	64M x 8	2.5V	4 ICs + 1 IC for ECC
DDR2	MT47H128M8CF-25:H TR	x 36	1G	400MHz	128M x 8	1.8V	4 ICs + 1 IC for ECC
DDR3	MT41J256M8HX-15E:D TR	x 36	2G	667MHz	256M x 8	1.5V	4 ICs + 1 IC for ECC

Following clock frequency ratios will be used for DDR validation

Timing Mode	FDDR clk_ddr:clk freq (MHz)	MSSDDR clk_ddr:clk freq (MHz)
tm1	166:166	153:153
tm2	333:166	306:153
tm3	333:111	333:111

For details on the DDR connection to the G4Main mezzanine connector refer DDRx custom DIMM schematics available at [G4 Main Validation Platform](#)

#### 3.2 UseCases

UseModel	Feature validation under	Description
UseCase1	MDDR-DDR2 Provisioning	MSS is the master for the APB configuration of the MDDR. Configure DDR2 by writing to the relevant configuration registers and verify that the controller is configuring the DDR and moved to Normal mode.
UseCase2	MDDR-DDR3 Provisioning	MSS is the master for the APB configuration of the MDDR. Configure DDR3 by writing to the relevant configuration registers and verify that the controller is configuring the DDR and moved to Normal mode.
UseCase3	MDDR-LPDDR Provisioning	MSS is the master for the APB configuration of the MDDR. Configure LPDDR by writing to the relevant configuration registers and verify that the controller is configuring the DDR and moved to Normal mode.
UseCase4	DDR2 ScratchPad memory	Perform read/write access to DDR2 memory using following pattern  Sequential Walking-1

UseModel	Feature validation	under	Description
			Walking-0 Simultaneous toggling of all datalines Perform the read write access through HPDMA and CM3
UseCase5	DDR3 ScratchPad memory		Repeat usecase4 for DDR3
UseCase6	LPDDR ScratchPad memory		Repeat usecase4 for DDR3
UseCase7	Remapping to DDR2		Remapping is done to DDR2 to execute the application from DDR2 and verify that the application executed successfully. Use UART terminal display application for execution
UseCase8	Remapping to DDR3		Remapping is done to DDR3 to execute the application from DDR3 and verify that the application executed successfully.
UseCase9	Remapping to DDR4		Remapping is done to LPDDR to execute the application from LPDDR and verify that the application executed successfully.
UseCase10	Dhrystone test with remapping to DDR2		Remapping is done to DDR2, cache is turned ON, DDRB WCB and read buffering is ON and DDR2 is running in BL-8 mode and measure the Dhrystone performance.
UseCase11	Dhrystone test with remapping to DDR3		Remapping is done to DDR3, cache is turned ON, DDRB WCB and read buffering is ON and DDR3 is running in BL-8 mode and measure the Dhrystone performance.
UseCase12	Dhrystone test with remapping to LPDDR		Remapping is done to LPDDR, cache is turned ON, DDRB WCB and read buffering is ON and LPDDR is running in BL-8 mode and measure the Dhrystone performance.
UseCase13	Bus Access Modes		Full Bus width and Half Bus width support
UseCase14	Interleaved/sequential Access Mode		Perform read/write access both in sequential and interleaved mode
UseCase15	DDR memory access with ECC ON		Make read write access to DDR2/DDR3 with ECC ON
UseCase16	Burst access		Burst length of 4, 8 and 16
UseCase17	Latency analysis: Read write access to open/closed page		Perform write and read access to closed page and compare the time taken with the time taken to read/write to an open page

UseModel	Feature validation under	Description
UseCase18	Priority test: Multi-master read/write access	Both MDDR and FIC64 are accessing DDR (read & write) and verify the following  Access time comparison: Simultaneous 100 write access from DDRBRIDGE & FIC64  Access time comparison: Simultaneous 100 read access from DDRBRIDGE & FIC64
UseCase19	FDDR: Simultaneous read/write access from AXI read and AXI write channel	To verify that when (ddrc_prefer_write) is set to '0' read access are executed before write  Verify that write access are finished first when ddrc_prefer_write = 1  Need support from FIC64 transactor module for this usecase
UseCase20	Simultaneous read/write access turnaround time	For different value of rdwr_idle_gap make 100 simultaneous write and read access and verify how the read write access are handled and monitor the operation of critical, hard-nocritical condition by defining go2critical_hysteresis values
UseCase21	Self refresh entry and exit conditions	Set the self refresh bit to bring the controller in self refresh mode, controller will be in self refresh mode as soon as the transaction buffers are empty  Exit condition: Make a read /write access
UseCase22	Power down entry and exit conditions	Verify that the controller will move to power down mode after the programmed number of idle cycles  Condition to come out of refresh:  Make a self refresh request  Make a read or write transfer  Clear the power down bit
UseCase23	Changing the clock frequency	Enable the self refresh mode  Wait for the controller to enter the self refresh mode  Change the clock frequency  Bring the controller out of self refresh mode
UseCase24	Loopback test	Set the reg_ddrc_loopback and make a write access.  Verify that the written data is sent back as response read data along with the response loopback address indicating the bank, row and column
UseCase25	Deep powerdown mode	Applicable only to LPDDR.  Enable reg_ddrc_deeppowerdown_en to put the DRAM in deep power down mode when the transaction storage is empty and verify that the operation mode status changes to this mode

UseModel	Feature validation	under	Description
UseCase26	Address handling	collision	New read colliding with queued read New write colliding with queued write New read colliding with queued write New write colliding with queued read New read colliding with both write and read
UseCase27	Code Shadowing		SPI to MDDR
UseCase28	Code Shadowing		NOR Flash to MDDR
UseCase29	EDAC error detection and correction		For the DDR single error and double bit error is generated and verified that on the read access request single error is corrected and double error is detected and a response is generated to indicate the bit error
UseCase30	Soak test for the different memory stress tests (to test DLL reliability etc)		Perform an infinite number of writes and read access to stress test and verify that the DDR writes and reads are successful by verifying the read data.

**Table 1 List of UseCases**

- FDDR: various AXI burst length and burst size and how it will be handled by DDR CTRL

### 3.3 Tool Flow

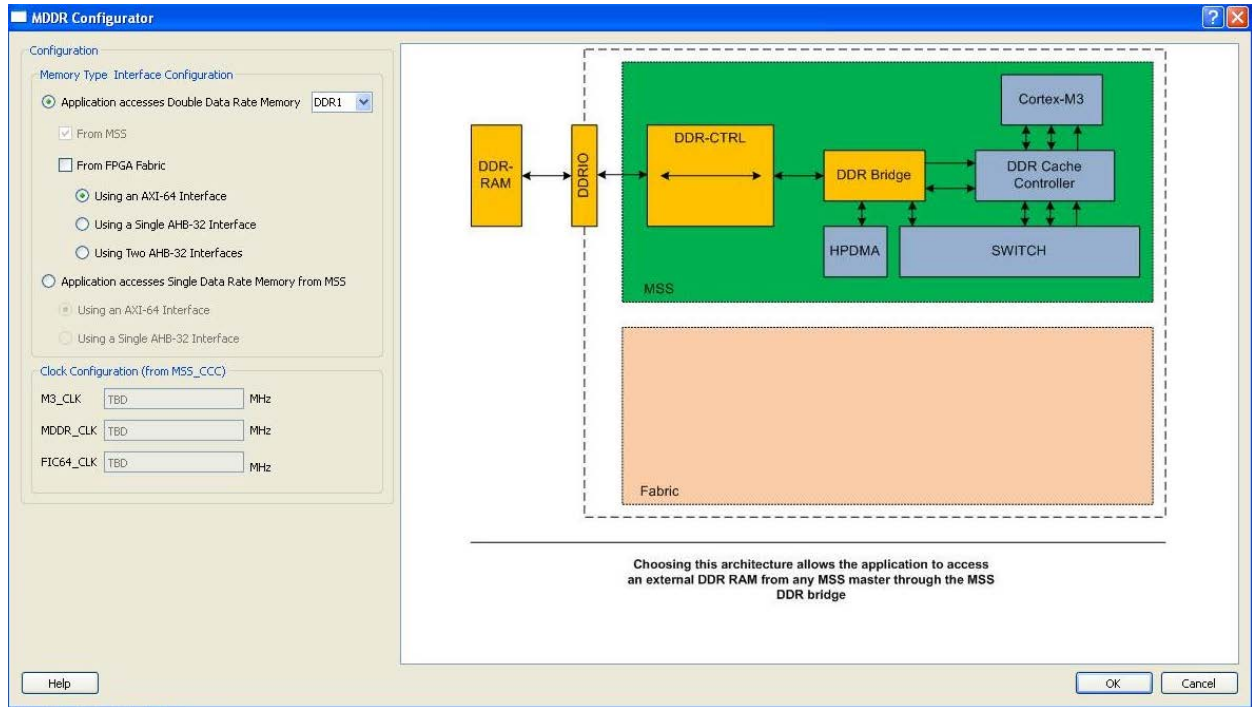


Figure 2 MDDR Configuration

#### **Libero SARs:**

**SAR 36757** - MSS DDR: CLK and DQS IOs shall be differential in designer → For LPDDR the DQS signals shall be single ended IOs, for DDR2/DDR3 is shall be differential

**SAR 37052** - MSS DDR: Unable to change the DDR memory type through GUI → DDR2 reset pin shall be removed, only DDR type definition will not generate initialization sequence on power up

## 4 Equipment Used

### 4.1 Hardware

S.No	Equipment/Board	Qty	Remarks/Serial Number
1	G4M Validation Board	1	DVP-102-000304-001-RevB(labelled-B3) (Socket Board) With Silicon labelled 11(for Rev-A) With Silicon labelled 64(for Rev-B) With Silicon labelled 119(for Rev-C)
2	EWARM Debugger	1	S/No:158006667
3	Flashpro4	1	30000
4	USB to Micro USB cable	1	On G4M Validation board UART0 is connected via fabric to the PC via USB cable.
5	DC Power supply	1	FSP200-50PL-B (12V 5V) is used to power-up the G4M validation board
6	PC	1	Stand-alone PC wxp-svg-09

**Table 2 Hardware Equipment used**

Usecase3a and 3b are validated using RevB silicon (labelled 64)

NOTE: All the usecases are executed on validation board, same usecases can be ported to Dev-Kit or Eval kit.

**Restriction on Dev-Kit: Note that till DevKit Rev-C MDDR-ECC feature is not supported. ECC feature is supported from Rev-D revision on Dev-kit**

### 4.2 Software

UseCase	Libero Capture	MSS	Silicon on Silicon
UseCase1	10.9.1.19	0.0.662	Rev-A
UseCase2	10.9.1.19	0.0.662	Rev-A
UseCase3	10.9.1.22	0.0.665	Rev-A
UseCase4	10.9.1.19	0.0.662	Rev-A
UseCase5	10.9.1.19	0.0.662	Rev-A
UseCase6	10.9.1.22	0.0.665	Rev-A
UseCase7	10.9.1.19	0.0.662	Rev-A
UseCase8	10.9.1.19	0.0.662	Rev-A
UseCase9	10.9.1.22	0.0.665	Rev-A

UseCase10	10.9.1.19	0.0.662	Rev-A
UseCase11	10.9.1.19	0.0.662	Rev-A
UseCase12	10.9.1.22	0.0.665	Rev-A
UseCase13	10.9.1. 19	0.0.662	Rev-A
UseCase14	10.9.1.19	0.0.662	Rev-A
UseCase15	10.9.1.22	0.0.662	Rev-A
UseCase16	10.9.1.22	0.0.662	Rev-A
UseCase17	10.9.3.4	0.0.700	Rev-B
UseCase18	10.9.1.26	0.0.665	Rev-B
UseCase19	10.9.3.10	0.0.720	Rev-C
UseCase20	10.9.3.10	0.0.720	Rev-C
UseCase21	10.9.3.4	0.0.700	Rev-B
UseCase22	10.9.3.4	0.0.700	Rev-B
UseCase23	10.9.3.4	0.0.700	Rev-B
UseCase25	10.9.1.22	0.0.665	Rev-B
UseCase26	10.9.1.22	0.0.662	Rev-A
UseCase27	By apps team	-	-
UseCase29	10.9.1.22	0.0.662	Rev-B
UseCase30	10.9.1.22	0.0.662	Rev-B

**Table 3 Libero Equipment used**

S.No	Tool	Version
1	EWARM(IAR)	Software version 6.0
2	Keil	uVision4

**Table 4 Software Equipment used**

- For MDDR validation G4Mvalidation board-DDR3, DDR2 and LPDDR memory interface is used
- On board Micron memory used:

S.No	MDDR Interface	DDR Memory Model	MSS Frequency	DDR Frequency
1	DDR3	MT41J256M8HX-15E:D TR	111MHz	333MHz
2	DDR2	MT47H128M8CF-25:H TR	111MHz	333MHz
3	LPDDR	MT46H32M16LFBF-6 IT:C TR	166MHz	166MHz



## 5 Use Models & Use Cases Test Phase

### 5.1 UseCase1- APB Configuration of MDDR→DDR2

#### 5.1.1 Deviation from the Validation Plan

None

#### 5.1.2 Implementation Guideline

Remapping is done to ESRAM.

Firmware is used to configure MDDR in DDR2 PHY-32, BL-8 and sequential mode.

#### 5.1.3 Issues

None

#### 5.1.4 PASS or FAIL criterion

Configuration validation is done by polling the status register in firmware.

Verified that status register reflects that MDDR is configured and MDDR is brought to normal mode.

Correctness of configuration is verified by read/write access to DDR2

#### 5.1.5 Observation

[svn://hoppin/IP/PDV/G4\\_MAIN/G4M\\_MDDR/tags/1.0.106/results/Validation\\_Board/VB\\_MDDR\\_DDR2.TXT](svn://hoppin/IP/PDV/G4_MAIN/G4M_MDDR/tags/1.0.106/results/Validation_Board/VB_MDDR_DDR2.TXT)

#### 5.1.6 SVN Database

[svn://hoppin/IP/PDV/G4\\_MAIN/G4M\\_MDDR/tags/1.0.106/design/hw/Validation\\_Board/VB\\_MDDR\\_DDR2\\_111\\_333MHz\\_ODT\\_ON.zip](svn://hoppin/IP/PDV/G4_MAIN/G4M_MDDR/tags/1.0.106/design/hw/Validation_Board/VB_MDDR_DDR2_111_333MHz_ODT_ON.zip)

[svn://hoppin/IP/PDV/G4\\_MAIN/G4M\\_MDDR/tags/1.0.106/design/fw/Validation\\_Board/VB\\_MDDR\\_DDR2\\_UseCase2.zip](svn://hoppin/IP/PDV/G4_MAIN/G4M_MDDR/tags/1.0.106/design/fw/Validation_Board/VB_MDDR_DDR2_UseCase2.zip)

### 5.2 UseCase2- APB Configuration of MDDR→DDR3

#### 5.2.1 Deviation from the Validation Plan

None

#### 5.2.2 Implementation Guideline

Remapping is done to ESRAM.

Firmware is used to configure MDDR DDR3 in DDR3 PHY-32, BL-8 and sequential mode.

#### 5.2.3 Issues

None

#### 5.2.4 PASS or FAIL criterion

Configuration validation is done by polling the status register in firmware.

Verified that status register reflects that MDDR is configured and MDDR is brought to normal mode.

Correctness of configuration is verified by read/write access to DDR3

### **5.2.5 Observation**

[svn://hoppin/IP/PDV/G4\\_MAIN/G4M\\_MDDR/tags/1.0.107/results/Validation\\_Board/VB\\_MDDR\\_DDR3.TXT](svn://hoppin/IP/PDV/G4_MAIN/G4M_MDDR/tags/1.0.107/results/Validation_Board/VB_MDDR_DDR3.TXT)

### **5.2.6 SVN Database**

[svn://hoppin/IP/PDV/G4\\_MAIN/G4M\\_MDDR/tags/1.0.107/design/hw/Validation\\_Board/VB\\_MDDR\\_DDR3\\_111\\_333MHz\\_ODD\\_ON.zip](svn://hoppin/IP/PDV/G4_MAIN/G4M_MDDR/tags/1.0.107/design/hw/Validation_Board/VB_MDDR_DDR3_111_333MHz_ODD_ON.zip)

[svn://hoppin/IP/PDV/G4\\_MAIN/G4M\\_MDDR/tags/1.0.107/design/fw/Validation\\_Board/VB\\_MDDR\\_DDR3\\_UseCase2.zip](svn://hoppin/IP/PDV/G4_MAIN/G4M_MDDR/tags/1.0.107/design/fw/Validation_Board/VB_MDDR_DDR3_UseCase2.zip)

## **5.3 UseCase3- APB Configuration of MDDR→LPDDR**

### **5.3.1 Deviation from the Validation Plan**

None

### **5.3.2 Implementation Guideline**

Remapping is done to ESRAM.

Firmware is used to configure MDDR in LPDDR PHY-32, BL-8 and sequential mode.

### **5.3.3 Issues**

None

### **5.3.4 PASS or FAIL criterion**

Configuration validation is done by polling the status register in firmware.

Verified that status register reflects that MDDR is configured and MDDR is brought to normal mode.

Correctness of configuration is verified by read/write access to LPDDR

### **5.3.5 Observation**

[svn://hoppin/IP/PDV/G4\\_MAIN/G4M\\_MDDR/tags/1.0.107/results/LPDDR/LPDDR\\_VB\\_UC1.TXT](svn://hoppin/IP/PDV/G4_MAIN/G4M_MDDR/tags/1.0.107/results/LPDDR/LPDDR_VB_UC1.TXT)

### **5.3.6 SVN Database**

[svn://hoppin/IP/PDV/G4\\_MAIN/G4M\\_MDDR/tags/1.0.107/design/hw/LPDDR.zip](svn://hoppin/IP/PDV/G4_MAIN/G4M_MDDR/tags/1.0.107/design/hw/LPDDR.zip)

[svn://hoppin/IP/PDV/G4\\_MAIN/G4M\\_MDDR/tags/1.0.107/design/fw/G4M\\_LPDDR\\_VB.zip](svn://hoppin/IP/PDV/G4_MAIN/G4M_MDDR/tags/1.0.107/design/fw/G4M_LPDDR_VB.zip)

## **5.4 UseCase4- DDR2 ScratchPad memory**

### **5.4.1 Deviation from the Validation Plan**

None

### **5.4.2 Implementation Guideline**

Remapping is done to ESRAM.

Firmware is used to configure MDDR in DDR2 PHY-32, BL-8 and sequential mode.

Following data patterns are tested as part of scratchpad memory validation

UseCase1 : Alternate read/write access

UseCase2 : Read only data traffic

UseCase3 : Write only data traffic

READ/WRITE ACCESS MODE:

1. Word (32 bit) Access
2. Half-Word (16 bit) Access

READ/WRITE DATA PATTERN:

1. Incrementing
2. Walking One Pattern
3. Walking Zero Pattern
4. Random Data

UseCase4 : Simultaneous toggling of all data lines

Simultaneous DATA Toggling pattern:

1. 0xAAAA5555, 0x5555AAAA, 0xAAAA5555, ..... so on
2. 0x00000000, 0xFFFFFFFF, 0x00000000, ..... so on

UseCase5 : Cross talk on data line

- the dataline number which shall be fixed to a value
- the value the dataline shall be fixed at:

UseCase6 : Soak testing

Read write access is done to 4KB of DDR memory.

### **5.4.3 Issues**

None

### **5.4.4 PASS or FAIL criterion**

For every datapattern (except for random access) for each write access, read request is issued to verify the DDR contents.

### **5.4.5 Observation**

[svn://hoppin/IP/PDV/G4\\_MAIN/G4M\\_MDDR/tags/1.0.106/results/Validation\\_Board/VB\\_MDDR\\_DDR2.TXT](svn://hoppin/IP/PDV/G4_MAIN/G4M_MDDR/tags/1.0.106/results/Validation_Board/VB_MDDR_DDR2.TXT)

### **5.4.6 SVN Database**

[svn://hoppin/IP/PDV/G4\\_MAIN/G4M\\_MDDR/tags/1.0.106/design/hw/Validation\\_Board/VB\\_MDDR\\_DDR2\\_111\\_333MHz\\_ODT\\_ON.zip](svn://hoppin/IP/PDV/G4_MAIN/G4M_MDDR/tags/1.0.106/design/hw/Validation_Board/VB_MDDR_DDR2_111_333MHz_ODT_ON.zip)

[svn://hoppin/IP/PDV/G4\\_MAIN/G4M\\_MDDR/tags/1.0.106/design/fw/Validation\\_Board/VB\\_MDDR\\_DDR2\\_UseCase2.zip](svn://hoppin/IP/PDV/G4_MAIN/G4M_MDDR/tags/1.0.106/design/fw/Validation_Board/VB_MDDR_DDR2_UseCase2.zip)

## **5.5 UseCase5- DDR3 ScratchPad memory**

### **5.5.1 Deviation from the Validation Plan**

None

### 5.5.2 Implementation Guideline

Remapping is done to ESRAM.

Firmware is used to configure MDDR in DDR3 PHY-32, BL-8 and sequential mode.

Following data patterns are tested as part of scratchpad memory validation

UseCase1 : Alternate read/write access

UseCase2 : Read only data traffic

UseCase3 : Write only data traffic

READ/WRITE ACCESS MODE:

1. Word (32 bit) Access
2. Half-Word (16 bit) Access

READ/WRITE DATA PATTERN:

1. Incrementing
2. Walking One Pattern
3. Walking Zero Pattern
4. Random Data

UseCase4 : Simultaneous toggling of all data lines

Simultaneous DATA Toggling pattern:

1. 0xAAAA5555, 0x5555AAAA, 0xAAAA5555, ..... so on
2. 0x00000000, 0xFFFFFFFF, 0x00000000, ..... so on

UseCase5 : Cross talk on data line

- the dataline number which shall be fixed to a value
- the value the dataline shall be fixed at:

UseCase6 : Soak testing

Read write access is done to 4KB of DDR memory.

### 5.5.3 Issues

None

### 5.5.4 PASS or FAIL criterion

For every datapattern (except for random access) for each write access, read request is issued to verify the DDR contents.

### 5.5.5 Observation

[svn://hoppin/IP/PDV/G4\\_MAIN/G4M\\_MDDR/tags/1.0.106/results/Validation\\_Board/VB\\_MDDR\\_DDR3.TXT](svn://hoppin/IP/PDV/G4_MAIN/G4M_MDDR/tags/1.0.106/results/Validation_Board/VB_MDDR_DDR3.TXT)

### 5.5.6 SVN Database

[svn://hoppin/IP/PDV/G4\\_MAIN/G4M\\_MDDR/tags/1.0.106/design/hw/Validation\\_Board/VB\\_MDDR\\_DDR3\\_111\\_333MHz\\_ODD\\_ON.zip](svn://hoppin/IP/PDV/G4_MAIN/G4M_MDDR/tags/1.0.106/design/hw/Validation_Board/VB_MDDR_DDR3_111_333MHz_ODD_ON.zip)

[svn://hoppin/IP/PDV/G4\\_MAIN/G4M\\_MDDR/tags/1.0.106/design/fw/Validation\\_Board/VB\\_MDDR\\_DDR3\\_UseCase2.zip](svn://hoppin/IP/PDV/G4_MAIN/G4M_MDDR/tags/1.0.106/design/fw/Validation_Board/VB_MDDR_DDR3_UseCase2.zip)

## 5.6 UseCase6- LPDDR ScratchPad memory

### 5.6.1 Deviation from the Validation Plan

None

### 5.6.2 Implementation Guideline

Remapping is done to ESRAM.

Firmware is used to configure MDDR in LPDDR PHY-32, BL-8 and sequential mode.

Following data patterns are tested as part of scratchpad memory validation

UseCase1 : Alternate read/write access

UseCase2 : Read only data traffic

UseCase3 : Write only data traffic

READ/WRITE ACCESS MODE:

1. Word (32 bit) Access
2. Half-Word (16 bit) Access

READ/WRITE DATA PATTERN:

1. Incrementing
2. Walking One Pattern
3. Walking Zero Pattern
4. Random Data

UseCase4 : Simultaneous toggling of all data lines

Simultaneous DATA Toggling pattern:

1. 0xAAAA5555, 0x5555AAAA, 0xAAAA5555, ..... so on
2. 0x00000000, 0xFFFFFFFF, 0x00000000, ..... so on

UseCase5 : Cross talk on data line

- the dataline number which shall be fixed to a value
- the value the dataline shall be fixed at:

UseCase6 : Soak testing

Read write access is done to 4KB of DDR memory.

### 5.6.3 Issues

None

### 5.6.4 PASS or FAIL criterion

For every datapattern (except for random access) for each write access, read request is issued to verify the DDR contents.

### **5.6.5 Observation**

[svn://hoppin/IP/PDV/G4\\_MAIN/G4M\\_MDDR/tags/1.0.106/results/LPDDR/LPDDR\\_VB\\_UC1.TXT](svn://hoppin/IP/PDV/G4_MAIN/G4M_MDDR/tags/1.0.106/results/LPDDR/LPDDR_VB_UC1.TXT)

### **5.6.6 SVN Database**

[svn://hoppin/IP/PDV/G4\\_MAIN/G4M\\_MDDR/tags/1.0.106/design/hw/LPDDR.zip](svn://hoppin/IP/PDV/G4_MAIN/G4M_MDDR/tags/1.0.106/design/hw/LPDDR.zip)

[svn://hoppin/IP/PDV/G4\\_MAIN/G4M\\_MDDR/tags/1.0.106/design/fw/G4M\\_LPDDR\\_VB.zip](svn://hoppin/IP/PDV/G4_MAIN/G4M_MDDR/tags/1.0.106/design/fw/G4M_LPDDR_VB.zip)

## **5.7 UseCase7- Remapping to DDR2**

### **5.7.1 Deviation from the Validation Plan**

None

### **5.7.2 Implementation Guideline**

Remapping is done to DDR2.

This usecase is covered as part of Dhrystone PDV. For details of implementation please refer section 3.2.2.2 of [G4M\\_Dhrystone\\_PDV\\_Result.docx](#)

### **5.7.3 Issues**

None

### **5.7.4 PASS or FAIL criterion**

Application code execution shall be successful when running out of DDR2 memory.

### **5.7.5 Observation**

[svn://hoppin/IP/PDV/G4\\_MAIN/G4M\\_Dhrystone/tags/1.0.100/results/G4M\\_Dhrystone\\_UC2/MDDR\\_DDR\\_3\\_Dhrystone\\_UC2](svn://hoppin/IP/PDV/G4_MAIN/G4M_Dhrystone/tags/1.0.100/results/G4M_Dhrystone_UC2/MDDR_DDR_3_Dhrystone_UC2)

### **5.7.6 SVN Database**

[svn://hoppin/IP/PDV/G4\\_MAIN/G4M\\_Dhrystone/tags/1.0.100/design/fw/G4M\\_Dhrystone\\_UC2/MDDR\\_DR2\\_Dhrystone\\_UC2.zip](svn://hoppin/IP/PDV/G4_MAIN/G4M_Dhrystone/tags/1.0.100/design/fw/G4M_Dhrystone_UC2/MDDR_DR2_Dhrystone_UC2.zip)

[svn://hoppin/IP/PDV/G4\\_MAIN/G4M\\_Dhrystone/tags/1.0.100/design/hw/G4M\\_Dhrystone\\_UC2/MDDR\\_DR2\\_111\\_333MHz\\_ODD\\_ON.zip](svn://hoppin/IP/PDV/G4_MAIN/G4M_Dhrystone/tags/1.0.100/design/hw/G4M_Dhrystone_UC2/MDDR_DR2_111_333MHz_ODD_ON.zip)

## **5.8 UseCase8- Remapping to DDR3**

### **5.8.1 Deviation from the Validation Plan**

None

### **5.8.2 Implementation Guideline**

Remapping is done to DDR3.

This usecase is covered as part of Dhrystone PDV. For details of implementation please refer section 3.2.1.2 of [G4M\\_Dhrystone\\_PDV\\_Result.docx](#)

### **5.8.3 Issues**

None

#### **5.8.4 PASS or FAIL criterion**

Application code execution shall be successful when running out of DDR3 memory.

#### **5.8.5 Observation**

[svn://hoppin/IP/PDV/G4\\_MAIN/G4M\\_Dhrystone/tags/1.0.100/results/G4M\\_Dhrystone\\_UC2/MDDR\\_DDR3\\_Dhrystone\\_UC2](svn://hoppin/IP/PDV/G4_MAIN/G4M_Dhrystone/tags/1.0.100/results/G4M_Dhrystone_UC2/MDDR_DDR3_Dhrystone_UC2)

#### **5.8.6 SVN Database**

[svn://hoppin/IP/PDV/G4\\_MAIN/G4M\\_Dhrystone/tags/1.0.100/design/hw/G4M\\_Dhrystone\\_UC2/MDDR\\_DDR3\\_111\\_333MHz\\_ODD\\_ON.zip](svn://hoppin/IP/PDV/G4_MAIN/G4M_Dhrystone/tags/1.0.100/design/hw/G4M_Dhrystone_UC2/MDDR_DDR3_111_333MHz_ODD_ON.zip)

[svn://hoppin/IP/PDV/G4\\_MAIN/G4M\\_Dhrystone/tags/1.0.100/design/fw/G4M\\_Dhrystone\\_UC2/MDDR\\_DDR3\\_Dhrystone\\_UC2.zip](svn://hoppin/IP/PDV/G4_MAIN/G4M_Dhrystone/tags/1.0.100/design/fw/G4M_Dhrystone_UC2/MDDR_DDR3_Dhrystone_UC2.zip)

### **5.9 UseCase9- Remapping to LPDDR**

#### **5.9.1 Deviation from the Validation Plan**

None

#### **5.9.2 Implementation Guideline**

Remapping is done to LPDDR.

This usecase is covered as part of Dhrystone PDV. For details of implementation please refer section 3.2.3.2 of [G4M\\_Dhrystone\\_PDV\\_Result.docx](#)

#### **5.9.3 Issues**

None

#### **5.9.4 PASS or FAIL criterion**

Application code execution shall be successful when running out of LPDDR memory.

#### **5.9.5 Observation**

[svn://hoppin/IP/PDV/G4\\_MAIN/G4M\\_Dhrystone/tags/1.0.100/results/MDDR\\_LPDDR\\_Dhrystone\\_UC2](svn://hoppin/IP/PDV/G4_MAIN/G4M_Dhrystone/tags/1.0.100/results/MDDR_LPDDR_Dhrystone_UC2)

#### **5.9.6 SVN Database**

[svn://hoppin/IP/PDV/G4\\_MAIN/G4M\\_Dhrystone/tags/1.0.100/design/fw/G4M\\_Dhrystone\\_UC2/MDDR\\_LPDDR\\_Dhrystone\\_UC2.zip](svn://hoppin/IP/PDV/G4_MAIN/G4M_Dhrystone/tags/1.0.100/design/fw/G4M_Dhrystone_UC2/MDDR_LPDDR_Dhrystone_UC2.zip)

[svn://hoppin/IP/PDV/G4\\_MAIN/G4M\\_Dhrystone/tags/1.0.100/design/hw/G4M\\_Dhrystone\\_UC2/MDDR\\_LPDDR3\\_166\\_166MHz.zip](svn://hoppin/IP/PDV/G4_MAIN/G4M_Dhrystone/tags/1.0.100/design/hw/G4M_Dhrystone_UC2/MDDR_LPDDR3_166_166MHz.zip)

### **5.10 UseCase10- Dhrystone test with remapping to DDR2**

#### **5.10.1 Deviation from the Validation Plan**

None

#### **5.10.2 Implementation Guideline**

Remapping is done to DDR2.

This usecase is covered as part of Dhrystone PDV. For details of implementation please refer section 3.2.2.2 of [G4M\\_Dhrystone\\_PDV\\_Result.docx](#)

### **5.10.3 Issues**

None

### **5.10.4 PASS or FAIL criterion**

When remapping is to DDR the Dhrystone performance shall be highest when ROM is in DDR and RAM is in ESRAM, with cache ON.

### **5.10.5 Observation**

For details of implementation please refer section 3.2.2.5 of [G4M\\_Dhrystone\\_PDV\\_Result.docx](#).

[svn://hoppin/IP/PDV/G4\\_MAIN/G4M\\_Dhrystone/tags/1.0.100/results/G4M\\_Dhrystone\\_UC2/MDDR\\_DDR\\_3\\_Dhrystone\\_UC2](svn://hoppin/IP/PDV/G4_MAIN/G4M_Dhrystone/tags/1.0.100/results/G4M_Dhrystone_UC2/MDDR_DDR_3_Dhrystone_UC2)

### **5.10.6 SVN Database**

[svn://hoppin/IP/PDV/G4\\_MAIN/G4M\\_Dhrystone/tags/1.0.100/design/fw/G4M\\_Dhrystone\\_UC2/MDDR\\_DR2\\_Dhrystone\\_UC2.zip](svn://hoppin/IP/PDV/G4_MAIN/G4M_Dhrystone/tags/1.0.100/design/fw/G4M_Dhrystone_UC2/MDDR_DR2_Dhrystone_UC2.zip)

[svn://hoppin/IP/PDV/G4\\_MAIN/G4M\\_Dhrystone/tags/1.0.100/design/hw/G4M\\_Dhrystone\\_UC2/MDDR\\_DR2\\_111\\_333MHz\\_ODD\\_ON.zip](svn://hoppin/IP/PDV/G4_MAIN/G4M_Dhrystone/tags/1.0.100/design/hw/G4M_Dhrystone_UC2/MDDR_DR2_111_333MHz_ODD_ON.zip)

## ***5.11 UseCase11- Dhrystone test with remapping to DDR3***

### **5.11.1 Deviation from the Validation Plan**

None

### **5.11.2 Implementation Guideline**

Remapping is done to DDR3.

This usecase is covered as part of Dhrystone PDV. For details of implementation please refer section 3.2.1.2 of [G4M\\_Dhrystone\\_PDV\\_Result.docx](#)

### **5.11.3 Issues**

None

### **5.11.4 PASS or FAIL criterion**

When remapping is to DDR the Dhrystone performance shall be highest when ROM is in DDR and RAM is in ESRAM, with cache ON.

### **5.11.5 Observation**

For details of implementation please refer section 3.2.1.5 of [G4M\\_Dhrystone\\_PDV\\_Result.docx](#).

[svn://hoppin/IP/PDV/G4\\_MAIN/G4M\\_Dhrystone/tags/1.0.100/results/G4M\\_Dhrystone\\_UC2/MDDR\\_DDR\\_3\\_Dhrystone\\_UC2](svn://hoppin/IP/PDV/G4_MAIN/G4M_Dhrystone/tags/1.0.100/results/G4M_Dhrystone_UC2/MDDR_DDR_3_Dhrystone_UC2)

### **5.11.6 SVN Database**

[svn://hoppin/IP/PDV/G4\\_MAIN/G4M\\_Dhrystone/tags/1.0.100/design/hw/G4M\\_Dhrystone\\_UC2/MDDR\\_DR3\\_111\\_333MHz\\_ODD\\_ON.zip](svn://hoppin/IP/PDV/G4_MAIN/G4M_Dhrystone/tags/1.0.100/design/hw/G4M_Dhrystone_UC2/MDDR_DR3_111_333MHz_ODD_ON.zip)

[svn://hoppin/IP/PDV/G4\\_MAIN/G4M\\_Dhrystone/tags/1.0.100/design/fw/G4M\\_Dhrystone\\_UC2/MDDR\\_DR3\\_Dhrystone\\_UC2.zip](svn://hoppin/IP/PDV/G4_MAIN/G4M_Dhrystone/tags/1.0.100/design/fw/G4M_Dhrystone_UC2/MDDR_DR3_Dhrystone_UC2.zip)

## **5.12 UseCase12- Dhrystone test with remapping to LDDR**

### **5.12.1 Deviation from the Validation Plan**

None

### **5.12.2 Implementation Guideline**

Remapping is done to LPDDR.

This usecase is covered as part of Dhrystone PDV. For details of implementation please refer section 3.2.3.2 of [G4M\\_Dhrystone\\_PDV\\_Result.docx](#)

### **5.12.3 Issues**

None

### **5.12.4 PASS or FAIL criterion**

When remapping is to DDR the Dhrystone performance shall be highest when ROM is in DDR and RAM is in ESRAM, with cache ON.

### **5.12.5 Observation**

For details of implementation please refer section 3.2.1.5 of [G4M\\_Dhrystone\\_PDV\\_Result.docx](#).

[svn://hoppin/IP/PDV/G4\\_MAIN/G4M\\_Dhrystone/tags/1.0.100/results/MDDR\\_LPDDR\\_Dhrystone\\_UC2](svn://hoppin/IP/PDV/G4_MAIN/G4M_Dhrystone/tags/1.0.100/results/MDDR_LPDDR_Dhrystone_UC2)

### **5.12.6 SVN Database**

[svn://hoppin/IP/PDV/G4\\_MAIN/G4M\\_Dhrystone/tags/1.0.100/design/fw/G4M\\_Dhrystone\\_UC2/MDDR\\_LPDDR\\_Dhrystone\\_UC2.zip](svn://hoppin/IP/PDV/G4_MAIN/G4M_Dhrystone/tags/1.0.100/design/fw/G4M_Dhrystone_UC2/MDDR_LPDDR_Dhrystone_UC2.zip)

[svn://hoppin/IP/PDV/G4\\_MAIN/G4M\\_Dhrystone/tags/1.0.100/design/hw/G4M\\_Dhrystone\\_UC2/MDDR\\_LPDDR3\\_166\\_166MHz.zip](svn://hoppin/IP/PDV/G4_MAIN/G4M_Dhrystone/tags/1.0.100/design/hw/G4M_Dhrystone_UC2/MDDR_LPDDR3_166_166MHz.zip)

## **5.13 UseCase13- Bus Access Modes**

### **5.13.1 Deviation from the Validation Plan**

Half Bus width is not validated because for A4P5000 full bus width, burst length =8 and sequential access is recommended, due to the RTL issues

### **5.13.2 Implementation Guideline**

Full bus access configuration is validated for DDR2, DDR3 and LPDDR as part of UseCase4, UseCase5 and Usecase6 respectively.

### **5.13.3 Issues**

None

### **5.13.4 PASS or FAIL criterion**

Read/ write access shall be successful when configured in full-bus mode

### **5.13.5 Observation**

Refer 5.4.5, 5.5.5 and 5.6.5 for results

### **5.13.6 SVN Database**

Refer 5.4.6, 5.5.6 and 5.6.6 for design database

## ***5.14 UseCase14- Interleaved/sequential Access Mode***

### **5.14.1 Deviation from the Validation Plan**

Interleaved access mode is not validated because, for A4P5000 full bus width, burst length =8 and **sequential** access is recommended, due to the RTL issues

### **5.14.2 Implementation Guideline**

Sequential access configuration is validated for DDR2, DDR3 and LPDDR as part of UseCase4, UseCase5 and Usecase6 respectively.

### **5.14.3 Issues**

None

### **5.14.4 PASS or FAIL criterion**

Read/ write access shall be successful when configured in sequential mode

### **5.14.5 Observation**

Refer 5.4.5, 5.5.5 and 5.6.5 for results

### **5.14.6 SVN Database**

Refer 5.4.6, 5.5.6 and 5.6.6 for design database

## ***5.15 UseCase15- DDR memory access with ECC ON***

### **5.15.1 Deviation from the Validation Plan**

None

### **5.15.2 Implementation Guideline**

Enable the ECC mode by modifying the DDR configuration registers and repeat UseCase5 to read/write to DDR memory when ECC is ON.

### **5.15.3 Issues**

None

### **5.15.4 PASS or FAIL criterion**

DDR memory shall be accessible also when ECC is turned ON.

### **5.15.5 Observation**

Read/write access is successful for all the data pattern mentioned in UseCase5 (5.5.2).

[svn://hoppin/IP/PDV/G4\\_MAIN/G4M\\_MDDR/tags/1.0.106/results/Validation\\_Board/VB\\_MDDR\\_DDR3\\_U\\_C15.TXT](svn://hoppin/IP/PDV/G4_MAIN/G4M_MDDR/tags/1.0.106/results/Validation_Board/VB_MDDR_DDR3_U_C15.TXT)

### **5.15.6 SVN Database**

[svn://hoppin/IP/PDV/G4\\_MAIN/G4M\\_MDDR/tags/1.0.106/design/hw/Validation\\_Board/VB\\_MDDR\\_DDR3\\_UseCase15.zip](svn://hoppin/IP/PDV/G4_MAIN/G4M_MDDR/tags/1.0.106/design/hw/Validation_Board/VB_MDDR_DDR3_UseCase15.zip)

[svn://hoppin/IP/PDV/G4\\_MAIN/G4M\\_MDDR/tags/1.0.106/design/fw/Validation\\_Board/VB\\_MDDR\\_DDR3\\_UseCase15.zip](svn://hoppin/IP/PDV/G4_MAIN/G4M_MDDR/tags/1.0.106/design/fw/Validation_Board/VB_MDDR_DDR3_UseCase15.zip)

## **5.16 UseCase16- Burst access**

### **5.16.1 Deviation from the Validation Plan**

Burst length of 4 and 16 are not validated because, for A4P5000 full bus width, **burst length =8** and sequential access is recommended, due to the RTL issues

### **5.16.2 Implementation Guideline**

Burst length of 8 is validated for DDR2, DDR3 and LPDDR as part of UseCase4, UseCase5 and UseCase6 respectively.

### **5.16.3 Issues**

None

### **5.16.4 PASS or FAIL criterion**

Read/ write access shall be successful when configured in BL =8

### **5.16.5 Observation**

Refer 5.4.5, 5.5.5 and 5.6.5 for results

### **5.16.6 SVN Database**

Refer 5.4.6, 5.5.6 and 5.6.6 for design database

## **5.17 UseCase17- Latency analysis: Read write access to open/closed page**

### **5.17.1 Deviation from the Validation Plan**

None

### **5.17.2 Implementation Guideline**

To validate the latency of a closed and open page, write access is done to an open page (i.e by accessing sequential address locations). Also write access is done to non sequential locations (with offset 0x100)

### 5.17.3 Issues

None

### 5.17.4 PASS or FAIL criterion

The page access time for a closed page shall be more than the access time of an open page.

### 5.17.5 Observation

NON Sequential Address TIMER Value = 0x5402d

Sequential Address TIMER Value = 0x44032

[svn://hoppin/IP/PDV/G4\\_MAIN/G4M\\_MDDR/tags/1.0.106/results/Validation\\_Board/VB\\_MDDR\\_DDR3\\_U\\_C17.txt](svn://hoppin/IP/PDV/G4_MAIN/G4M_MDDR/tags/1.0.106/results/Validation_Board/VB_MDDR_DDR3_U_C17.txt)

### 5.17.6 SVN Database

[svn://hoppin/IP/PDV/G4\\_MAIN/G4M\\_MDDR/tags/1.0.106/design/hw/Validation\\_Board/VB\\_MDDR\\_DDR3\\_UseCase17.zip](svn://hoppin/IP/PDV/G4_MAIN/G4M_MDDR/tags/1.0.106/design/hw/Validation_Board/VB_MDDR_DDR3_UseCase17.zip)

[svn://hoppin/IP/PDV/G4\\_MAIN/G4M\\_MDDR/tags/1.0.106/design/fw/Validation\\_Board/VB\\_MDDR\\_DDR3\\_UseCase17.zip](svn://hoppin/IP/PDV/G4_MAIN/G4M_MDDR/tags/1.0.106/design/fw/Validation_Board/VB_MDDR_DDR3_UseCase17.zip)

## 5.18 UseCase18- Priority test: Multi-master read/write access

### 5.18.1 Deviation from the Validation Plan

None

### 5.18.2 Implementation Guideline

#### Libero Design:

MDDR is configured in DDR2 mode.

MDDR configured so that both MSS and fabric Master can access DDR through AXI interface.

AXI Transactor is used as fabric master.

DDR running at 100MHz and MSS at 50 MHz

#### Firmware:

##### Write Access →

Both MSS and transactor will be trying to access MDDR

MSS: HPDMA is configured to write to MDDR-DDR2 memory through DDRBridge.

Transactor is configured to perform burst write access to MDDR

##### Read Access →

Both MSS and transactor will be trying to access MDDR

MSS: HPDMA is configured to read from MDDR-DDR2 memory through DDRBridge.

Transactor is configured to perform burst read access from MDDR

### 5.18.3 Issues

None

### 5.18.4 PASS or FAIL criterion

Both read/write access from MSS and fabric shall be successful and no data corruption shall occur.

### 5.18.5 Observation

It is observed that fabric access is executed first followed by MSS access.

[svn://hoppin/IP/PDV/G4\\_MAIN/G4M\\_MDDR/tags/1.0.107/results/Validation\\_Board/VB\\_MDDR\\_DDR2\\_UseCase18.txt](svn://hoppin/IP/PDV/G4_MAIN/G4M_MDDR/tags/1.0.107/results/Validation_Board/VB_MDDR_DDR2_UseCase18.txt)

### **5.18.6 SVN Database**

[svn://hoppin/IP/PDV/G4\\_MAIN/G4M\\_MDDR/tags/1.0.107/design/hw/Validation\\_Board/VB\\_MDDR\\_DDR3\\_UseCase18.zip](svn://hoppin/IP/PDV/G4_MAIN/G4M_MDDR/tags/1.0.107/design/hw/Validation_Board/VB_MDDR_DDR3_UseCase18.zip)

[svn://hoppin/IP/PDV/G4\\_MAIN/G4M\\_MDDR/tags/1.0.107/design/fw/Validation\\_Board/VB\\_MDDR\\_DDR3\\_UseCase18.zip](svn://hoppin/IP/PDV/G4_MAIN/G4M_MDDR/tags/1.0.107/design/fw/Validation_Board/VB_MDDR_DDR3_UseCase18.zip)

## **5.19 UseCase19- Simultaneous read/write access from AXI read and AXI write channel**

### **5.19.1 Deviation from the Validation Plan**

None

### **5.19.2 Implementation Guideline**

#### **Libero Design:**

Two Fabric transactors are used. One transactor is configured to control the AXI-Write channel and other transactor is configured to control AXI\_read channel of MDD AXI interface.

MDDR is configured in DDR3 mode

MSS is running at 50MHz and DDR at 100MHz

Firmware is used to configure sequential burst access at read and write interface of AXI channel and simultaneous triggering of read and write access is done by generating a TXEV pulse.

### **5.19.3 Issues**

None

### **5.19.4 PASS or FAIL criterion**

Both read and write access shall be successful and no data corruption shall occur.

As the read/write priority is controlled by DDRCTRL (by ddrctl\_prefer\_write), it cannot be controlled by AXI channel (irrespective of the configuration of ddrctl\_prefer\_write)

### **5.19.5 Observation**

[svn://hoppin/IP/PDV/G4\\_MAIN/G4M\\_MDDR/tags/1.0.107/results/Validation\\_Board/VB\\_MDDR\\_DDR3\\_UseCase19](svn://hoppin/IP/PDV/G4_MAIN/G4M_MDDR/tags/1.0.107/results/Validation_Board/VB_MDDR_DDR3_UseCase19)

### **5.19.6 SVN Database**

[svn://hoppin/IP/PDV/G4\\_MAIN/G4M\\_MDDR/tags/1.0.107/design/hw/Validation\\_Board/VB\\_MDDR\\_DDR3\\_UseCase19/FDDR\\_FIC64\\_AXI.zip](svn://hoppin/IP/PDV/G4_MAIN/G4M_MDDR/tags/1.0.107/design/hw/Validation_Board/VB_MDDR_DDR3_UseCase19/FDDR_FIC64_AXI.zip)

[svn://hoppin/IP/PDV/G4\\_MAIN/G4M\\_MDDR/tags/1.0.107/design/fw/Validation\\_Board/VB\\_MDDR\\_DDR3\\_UseCase19/UseCase\\_19\\_20.zip](svn://hoppin/IP/PDV/G4_MAIN/G4M_MDDR/tags/1.0.107/design/fw/Validation_Board/VB_MDDR_DDR3_UseCase19/UseCase_19_20.zip)

## **5.20 UseCase20- Simultaneous read/write access turnaround time**

### **5.20.1 Deviation from the Validation Plan**

None

### **5.20.2 Implementation Guideline**

Same as section 5.19.2

### **5.20.3 Issues**

None

### **5.20.4 PASS or FAIL criterion**

Both read and write access shall be successful and no data corruption shall occur.

As the read/write access gap is controlled by DDRCTRL (by rdwr\_idle\_gap), it cannot be controlled by AXI channel (irrespective of the configuration of rdwr\_idle\_gap)

### **5.20.5 Observation**

[svn://hoppin/IP/PDV/G4\\_MAIN/G4M\\_MDDR/tags/1.0.107/results/Validation\\_Board/VB\\_MDDR\\_DDR3\\_UseCase20](svn://hoppin/IP/PDV/G4_MAIN/G4M_MDDR/tags/1.0.107/results/Validation_Board/VB_MDDR_DDR3_UseCase20)

### **5.20.6 SVN Database**

[svn://hoppin/IP/PDV/G4\\_MAIN/G4M\\_MDDR/tags/1.0.107/design/fw/Validation\\_Board/VB\\_MDDR\\_DDR3\\_UseCase19](svn://hoppin/IP/PDV/G4_MAIN/G4M_MDDR/tags/1.0.107/design/fw/Validation_Board/VB_MDDR_DDR3_UseCase19)

[svn://hoppin/IP/PDV/G4\\_MAIN/G4M\\_MDDR/tags/1.0.107/design/hw/Validation\\_Board/VB\\_MDDR\\_DDR3\\_UseCase20.txt](svn://hoppin/IP/PDV/G4_MAIN/G4M_MDDR/tags/1.0.107/design/hw/Validation_Board/VB_MDDR_DDR3_UseCase20.txt)

## ***5.21 UseCase21- Self refresh entry and exit conditions***

### **5.21.1 Deviation from the Validation Plan**

None

### **5.21.2 Implementation Guideline**

Firmware : Enable the self refresh by setting **reg\_ddrc\_selfref\_en** bit and verify that when no transaction is running the DDR will enter in self refresh mode  
Disabling **reg\_ddrc\_selfref\_en** will not allow the DDR to enter self refresh mode

### **5.21.3 Issues**

None

### **5.21.4 PASS or FAIL criterion**

DDR status register shall read 0x18 when self refresh mode is active

### **5.21.5 Observation**

[svn://hoppin/IP/PDV/G4\\_MAIN/G4M\\_MDDR/tags/1.0.106/results/Validation\\_Board/VB\\_MDDR\\_DDR3\\_UseCase21.txt](svn://hoppin/IP/PDV/G4_MAIN/G4M_MDDR/tags/1.0.106/results/Validation_Board/VB_MDDR_DDR3_UseCase21.txt)

### **5.21.6 SVN Database**

[svn://hoppin/IP/PDV/G4\\_MAIN/G4M\\_MDDR/tags/1.0.106/design/hw/Validation\\_Board/VB\\_MDDR\\_DDR3\\_UseCase21.txt](svn://hoppin/IP/PDV/G4_MAIN/G4M_MDDR/tags/1.0.106/design/hw/Validation_Board/VB_MDDR_DDR3_UseCase21.txt)

[svn://hoppin/IP/PDV/G4\\_MAIN/G4M\\_MDDR/tags/1.0.106/design/fw/Validation\\_Board/VB\\_MDDR\\_DDR3\\_UseCase21.txt](svn://hoppin/IP/PDV/G4_MAIN/G4M_MDDR/tags/1.0.106/design/fw/Validation_Board/VB_MDDR_DDR3_UseCase21.txt)

## **5.22 UseCase22- Power down entry and exit conditions**

### **5.22.1 Deviation from the Validation Plan**

None

### **5.22.2 Implementation Guideline**

Validated on MDDR-DDR3

FirmwareL: Enable the powerdown mode by setting **reg\_ddrc\_powerdown\_en** and verify that, DDR will enter powerdown mode when bus is idle

A read/write access to DDR will bring it to normal mode.

Disabling the **reg\_ddrc\_powerdown\_en bit** will also bring DDR out of powerdown mode

### **5.22.3 Issues**

None

### **5.22.4 PASS or FAIL criterion**

DDR status register = 0x10 when in powerdown mode

DDR status register status shall be changed (!= 0x10) when coming out of powerdown mode.

### **5.22.5 Observation**

[svn://hoppin/IP/PDV/G4\\_MAIN/G4M\\_MDDR/tags/1.0.106/results/Validation\\_Board/VB\\_MDDR\\_DDR3\\_UseCase22.txt](svn://hoppin/IP/PDV/G4_MAIN/G4M_MDDR/tags/1.0.106/results/Validation_Board/VB_MDDR_DDR3_UseCase22.txt)

### **5.22.6 SVN Database**

[svn://hoppin/IP/PDV/G4\\_MAIN/G4M\\_MDDR/tags/1.0.106/design/hw/Validation\\_Board/VB\\_MDDR\\_DDR3\\_UseCase22.txt](svn://hoppin/IP/PDV/G4_MAIN/G4M_MDDR/tags/1.0.106/design/hw/Validation_Board/VB_MDDR_DDR3_UseCase22.txt)

[svn://hoppin/IP/PDV/G4\\_MAIN/G4M\\_MDDR/tags/1.0.106/design/fw/Validation\\_Board/VB\\_MDDR\\_DDR3\\_UseCase22.txt](svn://hoppin/IP/PDV/G4_MAIN/G4M_MDDR/tags/1.0.106/design/fw/Validation_Board/VB_MDDR_DDR3_UseCase22.txt)

## **5.23 UseCase23- Changing the clock frequency**

### **5.23.1 Deviation from the Validation Plan**

None

### **5.23.2 Implementation Guideline**

Validated on MDDR-DDR3.

Firmware:

1. MSS running at 111MHz and DDR running at 333MHz
2. Make read/write access
3. Enable the self refresh mode by setting **reg\_ddrc\_selfref\_en**.
4. Wait till DDR enter selfrefresh mode (DDR status = 0x18).
5. Change the CCC parameters to change the DDR clock frequency to 222MHz
6. Make write and read access to validate the DDR after frequency change

### **5.23.3 Issues**

None

#### **5.23.4 PASS or FAIL criterion**

DDR read/write access shall be successful after frequency change

#### **5.23.5 Observation**

[svn://hoppin/IP/PDV/G4\\_MAIN/G4M\\_MDDR/tags/1.0.106/results/Validation\\_Board/VB\\_MDDR\\_DDR3\\_U\\_C23.txt](svn://hoppin/IP/PDV/G4_MAIN/G4M_MDDR/tags/1.0.106/results/Validation_Board/VB_MDDR_DDR3_U_C23.txt)

#### **5.23.6 SVN Database**

[svn://hoppin/IP/PDV/G4\\_MAIN/G4M\\_MDDR/tags/1.0.106/design/fw/Validation\\_Board/VB\\_MDDR\\_DDR3\\_UseCase23.zip](svn://hoppin/IP/PDV/G4_MAIN/G4M_MDDR/tags/1.0.106/design/fw/Validation_Board/VB_MDDR_DDR3_UseCase23.zip)

[svn://hoppin/IP/PDV/G4\\_MAIN/G4M\\_MDDR/tags/1.0.106/design/hw/Validation\\_Board/VB\\_MDDR\\_DDR3\\_UseCase23.zip](svn://hoppin/IP/PDV/G4_MAIN/G4M_MDDR/tags/1.0.106/design/hw/Validation_Board/VB_MDDR_DDR3_UseCase23.zip)

### ***5.24 UseCase24- Loopback test***

#### **5.24.1 Deviation from the Validation Plan**

Featured removed from the final version of DDR Virage core

#### **5.24.2 Implementation Guideline**

NA

#### **5.24.3 Issues**

None

#### **5.24.4 PASS or FAIL criterion**

NA

#### **5.24.5 Observation**

[NA](#)

#### **5.24.6 SVN Database**

NA

### ***5.25 UseCase25- Deep powerdown mode***

#### **5.25.1 Deviation from the Validation Plan**

None

#### **5.25.2 Implementation Guideline**

LPDDR is used for validation

Enable reg\_ddrc\_deeppowerdown\_en and verify that the DDR status will change to deeppower down when no transactions are observed on DDR bus.

Disabling the deeppowerdown mode accordingly the DDR status will change.

Also observed that when reg\_ddrc\_deeppowerdown\_en is enabled traffic on DDR bus will be executed successfully before it does to deep powerdown mode.

### 5.25.3 Issues

None

### 5.25.4 PASS or FAIL criterion

.Changing the reg\_ddrc\_deeppowerdown\_en shall enable and disable deeppower down mode of DDR.

### 5.25.5 Observation

[svn://hoppin/IP/PDV/G4\\_MAIN/G4M\\_MDDR/tags/1.0.107/results/Validation\\_Board/VB\\_LPDDR\\_DDR3\\_U\\_C25.txt](svn://hoppin/IP/PDV/G4_MAIN/G4M_MDDR/tags/1.0.107/results/Validation_Board/VB_LPDDR_DDR3_U_C25.txt)

### 5.25.6 SVN Database

[svn://hoppin/IP/PDV/G4\\_MAIN/G4M\\_MDDR/tags/1.0.107/design/hw/Validation\\_Board/VB\\_MDDR\\_DDR3\\_UseCase25.zip](svn://hoppin/IP/PDV/G4_MAIN/G4M_MDDR/tags/1.0.107/design/hw/Validation_Board/VB_MDDR_DDR3_UseCase25.zip)

[svn://hoppin/IP/PDV/G4\\_MAIN/G4M\\_MDDR/tags/1.0.107/design/fw/Validation\\_Board/VB\\_MDDR\\_LPDDR\\_UseCase25.zip](svn://hoppin/IP/PDV/G4_MAIN/G4M_MDDR/tags/1.0.107/design/fw/Validation_Board/VB_MDDR_LPDDR_UseCase25.zip)

## 5.26 UseCase26- Address collision handling

### 5.26.1 Deviation from the Validation Plan

None

### 5.26.2 Implementation Guideline

Validated on MDDR-DDR3

Multiple writes to same address: CM3 trying to write different data to same address.

Multiple reads from same address: CM3 trying to access same memory to read data

Multiple writes colliding with read: Read access is made to same address when multiple write access is made by CM3.

Multiple reads colliding with write: Write access is made to same address when multiple read access is made by CM3.

### 5.26.3 Issues

None

### 5.26.4 PASS or FAIL criterion

In case of write collision last write access data shall be updated in the DDR memory.

### 5.26.5 Observation

[svn://hoppin/IP/PDV/G4\\_MAIN/G4M\\_MDDR/tags/1.0.106/results/Validation\\_Board/VB\\_MDDR\\_DDR3\\_U\\_C26.TXT](svn://hoppin/IP/PDV/G4_MAIN/G4M_MDDR/tags/1.0.106/results/Validation_Board/VB_MDDR_DDR3_U_C26.TXT)

### 5.26.6 SVN Database

[svn://hoppin/IP/PDV/G4\\_MAIN/G4M\\_MDDR/tags/1.0.106/design/hw/Validation\\_Board/VB\\_MDDR\\_DDR3\\_UseCase26.txt](svn://hoppin/IP/PDV/G4_MAIN/G4M_MDDR/tags/1.0.106/design/hw/Validation_Board/VB_MDDR_DDR3_UseCase26.txt)

[svn://hoppin/IP/PDV/G4\\_MAIN/G4M\\_MDDR/tags/1.0.106/design/fw/Validation\\_Board/VB\\_MDDR\\_DDR3\\_UseCase26.txt](svn://hoppin/IP/PDV/G4_MAIN/G4M_MDDR/tags/1.0.106/design/fw/Validation_Board/VB_MDDR_DDR3_UseCase26.txt)

## **5.27 UseCase27- Code Shadowing → SPI to MDDR**

### **5.27.1 Deviation from the Validation Plan**

None

### **5.27.2 Implementation Guideline**

This usecase is covered by Applications group.

### **5.27.3 Issues**

None

### **5.27.4 PASS or FAIL criterion**

Code shall be copied successfully from SPI to DDR and executions shall be successful.

### **5.27.5 Observation**

[SF2\\_CodeShadowing\\_DDR3\\_DF.rar](#) from [Version 1.0](#)

### **5.27.6 SVN Database**

[SF2\\_CodeShadowing\\_DDR3\\_DF.rar](#) from [Version 1.0](#)

## **5.28 UseCase28- Code Shadowing → NOR Flash to MDDR**

### **5.28.1 Deviation from the Validation Plan**

This usecase is not applicable as NOR Flash support is not available on board

### **5.28.2 Implementation Guideline**

NA

### **5.28.3 Issues**

None

### **5.28.4 PASS or FAIL criterion**

NA

### **5.28.5 Observation**

NA

### **5.28.6 SVN Database**

NA

## **5.29 UseCase29- EDAC error detection and correction**

### **5.29.1 Deviation from the Validation Plan**

None

### **5.29.2 Implementation Guideline**

The validation is done using MDDR-DDR3

Firmware:

1. EDAC for MDDR-DDR3 is enabled and data is written to single DDR memory location.
2. Disabled EDAC and single bit of the DDR memory is manipulated.
3. Enable EDAC and read the content of the manipulated memory location.
4. Steps 1-3 are repeated for various DDR memory locations

Verified that for single bit error the contents are corrected

Two bits of DDR memory is manipulated for Double bit error case. In case of double bit error the error counter is incremented but the CPU goes to HardFault error condition

### **5.29.3 Issues**

None

### **5.29.4 PASS or FAIL criterion**

For single bit error, error shall be detected and the single bit error counter shall be incremented by 1 for every bit error. The error shall also be corrected.

For double bit error the error shall be detected and the double bit error counter shall be incremented. This error cannot be corrected

### **5.29.5 Observation**

[svn://hoppin/IP/PDV/G4\\_MAIN/G4M\\_MDDR/tags/1.0.106/results/Validation\\_Board/VB\\_MDDR\\_DDR3\\_U\\_C29.TXT](svn://hoppin/IP/PDV/G4_MAIN/G4M_MDDR/tags/1.0.106/results/Validation_Board/VB_MDDR_DDR3_U_C29.TXT)

### **5.29.6 SVN Database**

[svn://hoppin/IP/PDV/G4\\_MAIN/G4M\\_MDDR/tags/1.0.106/design/fw/Validation\\_Board/VB\\_MDDR\\_DDR3\\_UseCase29.txt](svn://hoppin/IP/PDV/G4_MAIN/G4M_MDDR/tags/1.0.106/design/fw/Validation_Board/VB_MDDR_DDR3_UseCase29.txt)

[svn://hoppin/IP/PDV/G4\\_MAIN/G4M\\_MDDR/tags/1.0.106/design/hw/Validation\\_Board/VB\\_MDDR\\_DDR3\\_UseCase29.txt](svn://hoppin/IP/PDV/G4_MAIN/G4M_MDDR/tags/1.0.106/design/hw/Validation_Board/VB_MDDR_DDR3_UseCase29.txt)

## **5.30 UseCase30- Soak test**

### **5.30.1 Deviation from the Validation Plan**

None

### **5.30.2 Implementation Guideline**

The validation is done using MDDR-DDR3

### **5.30.3 Issues**

None

### 5.30.4 PASS or FAIL criterion

### 5.30.5 Observation

[svn://hoppin/IP/PDV/G4\\_MAIN/G4M\\_MDDR/tags/1.0.106/results/Validation\\_Board/VB\\_MDDR\\_DDR3\\_UC30.TXT](svn://hoppin/IP/PDV/G4_MAIN/G4M_MDDR/tags/1.0.106/results/Validation_Board/VB_MDDR_DDR3_UC30.TXT)

### 5.30.6 SVN Database

[svn://hoppin/IP/PDV/G4\\_MAIN/G4M\\_MDDR/tags/1.0.106/design/hw/Validation\\_Board/VB\\_MDDR\\_DDR3\\_UseCase30.txt](svn://hoppin/IP/PDV/G4_MAIN/G4M_MDDR/tags/1.0.106/design/hw/Validation_Board/VB_MDDR_DDR3_UseCase30.txt)

[svn://hoppin/IP/PDV/G4\\_MAIN/G4M\\_MDDR/tags/1.0.106/design/fw/Validation\\_Board/VB\\_MDDR\\_DDR3\\_UseCase30.txt](svn://hoppin/IP/PDV/G4_MAIN/G4M_MDDR/tags/1.0.106/design/fw/Validation_Board/VB_MDDR_DDR3_UseCase30.txt)

## 5.31 A2F5000 MDDR Validation Summary

UseModel	Feature under validation	Result	Issues/Comments
UseCase1	MDDR-DDR2 Provisioning	Passed	None
UseCase2	MDDR-DDR3 Provisioning	Passed	None
UseCase3	MDDR-LPDDR Provisioning	Passed	None
UseCase4	DDR2 ScratchPad memory	Passed	None
UseCase5	DDR3 ScratchPad memory	Passed	None
UseCase6	LPDDR ScratchPad memory	Passed	None
UseCase7	Remapping to DDR2	Passed	None

UseModel	Feature under validation	Result	Issues/Comments
UseCase8	Remapping to DDR3	Passed	None
UseCase9	Remapping to LPDDR	Passed	None
UseCase10	Dhrystone test with remapping to DDR2	Passed	None
UseCase11	Dhrystone test with remapping to DDR3	Passed	None
UseCase12	Dhrystone test with remapping to LPDDR	Passed	None
UseCase13	Bus Access Modes	Passed	None
UseCase14	Interleaved/sequential Access Mode	Passed	Sequential mode tested (A4P5000 restricted to sequential BL8 access)
UseCase15	DDR memory access with ECC ON	Passed	None
UseCase16	Burst access	Passed	BL = 8 validated (A4P5000 restricted to sequential BL8 access)
UseCase17	Latency analysis: Read write access to open/closed page	Passed	None
UseCase18	Priority test: Multi-master read/write access	Passed	None
UseCase19	Simultaneous read/write access from AXI read and AXI write channel	Passed	None

UseModel	Feature under validation	Result	Issues/Comments
UseCase20	Simultaneous read/write access turnaround time	Passed	None
UseCase21	Self refresh entry and exit conditions	Passed	None
UseCase22	Power down entry and exit conditions	Passed	None
UseCase23	Changing the clock frequency	Passed	None
UseCase24	Loopback test	NA	None
UseCase25	Deep powerdown mode	Passed	None
UseCase26	Address collision handling	Passed	None
UseCase27	Code Shadowing	Done	Validated by Apps team
UseCase28	Code Shadowing	NA	Not applicable as NOR FLASH support is not available
UseCase29	EDAC error detection and correction	Passed	None
UseCase30	Soak test for the different memory stress tests (to test DLL reliability etc)	Passed	None

**Table 5 List of UseCases**

## 6 M2S090 MDDR Results

### 6.1 Equipment Used

#### 6.1.1 Hardware

S.No	Equipment/Board	Qty	Remarks/Serial Number
1	M2S090 Validation Board	1	M2S090T_VALIDATION_BOARD Rev-A (X2-PAC003) (Socket Board)  With Silicon labelled 11(for Rev-A) With Silicon labelled 64(for Rev-B) With Silicon labelled 119(for Rev-C)
2	Silicon	1	M2S090 (labelled 12 NO FT)
3	EWARM Debugger	1	S/No:158009982
4	Flashpro4	1	30000
5	USB to Micro USB cable	1	On G4M Validation board UART0 is connected via fabric to the PC via USB cable.
6	PC	1	Stand-alone PC w764-mahveens1
7	DDR2 Custom DIMM	1	Labelled A2 (MT47H128M8CF-25:H TR)
8	DDR3 Custom DIMM	1	Labelled A2 (MT41J256M8HX-15E:D TR)
9	LPDDR Custom DIMM	1	Labelled 1(MT46H32M16LFBF-6 IT:C TR)

**Table 6 Hardware Equipment used**

#### 6.1.2 Software

UseCase	Libero Capture	MSS
All MDDR-DDR2 UseCase	11.2.1.12	Systembuilder 1.0
All MDDR-DDR3 UseCases	11.2.1.12	Systembuilder 1.0
All DDR-LPDDR UseCases	11.2.1.12	Systembuilder 1.0

**Table 7 Libero Equipment used**

S.No	Tool	Version
1	EWARM(IAR)	Software version 6.4

**Table 8 Software Equipment used**

S.No	MDDR Interface	DDR Memory Model	MSS Frequency	DDR Frequency
1	DDR3	MT41J256M8HX-15E:D TR	111MHz	333MHz
2	DDR2	MT47H128M8CF-25:H TR	111MHz	333MHz
3	LPDDR	MT46H32M16LFBF-6 IT:C TR	166MHz	166MHz

**Table 9 DDR Frequency**

## 6.2 Use Models & Use Cases

### 6.2.1 MDDR→DDR3 UseCase1- MSS to MDDR read/write access with ECC OFF

#### 6.2.1.1 Deviation from the Validation Plan

None

#### 6.2.1.2 Implementation Guideline

##### Libero:

Systembuilder is used to configure DDR by importing DDR configuration file.

DDR Configuration file is used to configure DDR in PHY\_16 mode with BL=8 and **ECC = OFF**

Remapping is done to eNVM. Application is stored in eNVM as part of programming file.

##### Firmware:

Firmware is used to configure MDDR in sequential/interleaved mode.

Word, half-word and byte access is done with incremental, walking-1 and walking-0 patterns

Write access: HPDMA is configured to transfer above mentioned data pattern from ESRAM1 to DDR.

CM3 will read the DDR contents to verify if the data written matches with expected data.

#### 6.2.1.3 Issues

None

#### 6.2.1.4 PASS or FAIL criterion

Configuration validation is done by polling the status register in firmware.

Verified that status register reflects that MDDR is configured and MDDR is brought to normal mode.

Correctness of configuration is verified by read/write access to DDR3

#### 6.2.1.5 Observation

[svn://owl/IP/PDV/G4\\_MAIN/DERIVATIVES/M2S090/tags/1.0.100/design/MDDR/DDR3/UseCase1/Result](svn://owl/IP/PDV/G4_MAIN/DERIVATIVES/M2S090/tags/1.0.100/design/MDDR/DDR3/UseCase1/Result)

#### 6.2.1.6 SVN Database

[svn://owl/IP/PDV/G4\\_MAIN/DERIVATIVES/M2S090/tags/1.0.100/design/MDDR/DDR3/UseCase1/design](svn://owl/IP/PDV/G4_MAIN/DERIVATIVES/M2S090/tags/1.0.100/design/MDDR/DDR3/UseCase1/design)

### 6.2.2 MDDR→DDR3 UseCase2- MSS to MDDR read/write access with ECC ON

#### 6.2.2.1 Deviation from the Validation Plan

None

#### 6.2.2.2 Implementation Guideline

##### Libero:

Systembuilder is used to configure DDR by importing DDR configuration file.

DDR Configuration file is used to configure DDR in PHY\_16 mode with BL=8 and **ECC = ON**

Remapping is done to eNVM. Application is stored in eNVM as part of programming file.

##### Firmware:

Firmware is used to configure MDDR in sequential/interleaved mode.

Word, half-word and byte access is done with incremental, walking-1 and walking-0 patterns

Write access: HPDMA is configured to transfer above mentioned data pattern from ESRAM1 to DDR. CM3 will read the DDR contents to verify if the data written matches with expected data.

### **6.2.2.3 Issues**

None

### **6.2.2.4 PASS or FAIL criterion**

Configuration validation is done by polling the status register in firmware.

Verified that status register reflects that MDDR is configured and MDDR is brought to normal mode.

Correctness of configuration is verified by read/write access to DDR3

### **6.2.2.5 Observation**

[svn://owl/IP/PDV/G4\\_MAIN/DERIVATIVES/M2S090/tags/1.0.100/design/MDDR/DDR3/UseCase2/Result](svn://owl/IP/PDV/G4_MAIN/DERIVATIVES/M2S090/tags/1.0.100/design/MDDR/DDR3/UseCase2/Result)

### **6.2.2.6 SVN Database**

[svn://owl/IP/PDV/G4\\_MAIN/DERIVATIVES/M2S090/tags/1.0.100/design/MDDR/DDR3/UseCase2/design](svn://owl/IP/PDV/G4_MAIN/DERIVATIVES/M2S090/tags/1.0.100/design/MDDR/DDR3/UseCase2/design)

## **6.2.3 MDDR→DDR2 UseCase1- MSS to MDDR read/write access with ECC OFF**

### **6.2.3.1 Deviation from the Validation Plan**

None

### **6.2.3.2 Implementation Guideline**

Implementation guideline is same as section 6.2.3.2 except that MDDR is configured for DDR2 mode.

### **6.2.3.3 Issues**

None

### **6.2.3.4 PASS or FAIL criterion**

Configuration validation is done by polling the status register in firmware.

Verified that status register reflects that MDDR is configured and MDDR is brought to normal mode.

Correctness of configuration is verified by read/write access to DDR2

### **6.2.3.5 Observation**

[svn://owl/IP/PDV/G4\\_MAIN/DERIVATIVES/M2S090/tags/1.0.100/design/MDDR/DDR2/UseCase1/Result](svn://owl/IP/PDV/G4_MAIN/DERIVATIVES/M2S090/tags/1.0.100/design/MDDR/DDR2/UseCase1/Result)

### **6.2.3.6 SVN Database**

[svn://owl/IP/PDV/G4\\_MAIN/DERIVATIVES/M2S090/tags/1.0.100/design/MDDR/DDR2/UseCase1/design](svn://owl/IP/PDV/G4_MAIN/DERIVATIVES/M2S090/tags/1.0.100/design/MDDR/DDR2/UseCase1/design)

## **6.2.4 MDDR→DDR2 UseCase2- MSS to MDDR read/write access with ECC ON**

### **6.2.4.1 Deviation from the Validation Plan**

None

### **6.2.4.2 Implementation Guideline**

#### **Libero:**

Systembuilder is used to configure DDR by importing DDR configuration file.

DDR Configuration file is used to configure DDR in PHY\_16 mode with BL=8 and **ECC = ON**

Remapping is done to eNVM. Application is stored in eNVM as part of programming file.

#### **Firmware:**

Firmware is used to configure MDDR in sequential/interleaved mode.

Word, half-word and byte access is done with incremental, walking-1 and walking-0 patterns

Write access: HPDMA is configured to transfer above mentioned data pattern from ESRAM1 to DDR.

CM3 will read the DDR contents to verify if the data written matches with expected data.

#### **6.2.4.3 Issues**

None

#### **6.2.4.4 PASS or FAIL criterion**

Configuration validation is done by polling the status register in firmware.

Verified that status register reflects that MDDR is configured and MDDR is brought to normal mode.

Correctness of configuration is verified by read/write access to DDR2

#### **6.2.4.5 Observation**

[svn://owl/IP/PDV/G4\\_MAIN/DERIVATIVES/M2S090/tags/1.0.100/design/MDDR/DDR2/UseCase2/Result](svn://owl/IP/PDV/G4_MAIN/DERIVATIVES/M2S090/tags/1.0.100/design/MDDR/DDR2/UseCase2/Result)

#### **6.2.4.6 SVN Database**

[svn://owl/IP/PDV/G4\\_MAIN/DERIVATIVES/M2S090/tags/1.0.100/design/MDDR/DDR2/UseCase2/design](svn://owl/IP/PDV/G4_MAIN/DERIVATIVES/M2S090/tags/1.0.100/design/MDDR/DDR2/UseCase2/design)

### **6.2.5 MDDR→LDDR UseCase1- MSS to MDDR read/write access with BL\_8 ECC OFF**

#### **6.2.5.1 Deviation from the Validation Plan**

None

#### **6.2.5.2 Implementation Guideline**

Implementation guideline is same as section 6.2.3.2 except that MDDR is configured for LPDDR in BL = 8 mode.

#### **6.2.5.3 Issues**

None

#### **6.2.5.4 PASS or FAIL criterion**

Configuration validation is done by polling the status register in firmware.

Verified that status register reflects that MDDR is configured and MDDR is brought to normal mode.

Correctness of configuration is verified by read/write access to LPDDR

#### **6.2.5.5 Observation**

[svn://owl/IP/PDV/G4\\_MAIN/DERIVATIVES/M2S090/tags/1.0.100/design/MDDR/LPDDR/UseCase1/Result](svn://owl/IP/PDV/G4_MAIN/DERIVATIVES/M2S090/tags/1.0.100/design/MDDR/LPDDR/UseCase1/Result)

#### **6.2.5.6 SVN Database**

[svn://owl/IP/PDV/G4\\_MAIN/DERIVATIVES/M2S090/tags/1.0.100/design/MDDR/LPDDR/UseCase1/design](svn://owl/IP/PDV/G4_MAIN/DERIVATIVES/M2S090/tags/1.0.100/design/MDDR/LPDDR/UseCase1/design)

### **6.2.6 MDDR→LPDDR UseCase2- MSS to MDDR read/write access with BL\_8 ECC ON**

#### **6.2.6.1 Deviation from the Validation Plan**

None

### **6.2.6.2 Implementation Guideline**

Implementation guideline is same as section 6.2.4.2 except that MDDR is configured for LPDDR in BL = 8 mode.

### **6.2.6.3 Issues**

None

### **6.2.6.4 PASS or FAIL criterion**

Configuration validation is done by polling the status register in firmware.

Verified that status register reflects that MDDR is configured and MDDR is brought to normal mode.

Correctness of configuration is verified by read/write access to LPDDR

### **6.2.6.5 Observation**

[svn://owl/IP/PDV/G4\\_MAIN/DERIVATIVES/M2S090/tags/1.0.100/design/MDDR/LPDDR/UseCase2/Result](svn://owl/IP/PDV/G4_MAIN/DERIVATIVES/M2S090/tags/1.0.100/design/MDDR/LPDDR/UseCase2/Result)

### **6.2.6.6 SVN Database**

[svn://owl/IP/PDV/G4\\_MAIN/DERIVATIVES/M2S090/tags/1.0.100/design/MDDR/LPDDR/UseCase2/design](svn://owl/IP/PDV/G4_MAIN/DERIVATIVES/M2S090/tags/1.0.100/design/MDDR/LPDDR/UseCase2/design)

## **6.2.7 MDDR→LDDR UseCase3- MSS to MDDR read/write access with BL\_16 ECC OFF**

### **6.2.7.1 Deviation from the Validation Plan**

None

### **6.2.7.2 Implementation Guideline**

Implementation guideline is same as section 6.2.3.2 except that MDDR is configured for LPDDR in BL = 16 mode.

### **6.2.7.3 Issues**

None

### **6.2.7.4 PASS or FAIL criterion**

Configuration validation is done by polling the status register in firmware.

Verified that status register reflects that MDDR is configured and MDDR is brought to normal mode.

Correctness of configuration is verified by read/write access to LPDDR

### **6.2.7.5 Observation**

Captured as part of LPDDR UseCase1

[svn://owl/IP/PDV/G4\\_MAIN/DERIVATIVES/M2S090/tags/1.0.100/design/MDDR/LPDDR/UseCase1/Result](svn://owl/IP/PDV/G4_MAIN/DERIVATIVES/M2S090/tags/1.0.100/design/MDDR/LPDDR/UseCase1/Result)

### **6.2.7.6 SVN Database**

[svn://owl/IP/PDV/G4\\_MAIN/DERIVATIVES/M2S090/tags/1.0.100/design/MDDR/LPDDR/UseCase1/design](svn://owl/IP/PDV/G4_MAIN/DERIVATIVES/M2S090/tags/1.0.100/design/MDDR/LPDDR/UseCase1/design)

## **6.2.8 MDDR→LPDDR UseCase4- MSS to MDDR read/write access with BL\_16 ECC ON**

### **6.2.8.1 Deviation from the Validation Plan**

None

### **6.2.8.2 Implementation Guideline**

Implementation guideline is same as section 6.2.4.2 except that MDDR is configured for LPDDR in BL = 16 mode.

### **6.2.8.3 Issues**

None

### **6.2.8.4 PASS or FAIL criterion**

Configuration validation is done by polling the status register in firmware.

Verified that status register reflects that MDDR is configured and MDDR is brought to normal mode.

Correctness of configuration is verified by read/write access to LPDDR

### **6.2.8.5 Observation**

Captured as part of LPDDR UseCase2

[svn://owl/IP/PDV/G4\\_MAIN/DERIVATIVES/M2S090/tags/1.0.100/design/MDDR/LPDDR/UseCase2/Result](svn://owl/IP/PDV/G4_MAIN/DERIVATIVES/M2S090/tags/1.0.100/design/MDDR/LPDDR/UseCase2/Result)

### **6.2.8.6 SVN Database**

[svn://owl/IP/PDV/G4\\_MAIN/DERIVATIVES/M2S090/tags/1.0.100/design/MDDR/LPDDR/UseCase2/design](svn://owl/IP/PDV/G4_MAIN/DERIVATIVES/M2S090/tags/1.0.100/design/MDDR/LPDDR/UseCase2/design)

### 6.3 M2S090 MDDR Validation Summary

UseModel	Feature under validation	Result	Issues/Comments
UseCase1	MSS to MDDR read/write access with ECC OFF	Passed	None
UseCase2	MSS to MDDR read/write access with BL_8 ECC ON	Passed	None
UseCase3	MSS to MDDR read/write access with BL_16 ECC OFF	Passed	None
UseCase4	MSS to MDDR read/write access with BL_16 ECC ON	Passed	None

**Table 10 List of UseCases**