G4M-FDDR Verification and Validation Report

Revision: 1.0

Date: September 9th, 2014

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Revision History

Version	Date	Modified by	Changes
0.1	1st October 2012	SM	Initial Version
0.2	31st January 2013	SM	Added validation result of Phase-II
0.3	8th September 2014	SW	Created Report version Created SAR Summary
1.0	9th September 2014	Mktg SW, KO	Finalized for customer distribution

Glossary

Term	Description
LIN	Local Interconnect Network
Use Case	A specific configuration of a use model.
Use Model	A reference platform designed from configurable h/w and s/w components, which is targeted at a focused application. The use model demonstrates one of several possible ways of integrating IPs to build a system and one of several ways in which it could be used by the customer.
ISR	Interrupt Service Routine – Subroutine executed as a result of an IRQ
MMUART	Multi-Mode Universal Asynchronous Receiver Transmitter
G4	4th Generation Flash chip from Microsemi
Frame	All LIN information is transmitted packed as frames; a frame consists of a header and a response

REFERENCES

1. G4M_FDDR_PDV_PLAN.docx
2. G4M_Dhrystone_PDV_Result.docx
3. G4M_FDDR_PDV_Results.docx

1 Introduction

This document explains the design of and execution of validation results of various A4P5000 FDDR PDV Phase-I UseCases executed on Validation Board.

[redacted] *Purpose and Scope*

The purpose of this document is to describe the G4 FDDR as well as its plans and tests that are performed as a part of silicon validation and verification. All UseCases are elaborated upon and reports of issues during verification are documented. This document is to provide a holistic view of the verification and validation process.

[redacted] *Standards and Requirements*

The Design team and the Verification and Validation Team have different reporting structures that are independent of one another.

2 G4M FDDR SubSystem background

In the case of the FDDR subsystem, there is one interface present to the DDR. This is a multiplexed interface from the FPGA fabric, which can be configured as either a single AXI 64-bit bus or two 32-bit AHB-Lite buses. There is also a 16-bit APB configuration bus, which is used to initialize the majority of the internal registers within the FDDR subsystem after reset. This APB configuration bus is mastered by the FPGA fabric only.

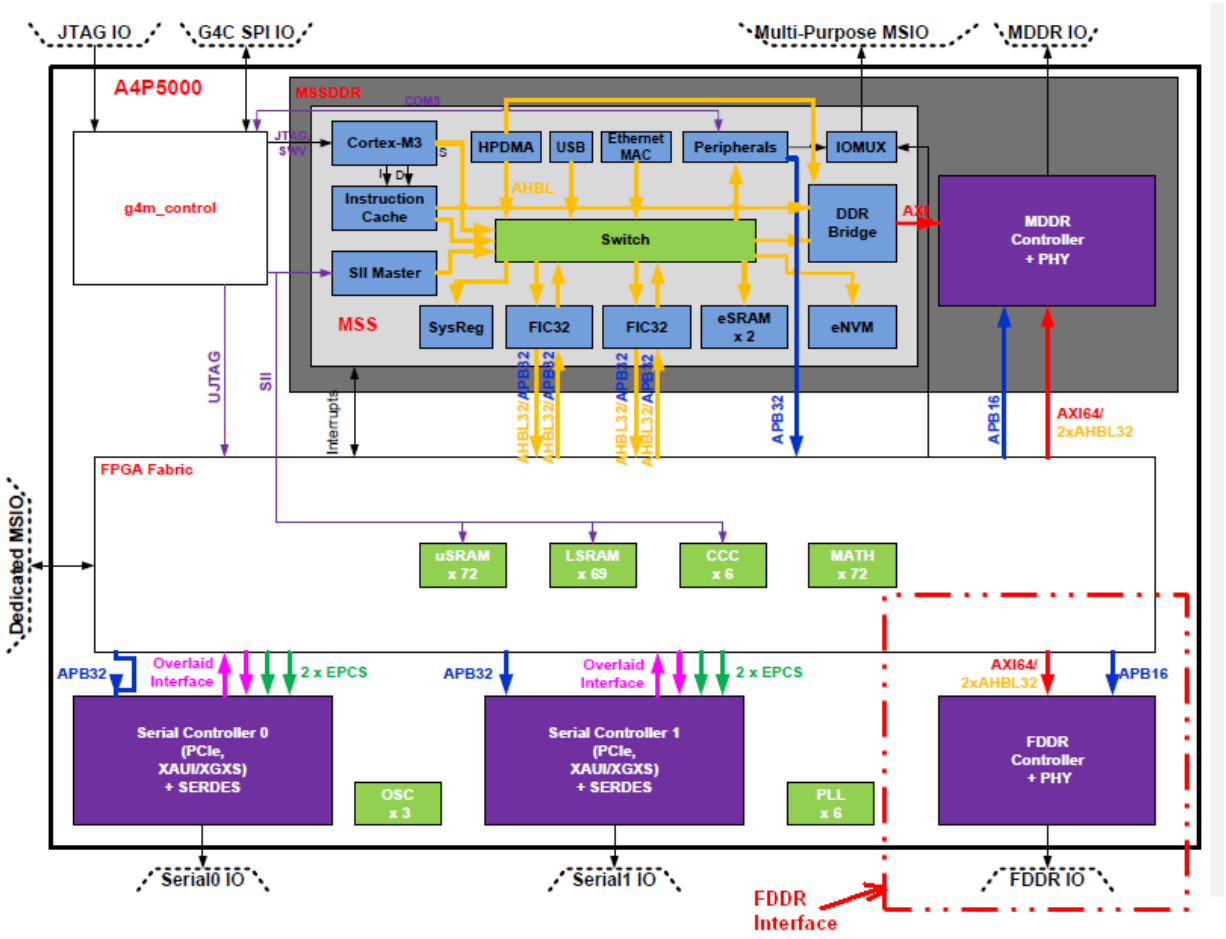

Figure 1 : A4P5000 Architecture

3 Use Models & Use Cases Design Phase

[redacted]*UseCases*

UseModel	Feature under validation	Description	
UseCase1	APB Configuration of FDDR	MSS is the master for the APB configuration of the FDDR. The APB-related clocks and resets in the fabric are connected as shown in Figure 4	
UseCase2a	AXI Slave → Read Write access	Read write access shall be done to FDDR in AXI mode with following data pattern	
		Data pattern 1. Sequential incrementing 2. Walking ones 3. Walking zeros 4. 0xAAAAAAAA, 0x55555555 …. so on	Access Mode 1. word 2. Half Word
UseCase2b	AXI Slave → Remapping to FDDR	Remapping is done to FDDR-DDR3 and the application shall be stored and executed out of FDDR-DDR3 memory	
UseCase2c	AXI Slave → Dhrystone test	Remapping is done to FDDR and Dhrystone tests are executed as described in UseCase2 of G4M_Dhrystone_PDV_PLAN.docx	
UseCase3a	AHB Slave → Read Write access	Read write access shall be done to FDDR in AHB mode with following data pattern	
		Data pattern 5. Sequential incrementing 6. Walking ones 7. Walking zeros 0xAAAAAAAA, 0x55555555 …. so on	Access Mode 3. word 4. Half Word
UseCase3b	AHB Slave → Remapping to FDDR	Remapping is done to FDDR-DDR3 and the application shall be stored and executed out of FDDR-DDR3 memory	
UseCase3c	AHB Slave → Dhrystone test	Remapping is done to FDDR and Dhrystone tests are executed as described in UseCase2 of G4M_Dhrystone_PDV_PLAN.docx	
UseCase4	FDDR Interrupt Validation	Create the ECC error interrupt scenario and verify that the ECC error interrupt is generated when enabled.	

UseModel	Feature under validation	Description
		Verify the PLL Lock interrupt
UseCase5	AXI Fabric Master Access → 4 Overlapping Reads	Fabric Master (Transactor) shall be used to access FDDR in AXI mode. Generate Burst of write and read transaction to FDDR→ DDR3
	AXI Fabric Master Access → 16 back to back transactions	
	AXI Fabric Master Access → INCR,WRAP transfers	
UseCase6	ABH_1 Fabric Master Access → 16 back to back transactions	Fabric Master (Transactor) shall be used to access FDDR in AHB mode. Generate Burst of write and read transaction to FDDR→ DDR3
	ABH_1 Fabric Master Access → INCR, WRAP Transactions	
UseCase7	Both AHBL_1 and AHBL_2 Fabric Master Access →16 back to back transactions	Fabric Master (Transactor) shall be used to access FDDR by two AHB interfaces. Generate Burst of write and read transaction to FDDR→ DDR3
	Both AHBL_1 and AHBL_2 Fabric Master Access → INCR, WRAP Transactions	

Table 1 List of UseCases

UseCases1

Fabric Use Models: MSS Master – APB Configuration Bus

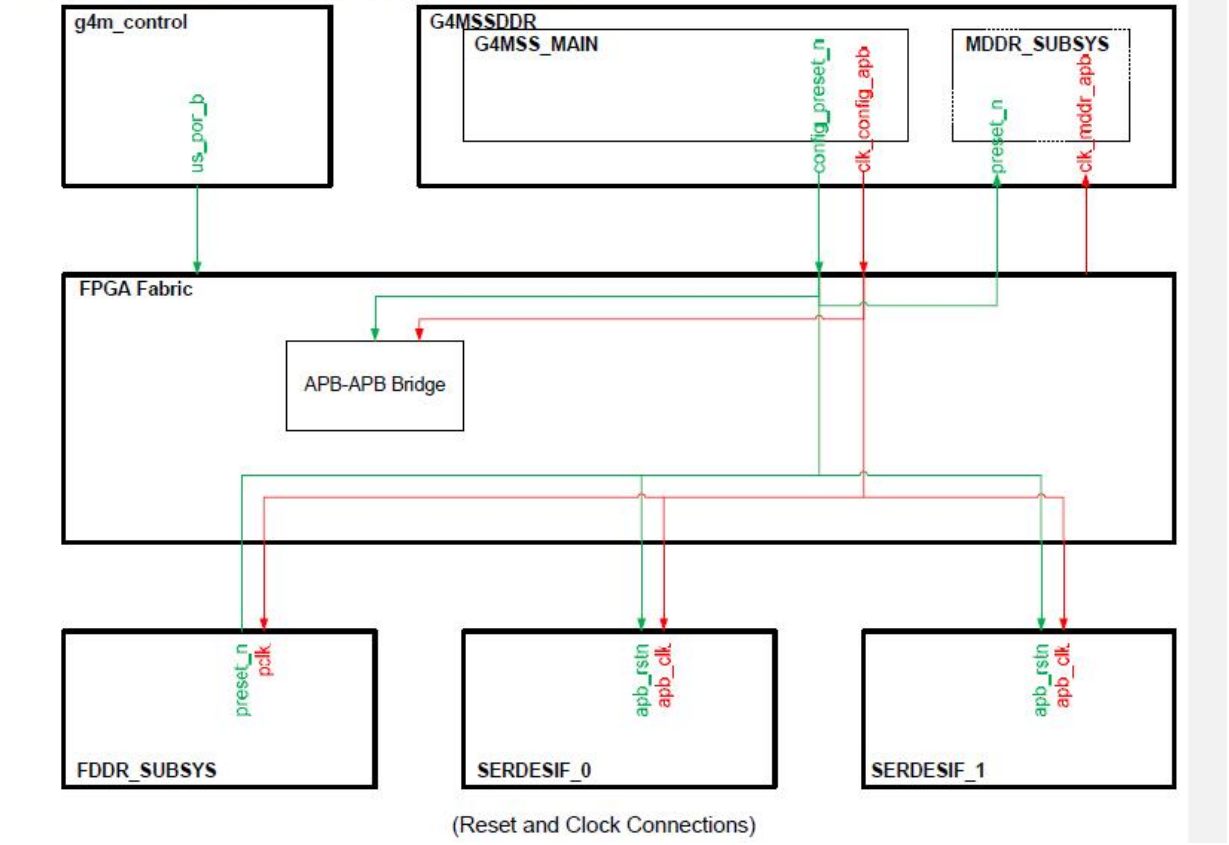

Figure 2 MSS Master – APB Configuration Bus Clocks and Resets

UseCases2/UseCase3

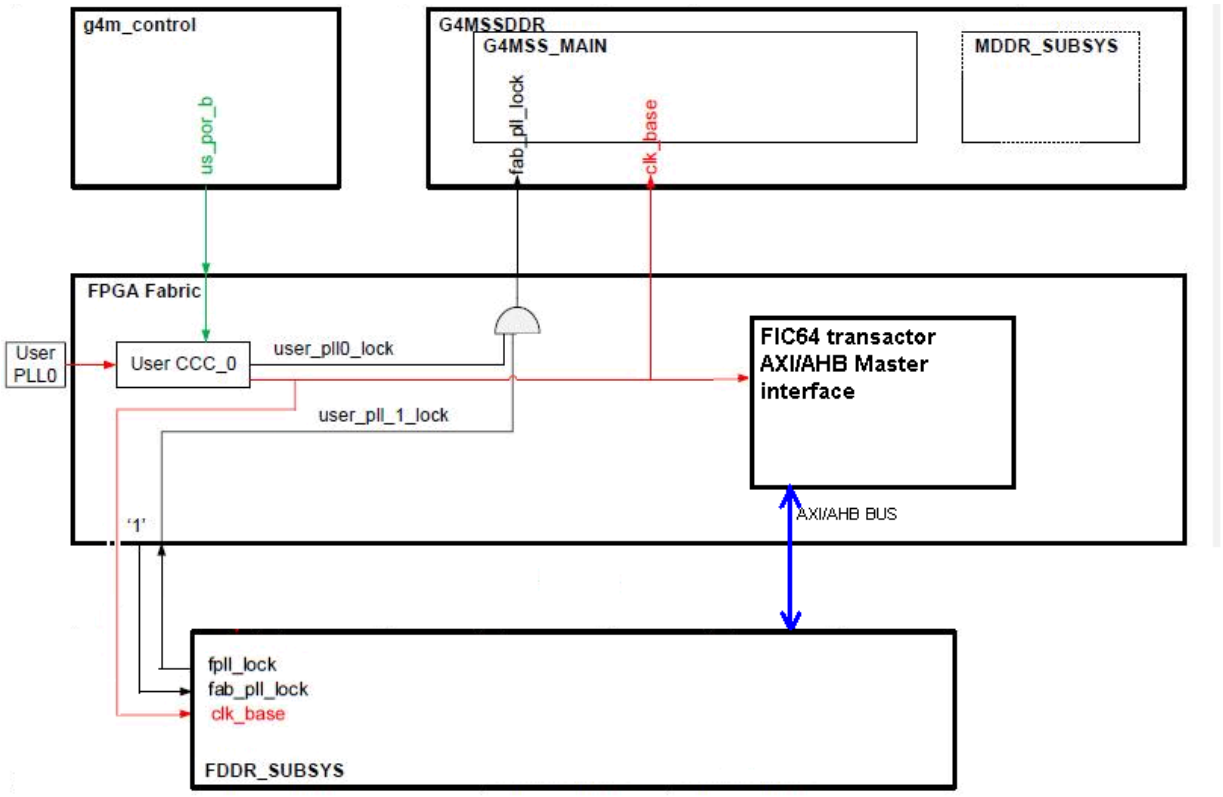

Figure 3 UseCase2/UseCase3 AXI/AHB interface setup

[redacted] Tool Flow

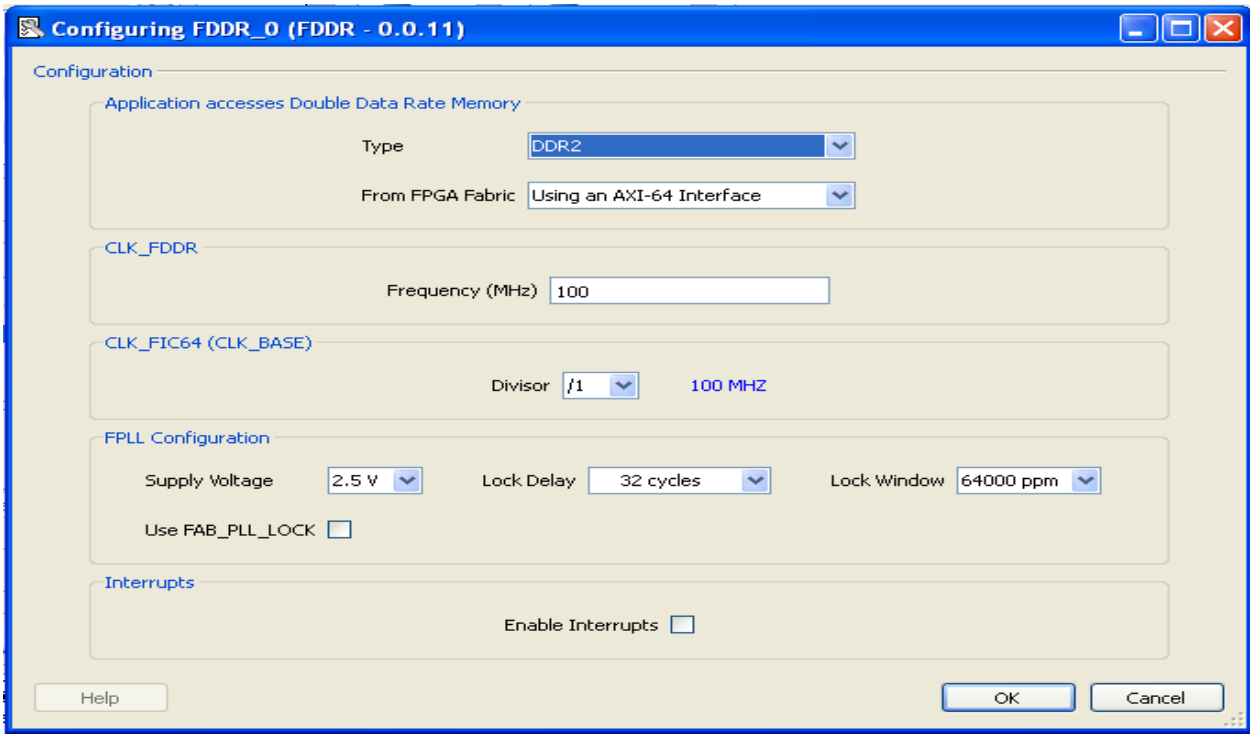

Figure 4 FDDR Configuration

4 Equipment Used

[redacted] *Hardware*

S.No	Equipment/Board	Qty	Remarks/Serial Number
1	G4M Validation Board	1	DVP-102-000304-001-RevB(labelled-B3) (Socket Board) With Silicon labelled 11(for Rev-A) With Silicon labelled 64(for Rev-B)
2	EWARM Debugger	1	S/No:158006667
3	Flashpro4	1	30000
4	USB to Micro USB cable	1	On G4M Validation board UART0 is connected via fabric to the PC via USB cable.
5	DC Power supply	1	FSP200-50PL-B (12V 5V) is used to power-up the G4M validation board
6	PC	1	Stand-alone PC wxp-svg-09

Table 2 Hardware Equipment used

[redacted] *Software*

UseCase	Libero Capture	MSS	FDDR	Silicon on Silicon
UseCase2a & 2b	10.9.1.20	0.0.662	0.0.523	Rev-A
UseCase2c	10.9.1.22	0.0.665	0.0.523	Rev-B(labelled 64)
USeCase3a & 3b	10.9.1.22	0.0.666	0.0.532	Rev-B(labelled 64)
UseCase4	10.9.1.20	0.0.662	0.0.523	Rev-A
UseCase5	10.9.3.10	0.0.720	0.0.616	Rev-C(labelled 119)
UseCase6	10.9.3.15	0.0.720	0.0.616	Rev-C(labelled 119)
UseCase7	10.9.3.10	0.0.720	0.0.616	Rev-C(labelled 119)

Table 3 Libero Equipment used

S.No	Tool	Version
1	EWARM(IAR)	Software version 6.0
2	Keil	uVision4
3	IAR	6.4

Table 4 Software Equipment used

- For FDDR validation G4Mvalidation board-DDR3 memory interface is used
- On board Micron memory used → **M**T41J256**M**8HX-15E:D TR

5 Use Models & Use Cases Test Phase

[redacted] *UseCase1- APB Configuration of FDDR*

5.1.1 Deviation from the Validation Plan

None

5.1.2 Implementation Guideline

Remapping is done to ESRAM.

DDR3 configuration is tested both for FDDR-AHB and FDDR-AXI mode.

Firmware is used to configure FDDR in DDR3 PHY-32, BL-8 and sequential mode.

5.1.3 Issues

None

5.1.4 PASS or FAIL criterion

Configuration validation is done by polling the status register in firmware.

Verified that status register reflects that FDDR is configured and FDDR is brought to normal mode.

Correctness of configuration is verified by read/write access to DDR3

5.1.5 Observation

AXI_Mode:
svn://hoppin/IP/PDV/G4_MAIN/G4M_FDDR/tags/1.0.102/results/Validation_Board/VB_UseCase2a.TXT

AHB Mode:
svn://hoppin/IP/PDV/G4_MAIN/G4M_FDDR/tags/1.0.102/results/Validation_Board/VB_UseCase3a.TXT

5.1.6 SVN Database

AXI-Mode:

svn://hoppin/IP/PDV/G4_MAIN/G4M_FDDR/tags/1.0.102/design/hw/Validation_Board/VB_UseCase2a/G4M_FDDR_AXI_333_ODT_ON_ODRIMP_4_Drive_12.zip

svn://hoppin/IP/PDV/G4_MAIN/G4M_FDDR/tags/1.0.102/design/fw/Validation_Board/VB_UseCase2a.zip

AHB Mode:

svn://hoppin/IP/PDV/G4_MAIN/G4M_FDDR/tags/1.0.102/design/hw/Validation_Board/VB_UseCase3a/FDDR_111MHz.zip

svn://hoppin/IP/PDV/G4_MAIN/G4M_FDDR/tags/1.0.102/design/fw/Validation_Board/VB_UseCase3a.zip

[redacted] *UseCase2- AXI Slave*

MDDR interface is configured in SDR-AXI mode and FDDR is connected to this AXI interface

Following usecases are validated as part of AXI Slave interface test

a) Read/write access to FDDR-DDR3 memory
b) Remapping to DDR3 and executing application out of DDR3
c) Dhrystone test (will be covered as part of Phase-II)

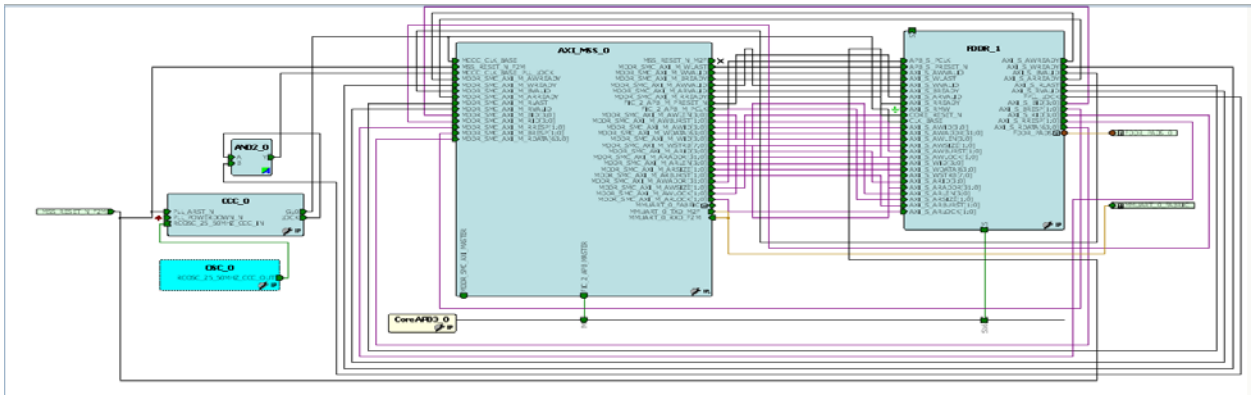

Figure 5 FDDR AXI Mode Setup

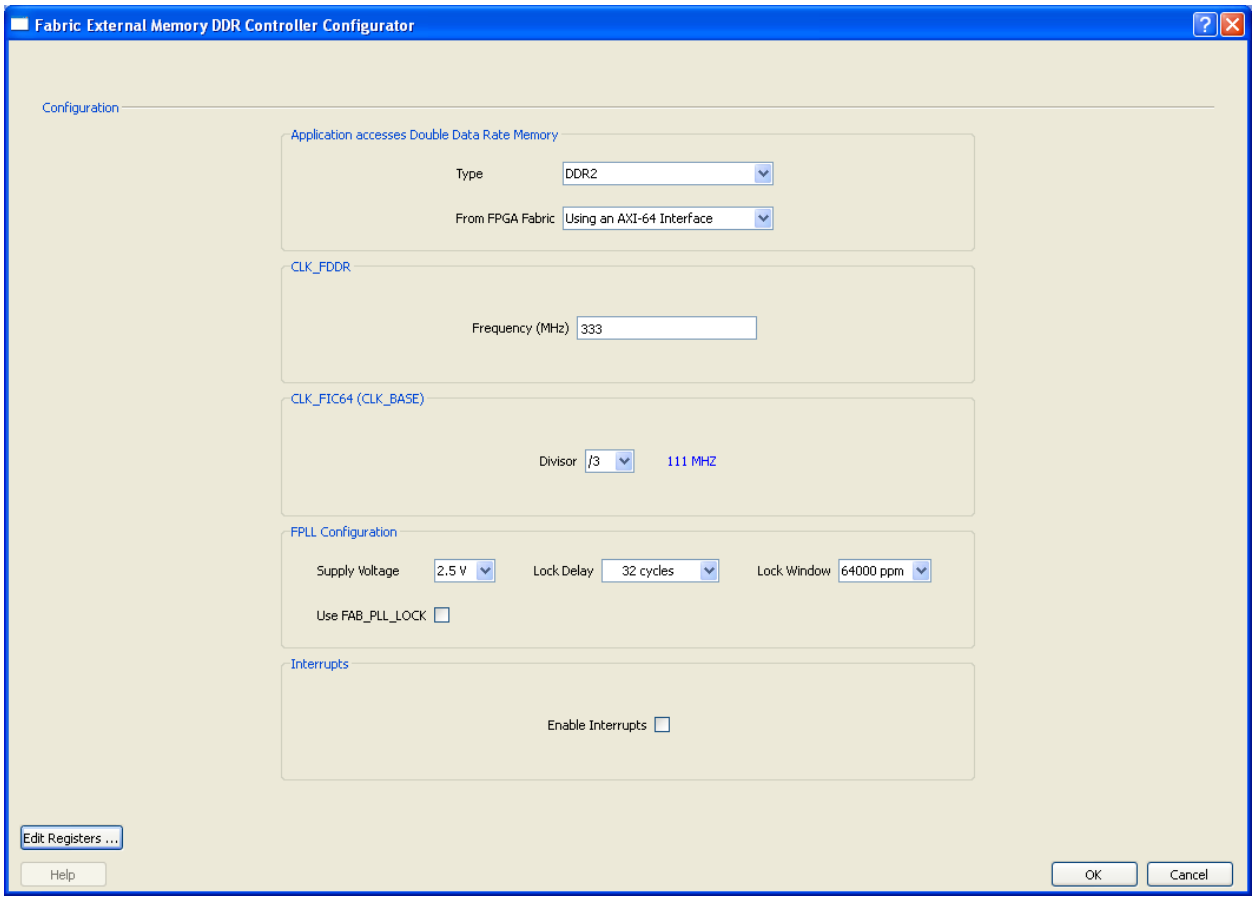

Figure 6 AXI Mode Configuration

5.2.1 Deviation from the Validation Plan

None

5.2.2 UseCase2a: AXI-Mode Read/Write access to FDDR-DDR3

5.2.2.1 Implementation Guideline

Following read/write access are verified as part of this test

- UseCase1 : Alternate read/write access
- UseCase2 : Read only data traffic
- UseCase3 : Write only data traffic
- UseCase4 : Simultaneous toggling of all data lines
- UseCase5 : Cross talk on data line
- UseCase6 : Soak testing

For details on the above test case implementation please refer
DDR_Characterization_Firmware_PLAN.docx

Firmware Implementation:

Remapping is done to ESRAM. Firmware is used to implement and execute the above usecases.

Both 32-bit and 16 bit access are validated with various data patterns (sequential, walking-1, walking-0 etc).

5.2.2.2 Issues

None

5.2.2.3 PASS or FAIL criterion

Access is verified for FDDR-DDR3 by reading the DATA written to memory and comparing it against the expected data (except for random data pattern) and the result of the test is displayed on UART terminal.

5.2.2.4 Observation

Copied from result log:

```
*********************************************

SmartFusion2- FDDR-DDR3 Characterization Firmware:


*********************************************

UseCase1 : Alternate read/write access

UseCase2 : Read only data traffic

UseCase3 : Write only data traffic

UseCase4 : Simultaneous toggling of all data lines

UseCase5 : Cross talk on data line

UseCase6 : Soak testing

Enter your choice (press 1,2, ... or 6): 1


 ALTERNATE READ/ WRITE ACCESS PASSED


*********************************************

SmartFusion2- FDDR-DDR3 Characterization Firmware:


*********************************************

UseCase1 : Alternate read/write access
```

UseCase2 : Read only data traffic

UseCase3 : Write only data traffic

UseCase4 : Simultaneous toggling of all data lines

UseCase5 : Cross talk on data line

UseCase6 : Soak testing

Enter your choice (press 1,2, ... or 6): 3

SELECT READ/WRITTE ACCESS MODE:

1. Word (32 bit) Access

2. Half-Word (16 bit) Access

Enter 1 or 2 accordingly : 1

SELECT READ/WRITTE DATA PATTERN:

1. Incrementing

2. Walking One Pattern

3. Walking Zero Pattern

4. Random Data (Read verify not implemented)

Enter 1,2,3 or 4 accordingly : 1

HPDMA READ DATA MATCH WITH WRITEN DATA --> TESTCASE PASSED

svn://hoppin/IP/PDV/G4_MAIN/G4M_FDDR/tags/1.0.102/results/Validation_Board/VB_UseCase2a.TXT

5.2.2.5 SVN Database

svn://hoppin/IP/PDV/G4_MAIN/G4M_FDDR/tags/1.0.102/design/hw/Validation_Board/VB_UseCase2a/G4M_FDDR_AXI_333_ODT_ON_ODRIMP_4_Drive_12.zip

svn://hoppin/IP/PDV/G4_MAIN/G4M_FDDR/tags/1.0.102/design/fw/Validation_Board/VB_UseCase2a.zip

5.2.3 UseCase2b: AXI-Mode: Remapping to FDDR-DDR3

5.2.3.1 Implementation Guideline

This usecase is validated as part of Dhrystone usecase. Keil debugger is used for this purpose.

Figure 7 shows the setup in which the initialization file (FDDR_DDR3.ini) is used to configure the FDDR in DDR3 mode, so that DDR configuration is done and is in normal mode before loading the application.

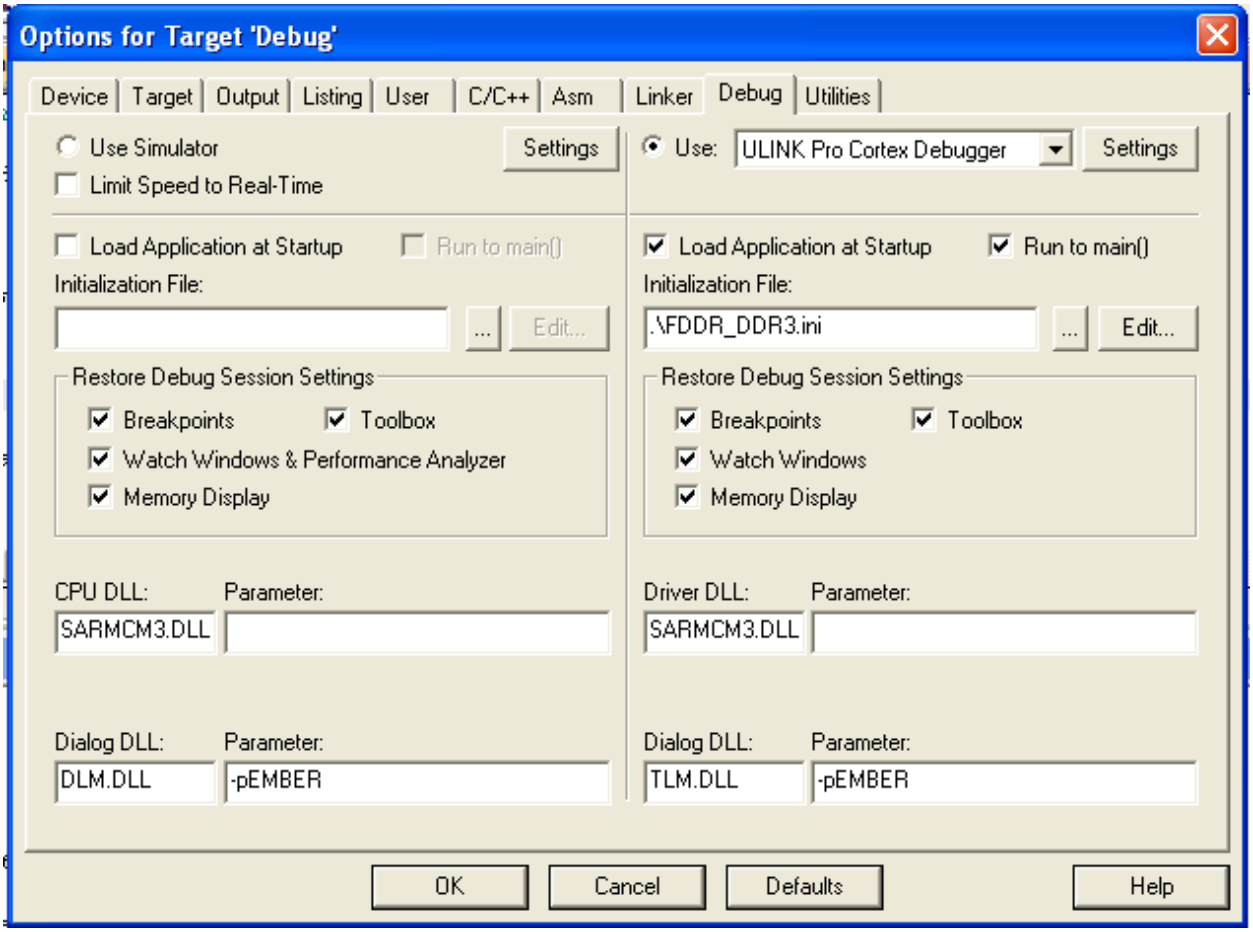

Figure 7 Keil Configuration

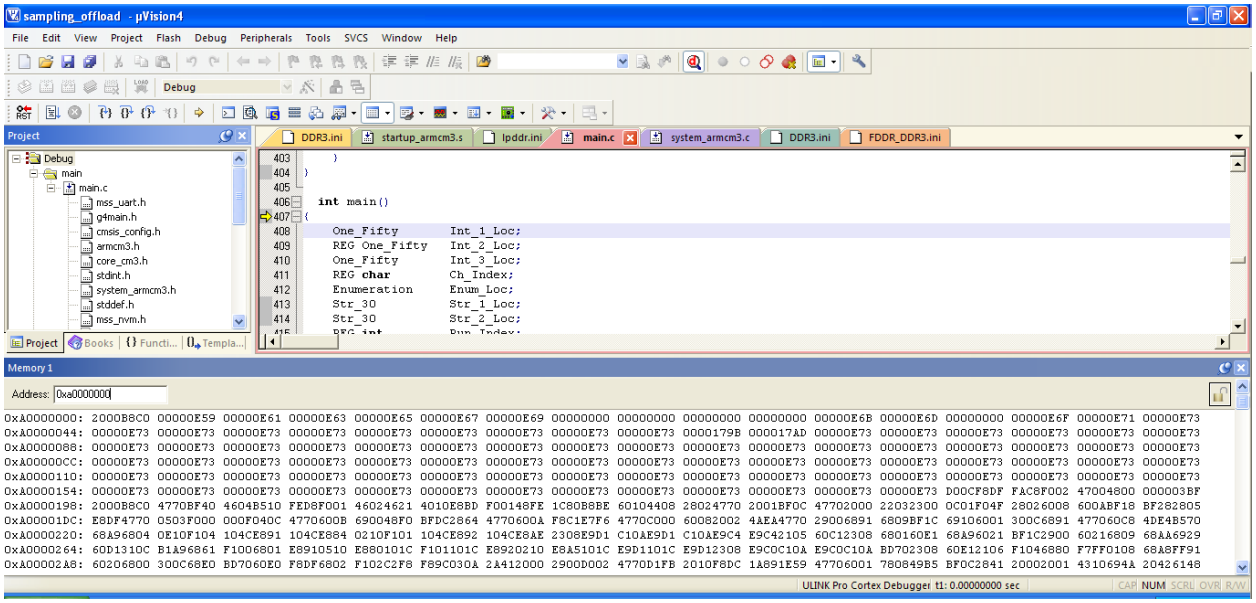

Figure 8 Remapping to FDDR (Code in DDR Memory)

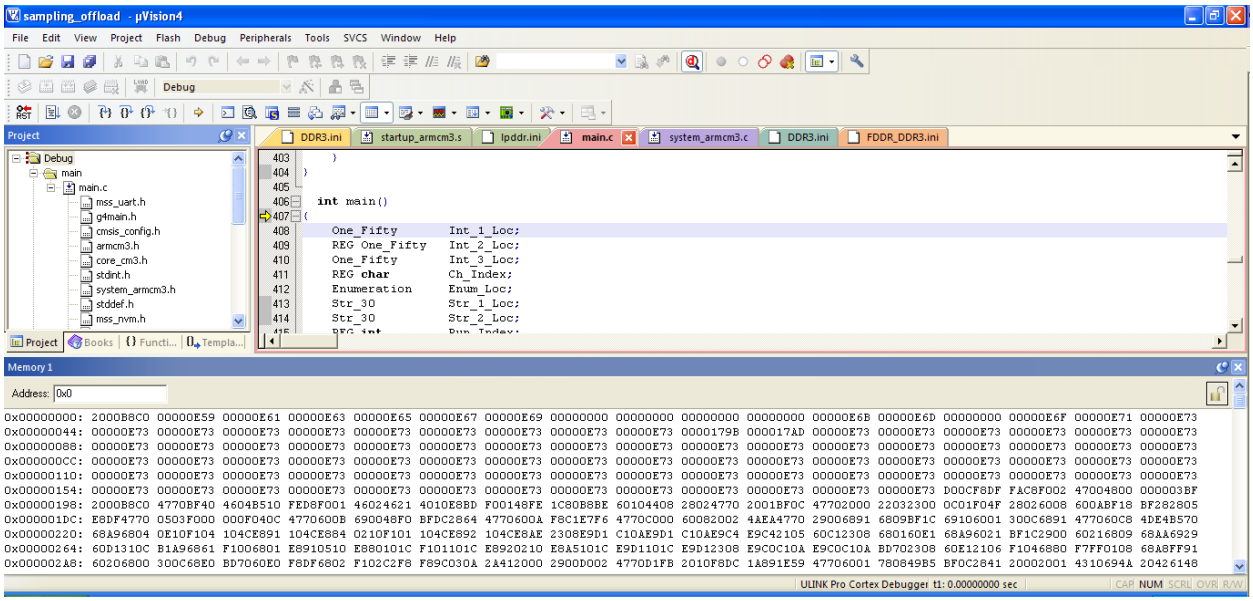

Figure 9 Remapping to FDDR (Code at offset 0x000)

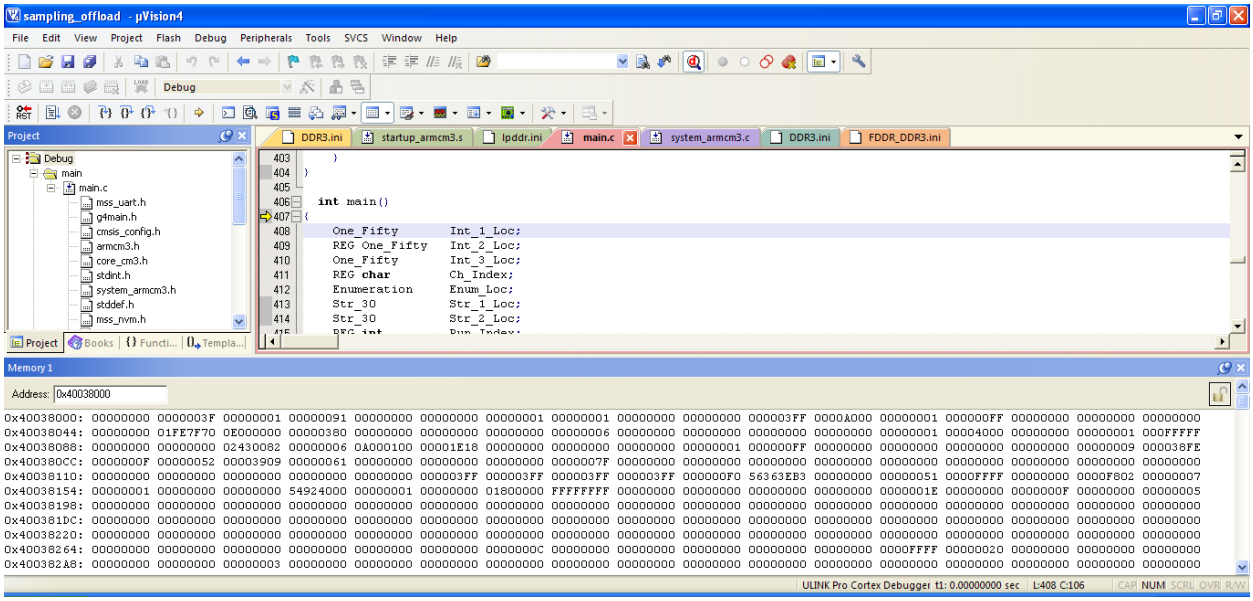

Figure 10 Sysreg configuration: offset 0x60 : FDDR interface to MSS configured in SDR-AXI Mode

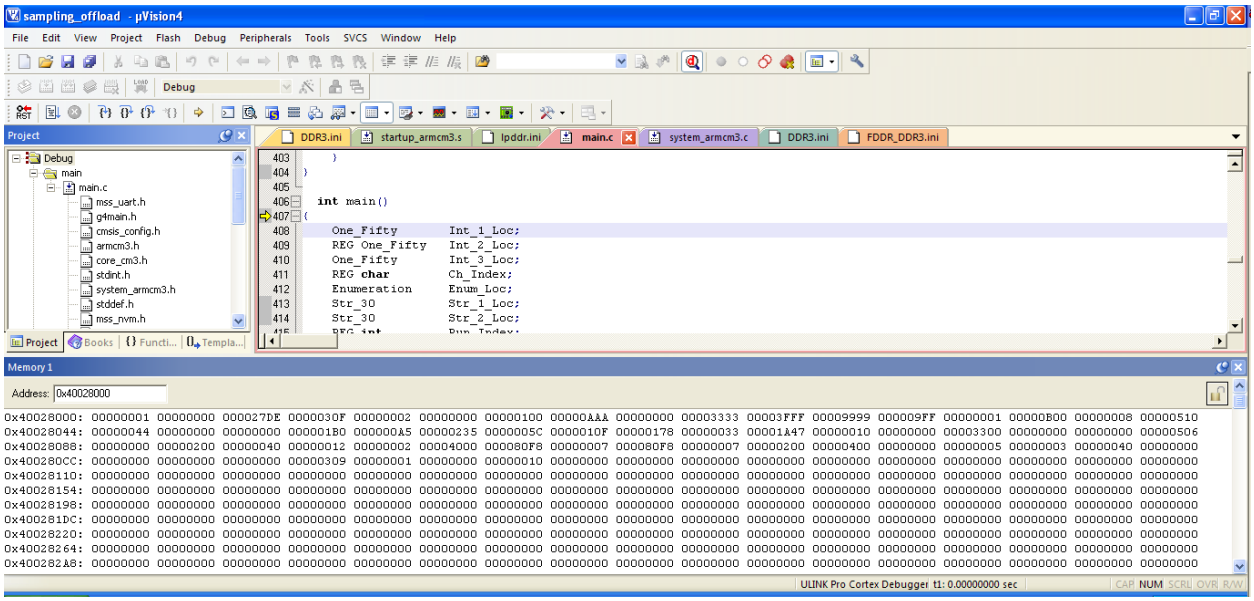

Figure 11 FDDR configuration Window

5.2.3.2 Issues

None

5.2.3.3 PASS or FAIL criterion

Same image at offset 0x0000 and in FDDR-DDR3 offset(0xA0000000)

Dhrystone application executed out of FDDR-DDR3 memory successfully when configured in AXI mode.

5.2.3.4 Observation

svn://hoppin/IP/PDV/G4_MAIN/G4M_FDDR/tags/1.0.102/results/Validation_Board/VB_UseCase2b.TXT

5.2.3.5 SVN Database

svn://hoppin/IP/PDV/G4_MAIN/G4M_FDDR/tags/1.0.102/design/hw/Validation_Board/VB_UseCase2b/G4M_FDDR_AXI_333_ODT_ON_ODRIMP_4_Drive_12.zip

svn://hoppin/IP/PDV/G4_MAIN/G4M_FDDR/tags/1.0.102/design/fw/Validation_Board/VB_UseCase2b.zip

5.2.4 UseCase2c: AXI-Mode: Dhrystone test

5.2.4.1 Implementation Guideline

UseCase covered in **G4M_Dhrystone_PDV_Result.docx**.

For details please refer Section 3.2.4 of G4M_Dhrystone_PDV_Result.docx

5.2.4.2 Issues

None

5.2.4.3 PASS or FAIL criterion

Covered in G4M_Dhrystone_PDV_Result.docx

5.2.4.4 Observation

Covered in[G4M_Dhrystone_PDV_Result.docx](#)

5.2.4.5 SVN Database

For details please refer Section 3.2.4 of [G4M_Dhrystone_PDV_Result.docx](#)

[redacted] *UseCase3- AHB Slave*

5.3.1 Implementation Guideline

Following usecases are validated as part of AHB Slave interface test

a) Read/write access to FDDR-DDR3 memory
b) Remapping to DDR3 and executing application out of DDR3
c) Dhrystone test (will be covered as part of Dhrystone PDV)

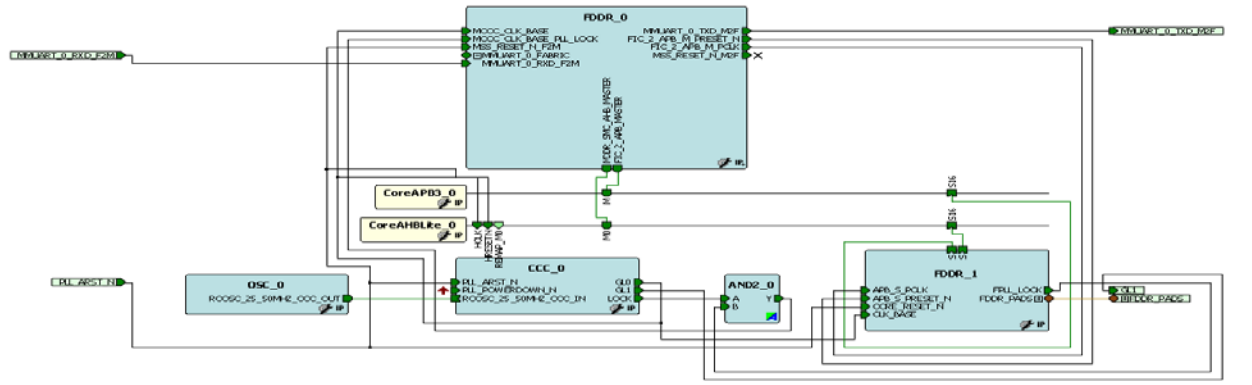

Figure 12 AHB Mode Setup

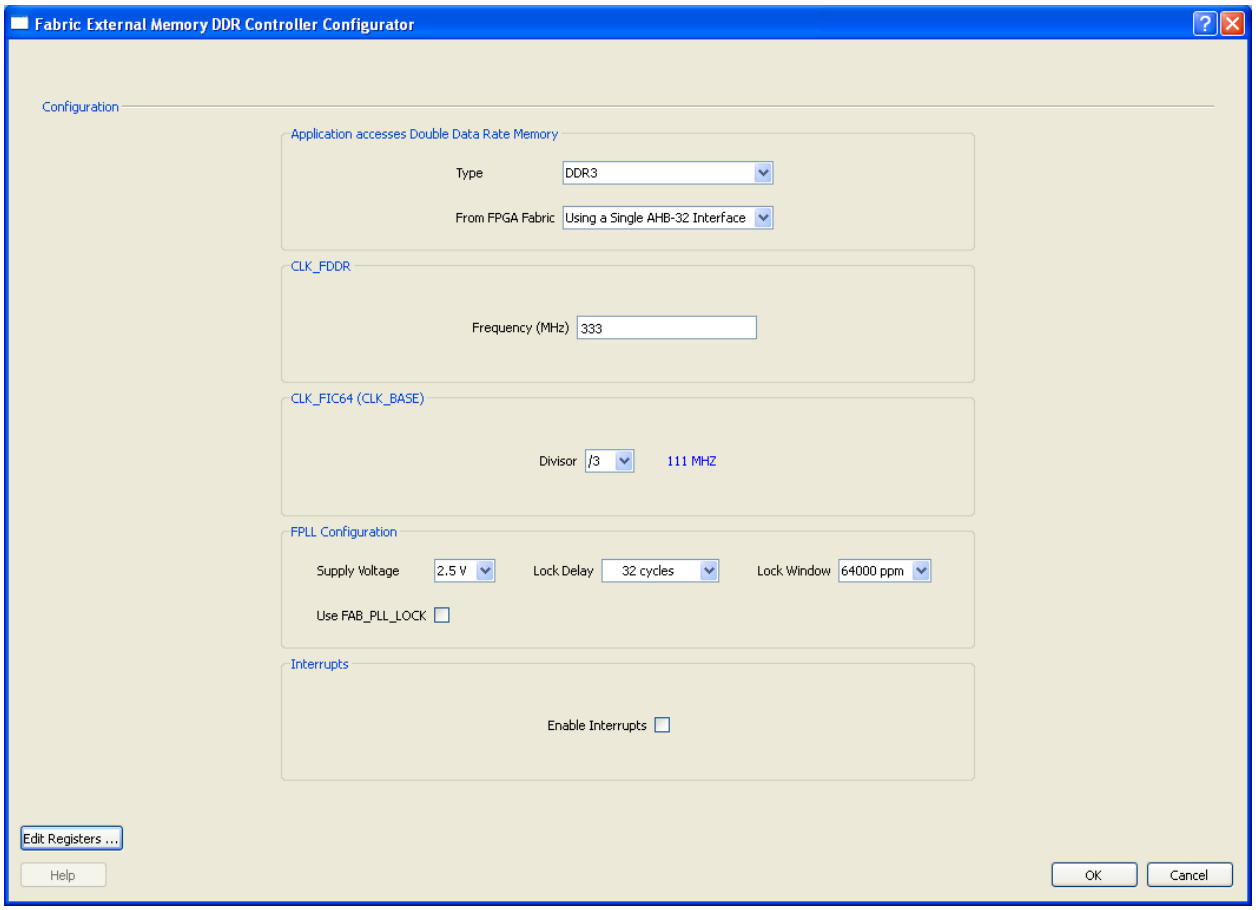

Figure 13 AHB Mode Configuration

5.3.2 Deviation from the Validation Plan

None

5.3.3 UseCase3a: AHB-Mode Read/Write access to FDDR-DDR3

5.3.3.1 Implementation Guideline

Following read/write access are verified as part of this test

- UseCase1 : Alternate read/write access
- UseCase2 : Read only data traffic
- UseCase3 : Write only data traffic
- UseCase4 : Simultaneous toggling of all data lines
- UseCase5 : Cross talk on data line
- UseCase6 : Soak testing

For details on the above test case implementation please refer
DDR_Characterization_Firmware_PLAN.docx

Firmware Implementation:

Remapping is done to ESRAM. Firmware is used to implement and execute the above usecases.

Both 32-bit and 16 bit access are validated with various data patterns (sequential, walking-1, walking-0 etc).

5.3.3.2 Issues

SAR 41364 - FDDR AHB mode read access fails for DDR3 memory → Issue resolved in MSS 0.0.666

5.3.3.3 PASS or FAIL criterion

Access is verified for FDDR-DDR3 by reading the DATA written to memory and comparing it against the expected data (except for random data pattern) and the result of the test is displayed on UART terminal.

5.3.3.4 Observation

Copied from result log:

G4Main says hello.

****

SmartFusion2- FDDR-DDR3 Characterization Firmware:

****

UseCase1 : Alternate read/write access

UseCase2 : Read only data traffic

UseCase3 : Write only data traffic

UseCase4 : Simultaneous toggling of all data lines

UseCase5 : Cross talk on data line

UseCase6 : Soak testing

Enter your choice (press 1,2, ... or 6): 1

ALTERNATE READ/ WRITE ACCESS PASSED

svn://hoppin/IP/PDV/G4_MAIN/G4M_FDDR/tags/1.0.102/results/Validation_Board/VB_UseCase3a.TXT

5.3.3.5 SVN Database

svn://hoppin/IP/PDV/G4_MAIN/G4M_FDDR/tags/1.0.102/design/hw/Validation_Board/VB_UseCase3a/FDDR_111MHz.zip

svn://hoppin/IP/PDV/G4_MAIN/G4M_FDDR/tags/1.0.102/design/fw/Validation_Board/VB_UseCase3a.zip

5.3.4 UseCase3b: AHB-Mode Remapping to FDDR-DDR3

5.3.4.1 Implementation Guideline

Figure 14 shows the IAR setup in which the initialization file (FDDR_DDR3.mac) is used to configure the FDDR in DDR3 mode, so that DDR configuration is done and is in normal mode before loading the application.

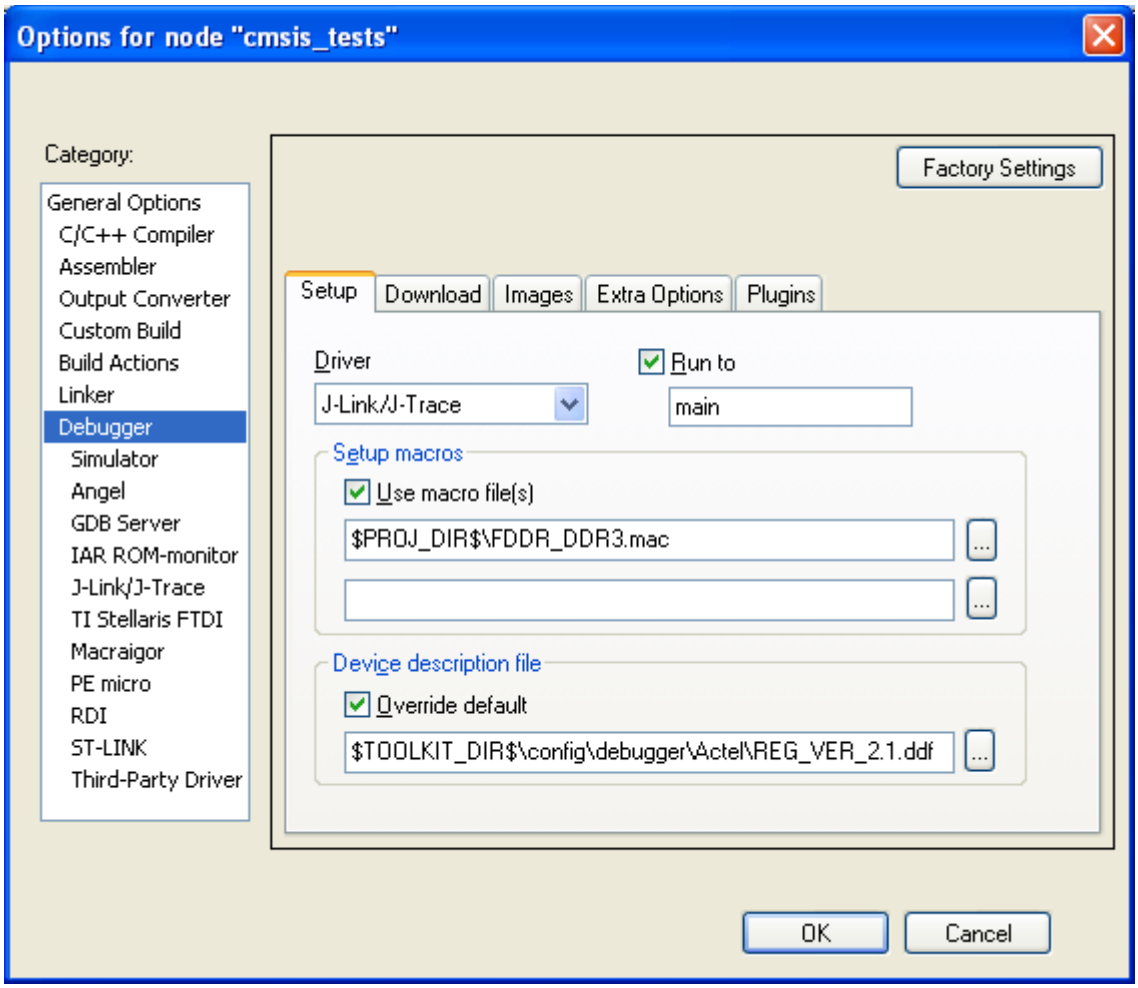

Figure 14 IAR option to configure FDDR through mac file

5.3.4.2 Issues

None

5.3.4.3 PASS or FAIL criterion

Application executed out of FDDR-DDR3 memory successfully when configured in AHB mode and UART display message is shown.

5.3.4.4 Observation

svn://hoppin/IP/PDV/G4_MAIN/G4M_FDDR/tags/1.0.102/results/Validation_Board/VB_UseCase3b.txt

5.3.4.5 SVN Database

svn://hoppin/IP/PDV/G4_MAIN/G4M_FDDR/tags/1.0.102/design/hw/Validation_Board/VB_UseCase3a/FDDR_111MHz.zip (hw project same as Usecase3a)

svn://hoppin/IP/PDV/G4_MAIN/G4M_FDDR/tags/1.0.102/design/fw/Validation_Board/VB_UseCase3b.zip

5.3.5 UseCase3c: AHB-Mode → Dhrystone test

This usecase will be covered as part of Dhrystone PDV.

[redacted] *UseCase4- FDDR Interrupt Validation*

5.4.1 Deviation from the Validation Plan

None

5.4.2 Implementation Guideline

Same as UseCase2b

5.4.3 Issues

None

5.4.4 PASS or FAIL criterion

PLL Lock (PLL_LOCK_INT) interrupt is brought to the LED output. And the LED is switched OFF when PLL_LOCK_INT is set and is on when lock is not set

5.4.5 Observation

svn://hoppin/IP/PDV/G4_MAIN/G4M_FDDR/tags/1.0.102/results/Validation_Board/VB_UseCase2b.TXT

5.4.6 SVN Database

svn://hoppin/IP/PDV/G4_MAIN/G4M_FDDR/tags/1.0.102/design/hw/Validation_Board/VB_UseCase2b/G4M_FDDR_AXI_333_ODT_ON_ODRIMP_4_Drive_12.zip

svn://hoppin/IP/PDV/G4_MAIN/G4M_FDDR/tags/1.0.102/design/fw/Validation_Board/VB_UseCase2a.zip

[redacted] *UseCase5- FDDR AXI Fabric Master*

5.5.1 Deviation from the Validation Plan

None

5.5.2 Implementation Guideline

Fabric master (AXI transactor) is used to access FDDR_DDR3 memory. MSS is running at 50MHz and fabric design and FDDR is running at 100MHz.

Fabric transactor is controlled by CM3 to write the type of AXI transactions to be performed by fabric master to FDDR.

Following read/write access are executed by fabric master to FDDR.

1) AXI -> 16 back to back transactions : Incremental read write access is performed with a burst length of 16
2) AXI -> INCR transfers: Incremental read write access is performed with a burst length of 8
3) AXI -> WRAP transfers: Wrap write access is performed with offset 0xA0000004 followed by incremental read access with burst length of 8.

Overlapped access is taken care by transactor block.

For read access the data is read from FDDR memory and stored at offset 0x50002000.

5.5.3 Issues

None

5.5.4 PASS or FAIL criterion

FDDR access is verified by reading the data written to FDDR. The data read is stored at offset 0x50002000 and displayed to terminal

5.5.5 Observation

svn://hoppin/IP/PDV/G4_MAIN/G4M_FDDR/tags/1.0.103/results/Validation_Board/VB_USeCase5/FDDR_FIC64_AXI

5.5.6 SVN Database

svn://hoppin/IP/PDV/G4_MAIN/G4M_FDDR/tags/1.0.103/design/hw/Validation_Board/VB_UseCase5/FDDR_FIC64_AXI_Overlapread.zip

svn://hoppin/IP/PDV/G4_MAIN/G4M_FDDR/tags/1.0.103/design/fw/Validation_Board/VB_UseCase5/FDDR_FIC64_AXI.zip

[redacted] *UseCase6- FDDR ABH_1 Fabric Master Access*

5.6.1 Deviation from the Validation Plan

None

5.6.2 Implementation Guideline

FDDR is configured in single AHB mode.

Fabric master (AHB transactor) is used to access FDDR_DDR3 memory. MSS and FDDR are running at 80MHz.

Fabric transactor is controlled by CM3 to write the type of AHB transactions to be performed by fabric master to FDDR.

Following read/write access are executed by fabric master to FDDR.

1) AHB Test: 16 back to back transactions → 16 back to back transactions : Incremental read write access is performed with a burst length of 16. Four such bursts are generated
2) AHB Test: INCR Write Access & INCR Read Access → Incremental read write access is performed with a burst length of 8. Four such bursts are generated
3) AHB Test: WRAP Write Access & INCR Read Access → Wrap write access is performed with offset 0xA0000004 followed by incremental read access with burst length of 8. Four such bursts are generated

For read access the data is read from FDDR memory and stored at offset 0x50002000.

5.6.3 Issues

None

5.6.4 PASS or FAIL criterion

FDDR access is verified by reading the data written to FDDR.

5.6.5 Observation

svn://hoppin/IP/PDV/G4_MAIN/G4M_FDDR/tags/1.0.103/results/Validation_Board/VB_UseCase6

5.6.6 SVN Database

svn://hoppin/IP/PDV/G4_MAIN/G4M_FDDR/tags/1.0.103/design/fw/Validation_Board/VB_UseCase6/IAR.zip

svn://hoppin/IP/PDV/G4_MAIN/G4M_FDDR/tags/1.0.103/design/hw/Validation_Board/VB_UseCase6/revC_FIC64_Single_AHB.zip

[redacted] *UseCase7- FDDR AHBL_1 and AHBL_2 Fabric Master Access*

5.7.1 Deviation from the Validation Plan

None

5.7.2 Implementation Guideline

FDDR is configured in dual AHB mode.

Fabric master (two AHB transactors) is used to access FDDR_DDR3 memory. MSS and FDDR are running at 80MHz.

Fabric transactor is controlled by CM3 to write the type of AHB transactions to be performed by fabric master to FDDR.

Following read/write access are executed by fabric master to FDDR.

1) AHB Test: 16 back to back transactions → 16 back to back transactions : Incremental read write access is performed with a burst length of 16
2) AHB Test: INCR Write Access & INCR Read Access → Incremental read write access is performed with a burst length of 8
3) AHB Test: WRAP Write Access & INCR Read Access → Wrap write access is performed with offset 0xA0000004 followed by incremental read access with burst length of 8.

For read access the data is read from FDDR memory and stored at offset 0x50002000 and 0x70002000.

5.7.3 Issues

None on FDDR

There are some known issues in the Fabric Master, transactor

- Last word of burst is not written/read.
- When more than 1 burst access are generated, RxRAM of transactor is not reading the contents from second burst.

5.7.4 PASS or FAIL criterion

FDDR access is verified by reading the data written to FDDR.

5.7.5 Observation

svn://hoppin/IP/PDV/G4_MAIN/G4M_FDDR/tags/1.0.103/results/Validation_Board/VB_UseCase7

5.7.6 SVN Database

svn://hoppin/IP/PDV/G4_MAIN/G4M_FDDR/tags/1.0.103/design/fw/Validation_Board/VB_UseCase7/IAR.zip

svn://hoppin/IP/PDV/G4_MAIN/G4M_FDDR/tags/1.0.103/design/hw/Validation_Board/VB_UseCase7/FIC64_dual_AHB.zip

[redacted] *A2F5000 FDDR Validation Summary*

UseModel	Feature under validation	Result	Issues/Comments
UseCase1	APB Configuration of FDDR	Passed	None
UseCase2a	AXI Slave→ Read/write Access	Passed	None
UseCase2b	AXI Slave → Remapping to FDDR	Passed	NA
UseCase2c	AXI Slave → Dhrystone test	Passed	None
UseCase3a	AHB Slave → Read/write Access	Passed	SAR 41364
UseCase3b	AHB Slave → Remapping to FDDR	Passed	SAR 41364
UseCase3c	AHB Slave → Dhrystone test	Phase-III Low priority	NA
UseCase4	FDDR Interrupt Validation	Passed	None
UseCase5	AXI Fabric Master Access	Passed	None
UseCase6	ABH_1 Fabric Master Access	Passed	None
UseCase7	Both AHBL_1 and AHBL_2 Fabric Master Access	Passed	None

Table 5 List of UseCases

6 SAR Summary

SAR	Description	Detected Phase	Issue Revision Number
41364	FDDR AHB mode read access fails for DDR3 memory	Pre-ES Post-Mask Making	Rev A