AT40K Check Function on Configuration

Description

The AT40K family supports a check function in mode 2 configuration SRAM data (a write verify). This is accomplished by normally initiating a configuration download while driving CHECK low. Instead of writing the contents of the bitstream to the memory, the contents of the memory are read and compared to the bitstream on a byte-by-byte basis in the configuration logic. Any differences are reported by driving the INIT pin low. The INIT pin will lower two clocks after the miscompare. The check function is available after power-on-reset and manual reset, and can be performed on an "empty" FPGA prior to the first programming of the device. Windowed or non-windowed bitstreams may be checked. Although the check function does not write the FPGA SRAM contents, the configuration control register is written. The configuration control register is not checked, as they are in every download, but only the data at those addresses is "checked". The contents of the Checksum registers cannot be verified with the check function.

Check Function in Mode 2

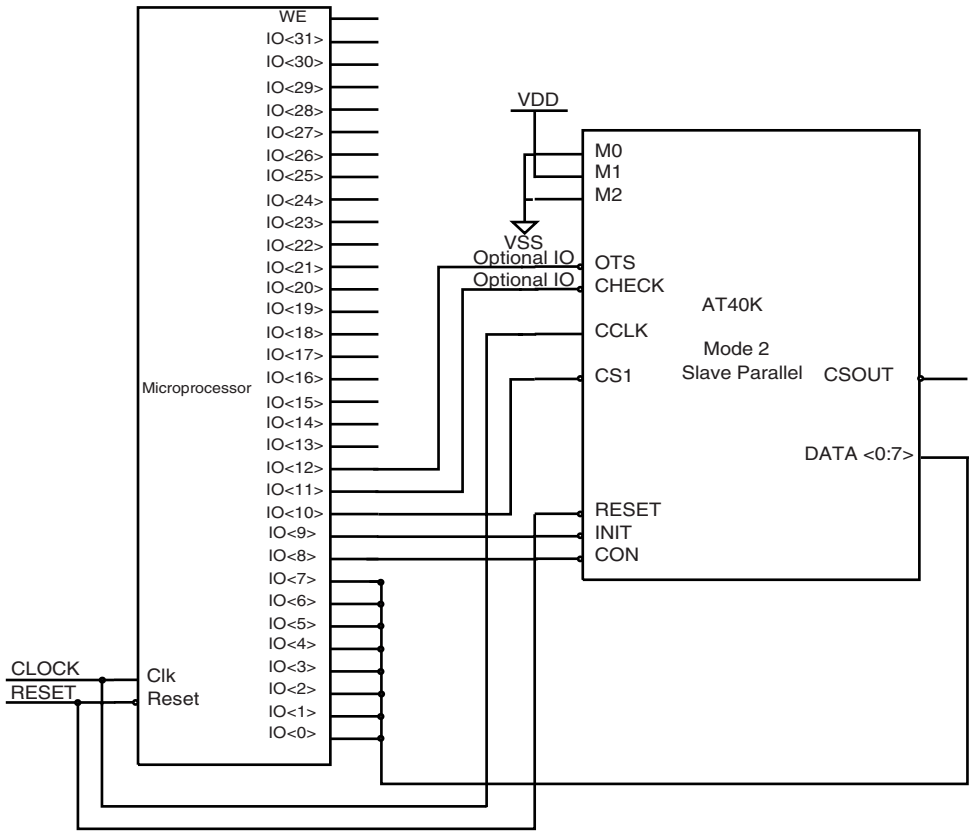
A mode 2 slave parallel device can be configured in a system in two ways: a standalone or cascade scheme whereby data comes from a microprocessor, see Figure 1 on page 2; or a cascade scheme where the data is driven by a parallel PROM, and the FPGA is usually downstream from a mode 6 device. Figure 2 on page 3 shows a 6-2 cascade system application.

AT40K FPGAs

Application Note

Rev. 2293A–04/01

Figure 1. Standalone Microprocessor



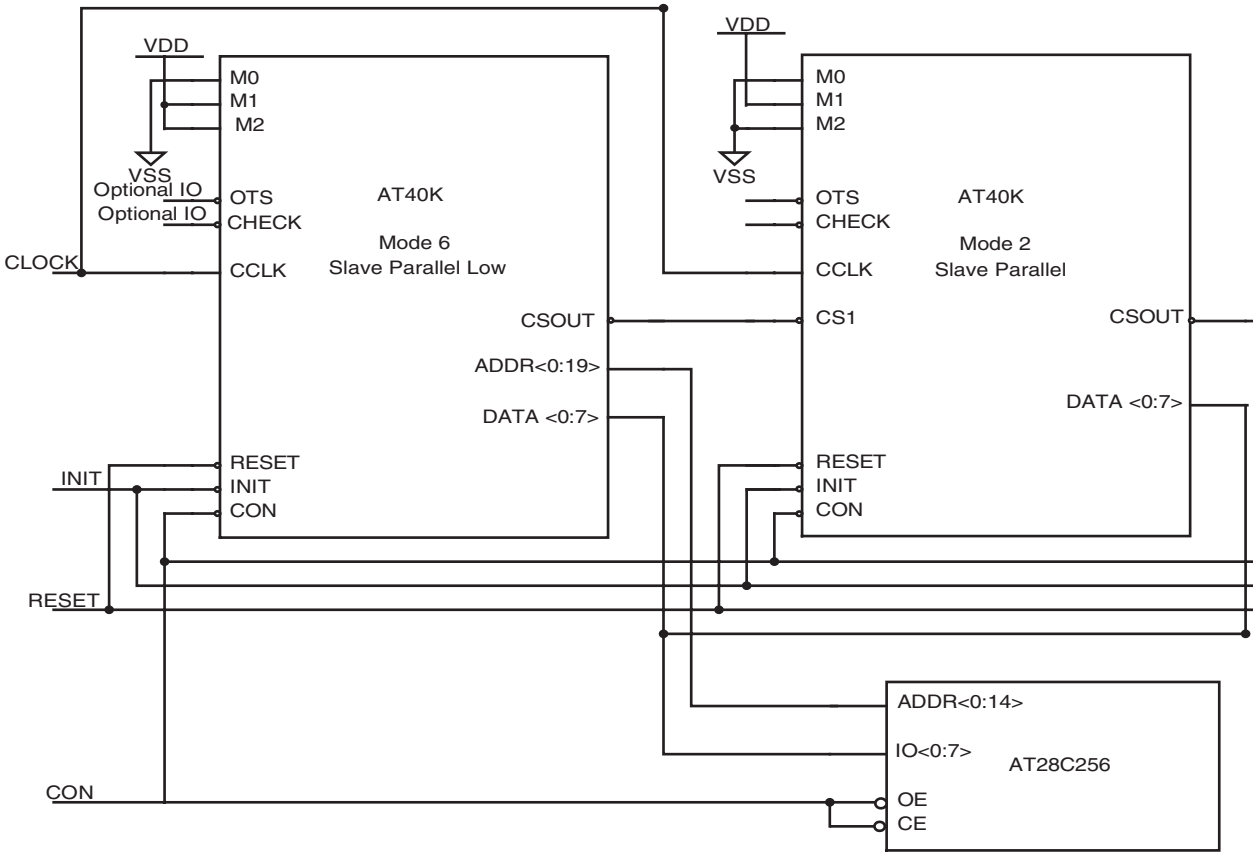
Board Setup and Configuration Requirements

This application note has been implemented using a parallel EEPROM as the configuration data source on a cascade 6-2 Parallel EEPROM circuit. Other sources such as a microprocessor, an EPROM, and a PROM can also be used.

The maximum CCLK frequency when performing a check function is much lower than that of a normal download. During check function, CCLK should be lower than 1 MHZ. Exact timing specifications are listed under the mode description in the AT40K FPGA application note.

Make sure the FPGA is set up for mode 2 before applying power to the board, see Figure 2 on page 3. To configure a device, set M2=1, M1=1, M0=0 and CS=0 for mode 6, and M2=0, M1=1, M0=0 and CS=0 for mode 2 FPGA.

Figure 2. Cascade 6-2 Parallel EEPROM



Initiating Configuration

Instructions for using IDS to generate the cascade bitstream with check function option set:

1. From Figaro, choose **Option** -> **Option**. Select AT40K bitstream. Under the **Configuration Register** window, deselect **B2 Cascade Disabled** and **B3 Check Function Disabled**.
2. Make another copy of the bitstream file from the same design with a different name (for example, design1_a.bst and design1_b.bst). From Figaro, choose **Tool** -> **Bitstream** -> **Cascade**. Select the two different name bitstreams (remember the two different bitstreams are from the same design). Figaro will combine the two bitstream files into a single bitstream. The purpose of doing this is because we want to compare this bitstream file using the check function feature in AT40K.
3. Program the file to the AT28C512 using a third party programmer.
4. Prepare a second bitstream to program the second EPROM for comparison (for example, design2_a.bst and design2_b.bst). When creating the second bitstream, use a different design for the second bitstream. This is used for producing failure when doing comparison of two bitstreams (EPROMs).

Verify the Check Function in Mode 2

1. Have the logic analyzer setup ready. The CON, CS1, CHECK, INIT and the output of the design should be monitored on screen.
2. Set the trigger mode on CON signal and hit run, then power up the board. The output of the design should be displayed.
3. Leave the power ON, otherwise, the contents of the FPGA will be lost. Changes trigger mode to be LOW on INIT signal and pull the CHECK pin to GND. Leave the EPROM in place. Reset the configuration data source and drive the CON pin to LOW to reconfigure the device. This will force the FPGA to compare the same bitstream (EPROM) using check function. If there is no difference on the two bitstreams, nothing will display since any bitstream errors cause the INIT pin to drive low (see Figure 3).
4. Trigger the CON signal to LOW and power up the board. The original bitstream is downloaded on the FPGA. (design1_a.bst and design1_b.bst). Change the trigger mode on INIT signal to LOW and replace with the second EPROM (design2_a.bst and design2_b.bst). Reset the data source and drive the CON pin to LOW to start reconfiguration. Remember to use the second bitstream instead of the first one because our goal is to compare the two different bitstreams (EPROMs). INIT signal will be trigger by the FPGA since we are comparing two different bitstreams (EPROMs) (see Figure 4 on page 5).

Figure 3. Compared to its Own Bitstream

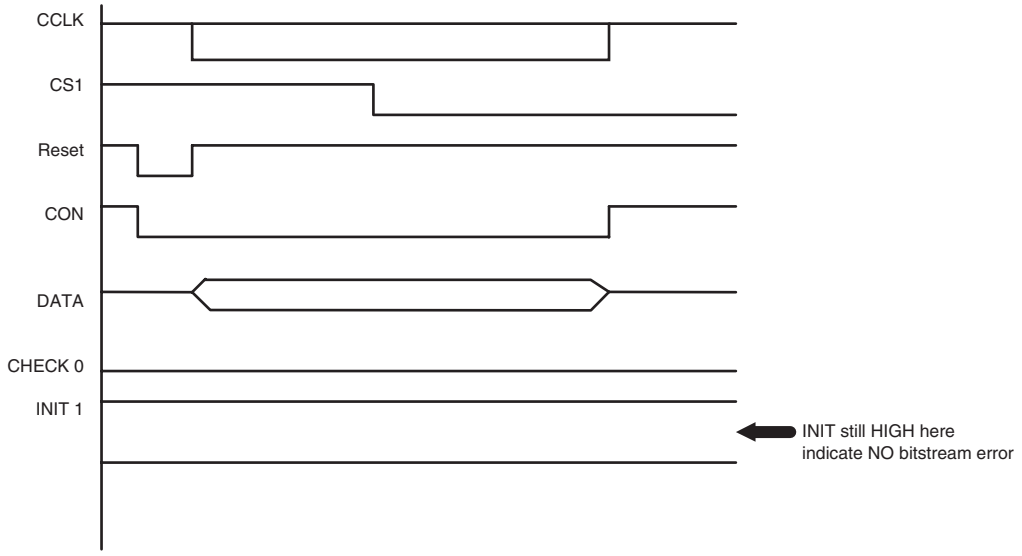
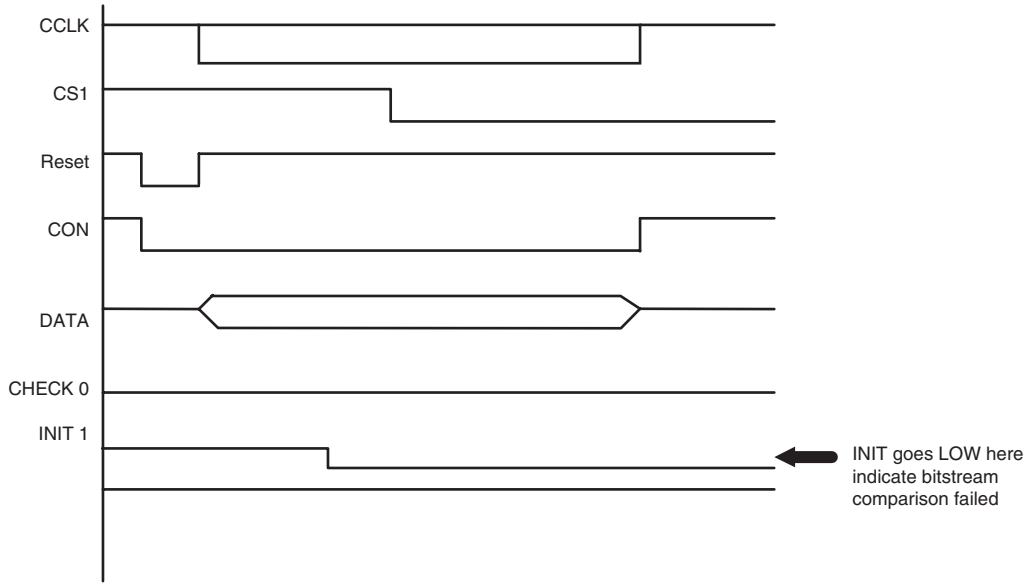


Figure 4. Compared Two Different Bitstreams



Bitstream Errors

The INIT pin is driven low by the FPGA for a number of reasons. In all cases, the INIT pin will be driven low two clocks after the byte that caused the error. Some errors will cause a bitstream to be terminated. Some will not. If a bitstream is terminated, all configuration pins are released by the configuration logic, and the configuration state returns to Idle.

A bad preamble causes the INIT pin to be driven low, and causes the download to be terminated.

A bad window start address or end address causes the INIT pin to be driven low two clocks after the third byte of the end address is seen by the device. The download is terminated.

During a check function, a mismatched write-verify error results in the INIT pin being driven low two clocks after the byte. The INIT will remain low until the end of the bitstream. The download will NOT terminate.

If the security flag bit was set in the previous bitstream, the FPGA will drive the INIT pin low two clocks after CON was driven low by the user. The download will immediately terminate.

If a checksum error is detected during a bitstream download, the INIT is driven low two clocks after the write to the Checksum page. The INIT pin will remain low until the end of the bitstream. The download will not terminate.

Full vs. Partial Bitstreams

When programming an AT40K series FPGA, the user will normally load the entire configuration SRAM memory map from start to finish. This requires a full bitstream. Bitstream sizes are shown in Table 1.

Table 1. AT40K Series Bitstream Sizes

Device	Array Size	Bytes	Bits
AT40K05	16 x 16	5263	42104
AT40K10	24 x 24	11175	89400
AT40K20	32 x 32	19279	154232
AT40K40	48 x 48	42603	336504

It is possible, by using the windowing mechanism, to download the SRAM memory map in smaller segments. The user may load portions of the array before others, eliminate the loading of unused portions of the array and overwrite previously written portions of configuration SRAM with new design information.

AT40K software tools (Atmel's FPGA integrated development system) supports bitstream compression.

Procedure to generate a compress bitstream using IDS software

1. Compile the design as usual and it will generate a normal (Full) bitstream file.
2. Under **Tools** pull-down menu on Figaro, select **bitstream**, **compress**.
3. Select the design.bst bitstream file.
4. The final bitstream file will be compressed and will overwrite the original file.

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