Image Enhancement IP User Guide

Introduction (Ask a Question)

The Image Enhancement IP (Intellectual Property) for the PolarFire FPGA Video and Imaging Kit is a suite of algorithms and techniques used to improve the quality of images and videos. It includes features such as noise reduction, color enhancement, sharpening, scaling, and interlacing.

The Image Enhancement IP can process images in real-time, making it ideal for applications that require immediate feedback, such as video surveillance, machine vision, and medical imaging. It is also highly configurable, allowing developers to fine-tune the image enhancement process to meet their specific needs.

The PolarFire FPGA Video and Imaging Kit, combined with the Image Enhancement IP, provides a powerful and flexible platform for developing advanced image and video processing applications. It offers high performance, low power consumption, and a small form factor, making it a great choice for a wide range of applications.

Image Enhancement IP enables you to adjust the brightness, contrast, and color balance of a final video Image according to personal preferences. These calculations are done in the RGB domain.

The inputs to Image Enhancement IP in terms of brightness and contrast are as follows:

$R\_CONST\_I = (R_{gain} \times contrast\_factor) / 10$

$G\_CONST\_I = (G_{gain} \times contrast\_factor) / 10$

$B\_CONST\_I = (B_{gain} \times contrast\_factor) / 10$

$COMMON\_CONST\_I = 128 \times (brightness - ((128 \times contrast\_factor) / 10))$

where,

$$contrast\_factor = \frac{325 \times (contrast + 128)}{(387 - contrast) \times 32}$$

R_{gain}, G_{gain}, and B_{gain} are the red, green, and blue gain values.

The output RGB values are calculated from the preceding inputs based on the following equations:

$R_{out} = (COMMON\_CONST\_I + R\_CONST\_I \times R_{in}) / 128$

$G_{out} = (COMMON\_CONST\_I + R\_CONST\_I \times G_{in}) / 128$

$B_{out} = (COMMON\_CONST\_I + R\_CONST\_I \times B_{in}) / 128$

where,

R_{in}, G_{in}, and B_{in} are the red, green, and blue values of input data.

R_{out}, G_{out}, and B_{out} are the red, green, and blue values of output data.

Image Enhancement Summary

Core Version	This document applies to Image Enhancement v4.6.
Supported Device Families	• PolarFire® SoC • PolarFire • RTG4™ • IGLOO® 2 • SmartFusion® 2
Supported Tool Flow	Requires Libero® SoC v12.0 or later releases.
Supported Interfaces	• AXI4-Lite Configuration Interface • AXI4 Stream Video Interface
Licensing	Image Enhancement clear RTL is license locked, and the encrypted RTL is available for free. **Encrypted** Complete RTL code is provided for the core, allowing it to be instantiated with the SmartDesign tool. Simulation, synthesis, and layout can be performed within Libero System-on-Chip (SoC). The RTL code is encrypted for the core. **RTL** Complete RTL source code is provided for the core.
Installation Instructions	Image Enhancement must be installed to the IP Catalog automatically through the IP Catalog update function. Alternatively, Image Enhancement could be manually downloaded from the catalog. Once the IP core is installed, it is configured, generated, and instantiated for inclusion in the project.
Device Utilization and Performance	A summary of utilization and performance information for image enhancement is listed in Device Utilization.

Key Features (Ask a Question)

Image Enhancement supports the following key feature:

- Supports image enhancement in terms of brightness, contrast, saturation, and hue
- Supports 1 pixel and 4 pixel configuration
- Supports color depth of 8/10/12/16 bit per color channel (red, green, and blue)
- Supports AXI4-Lite Configuration Interface for parameter modification
- Supports Native and AXI4 Stream Video Interface for video data transfer
- Supports Full HD resolution @60fps in 1 pixel mode
- Supports 4k resolution @60fps in 4 pixel mode

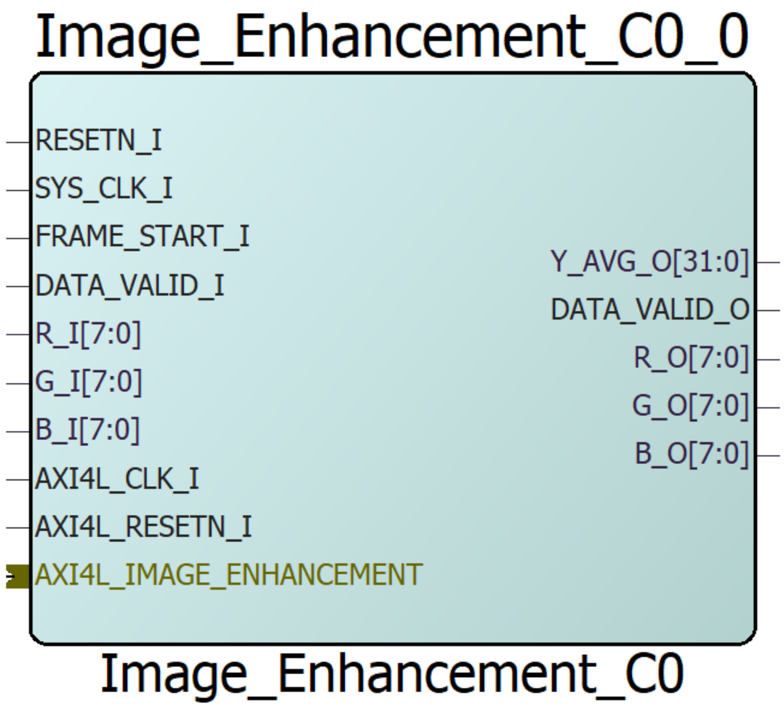
Table of Contents

1. Functional Description (Ask a Question)

This section describes the design inputs and outputs of the Image Enhancement IP.

The following figure shows the input and output ports of the Image Enhancement IP for 1 pixel, with 8-bit color depth, in native video interface.

Figure 1-1. Block Diagram Image Enhancement IP



When the DATA_VALID_I signal goes high, the R, G, and B values of the output are computed from the inputs, according to the formula given in the introduction section. The output RGB data (R_O, G_O, and B_O) is valid when the DATA_VALID_O goes high.

2. IP Core Parameters and Interface Signals (Ask a Question)

This section describes the ports and configuration parameters of the Image Enhancement IP.

2.1. Configuration Settings (Ask a Question)

The following table lists the configuration parameters used in the hardware implementation of the Image Enhancement. These parameters are generic and can be varied based on the application requirement. The default Red, Green, Blue, and common constant values can be configured in the configurator and these values will be used unless overwritten through AXI4-Lite interface.

Table 2-1. Configuration Parameters

Parameter Name	Description
Number of pixels	Number of pixels, per clock, processed by the IP Currently it can process 1 or 4 pixels.
Configuration Interface	IP can be configured using the Native interface or through the AXI4-Lite interface.
Video Interface	Video can be streamed either in native video interface, exposing individual signals, or can be streamed using the AXI4 stream interface easing connectivity.
Color Depth (per color channel)	Each color channel (red, green and blue) supports 8/10/12/16 bit color depth.
Red Constant	Input constant to be multiplied with the red color channel data component
Green Constant	Input constant to be multiplied with the green color channel data component
Blue Constant	Input constant to be multiplied with the blue color channel data component
Common Constant	Input constant with brightness and contrast

The following figures show the IP configurator information of Image Enhancement IP.

Figure 2-1. Image Enhancement IP - Configuration Tab

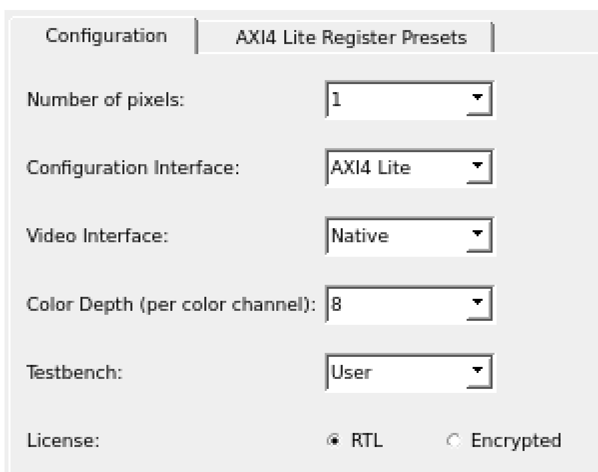
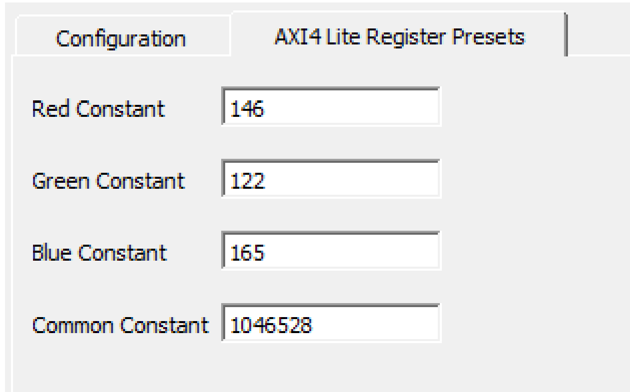


Figure 2-2. Image Enhancement IP - AXI4 Lite Register Presets Tab



2.2. Inputs and Outputs Signals (Ask a Question)

AXI4L_CLK_I and AXI4L_RESETN_I are the clock and reset signals for the AXI4-Lite configuration interface. Other AXI4-Lite signals can be seen as a bus at the input interface of the IP, as shown in Figure 1-1. The following table lists the other native signals, which are present at the input and output ports of the Image Enhancement IP, for single pixel with 8-bit color depth configuration.

Table 2-2. Input and Output Ports

Port Name	Direction	Width	Description
RESETN_I	Input	1-bit	Active-low asynchronous reset signal to design
SYS_CLK_I	Input	1-bit	System clock
DATA_VALID_I	Input	1-bit	Input data valid signal This signal is asserted high when the data is valid.
R_I	Input	8 bits	Red component of the input data frame
G_I	Input	8 bits	Green component of the input data frame
B_I	Input	8 bits	Blue component of the input data frame
FRAME_START_I	Input	1-bit	Frame Start bit is used to compute the intensity average of the incoming frame. AXI4-Lite register values are read for every frame based on this signal.
AXI4L_CLK_I	Input	1-bit	AXI4-Lite clock input
AXI4L_RESETN_I	Input	1-bit	AXI4-Lite active-low reset signal input
AXI4L_IMAGE_ENHANCEMENT	AXI4 Lite interface	—	AXI4-Lite interface to access control registers of the IP
DATA_VALID_O	Output	1-bit	Output data valid signal This signal is asserted high when the data is valid.
R_O	Output	8 bits	Red component of the processed input data frame
G_O	Output	8 bits	Green component of the processed input data frame
B_O	Output	8 bits	Blue component of the processed input data frame
Y_AVG_O	Output	32 bits	For every frame, intensity average is computed and given out on this port. This computation is done based on the frame Start signal at the input.

Table 2-3. Input and Output Ports for AXI4 Stream Video Interface

Port Name	Type	Width	Description
RESETN_I	Input	1-bit	Active-low asynchronous reset signal to design
SYS_CLK_I	Input	1-bit	System clock
TREADY_O	Output	1-bit	Output target ready

Table 2-3. Input and Output Ports for AXI4 Stream Video Interface (continued)

Port Name	Type	Width	Description
TDATA_I	Input	1 pixel: 24/30/36/48 bit 4 pixel: 96/120/144/192 bit	Input video data
TVALID_I	Input	1-bit	Input video valid
TUSER_I	Input	4 bits	Bit 0 = Frame Start Bit 1 = Unused Bit 2 = Unused Bit 3 = Unused
TDATA_O	Output	1 pixel: 24/30/36/48 bit 4 pixel: 96/120/144/192 bit	Output video data
TVALID_O	Output	1-bit	Output video valid
TUSER_O	Output	4 bits	Bit 0 = Frame Start Bit 1 = Unused Bit 2 = Unused Bit 3 = Unused
TLAST_O	Output	1-bit	Output video end of frame
TSTRB_O	Output	1 or 2 bit based on color depth	Output video data strobe
TKEEP_O	Output	1 or 2 bit based on color depth	Output video data keep

3. Timing Diagram (Ask a Question)

The following figures show the timing diagrams of Image Enhancement.

Figure 3-1. Output Computation for a Fixed Set of Inputs

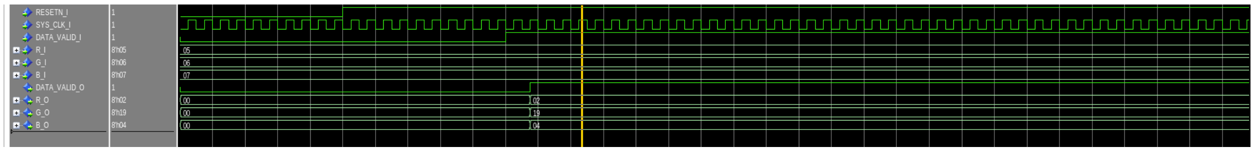
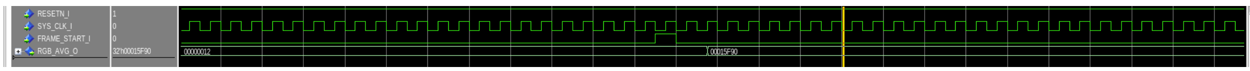


Figure 3-2. Intensity Average Computation based on the Frame Start Signal



4. Register Maps and Descriptions (Ask a Question)

This section discusses about register maps and descriptions.

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x00	IP_VER	7:0	IP VERSION[7:0]							
		15:8	IP VERSION[15:8]							
		23:16	IP VERSION[23:16]							
		31:24								
0x04	Control_Register	7:0							IP RESET	ENABLE/ DISABLE
		15:8								
		23:16								
		31:24								
0x08	R_Constant	7:0	R_CONSTANT[7:0]							
		15:8							R_CONSTANT[9:8]	
		23:16								
		31:24								
0x0C	G_Constant	7:0	G_CONSTANT[7:0]							
		15:8							G_CONSTANT[9:8]	
		23:16								
		31:24								
0x10	B_Constant	7:0	B_CONSTANT[7:0]							
		15:8							B_CONSTANT[9:8]	
		23:16								
		31:24								
0x14	Common_Constant	7:0	COMMON_CONSTANT[7:0]							
		15:8	COMMON_CONSTANT[15:8]							
		23:16					COMMON_CONSTANT[19:16]			
		31:24								
0x18	Intensity_Average	7:0	INTENSITY_AVERAGE[7:0]							
		15:8	INTENSITY_AVERAGE[15:8]							
		23:16	INTENSITY_AVERAGE[23:16]							
		31:24	INTENSITY_AVERAGE[31:24]							

4.1. IP_VER (Ask a Question)

Name: IP_VER
Offset: 0x000
Reset: 0x40600
Property: Read-only

Image Enhancement IP version number. The lower 8 bits of the IP version may not match the version mentioned in the document, if the IP has an updated version due to minor updates or bug fixes.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
	IP VERSION[23:16]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	1	0	0

Bit	15	14	13	12	11	10	9	8
	IP VERSION[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	1	1	0

Bit	7	6	5	4	3	2	1	0
	IP VERSION[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 23:0 – IP VERSION[23:0] Current Image Enhancement IP version number

4.2. Control_Register (Ask a Question)

Name: Control_Register
Offset: 0x004
Reset: 0x1
Property: Read-Write

Register to Enable/Disable/Reset the Image Enhancement IP

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
							IP RESET	ENABLE/ DISABLE
Access							W	R/W
Reset							0	1

Bit 1 – IP RESET To reset, the IP core value of '1' needs to be written to this bit once. It does not hold the written value.

Bit 0 – ENABLE/DISABLE This bit controls Enabling or Disabling the IP.
The following table lists the IP control register value with its functionality.

IP Control Register Value	Functionality
0	Disable
1	Enable

4.3. R_Constant (Ask a Question)

Name: R_Constant
Offset: 0x008
Reset: 0x92
Property: Write-only

Input constant to multiply with RED data component

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
							R_CONSTANT[9:8]	
Access							W	W
Reset							0	0

Bit	7	6	5	4	3	2	1	0
	R_CONSTANT[7:0]							
Access	W	W	W	W	W	W	W	W
Reset	1	0	0	1	0	0	1	0

Bits 9:0 – R_CONSTANT[9:0] Input constant to multiply with RED data component

4.4. G_Constant (Ask a Question)

Name: G_Constant
Offset: 0x00C
Reset: 0x7a
Property: Write-only

Input constant to multiply with GREEN data component

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
							G_CONSTANT[9:8]	
Access							W	W
Reset							0	0

Bit	7	6	5	4	3	2	1	0
	G_CONSTANT[7:0]							
Access	W	W	W	W	W	W	W	W
Reset	0	1	1	1	1	0	1	0

Bits 9:0 – G_CONSTANT[9:0] Input constant to multiply with GREEN data component

4.5. B_Constant (Ask a Question)

Name: B_Constant
Offset: 0x010
Reset: 0xa5
Property: Write-only

Input constant to multiply with BLUE data component

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
							B_CONSTANT[9:8]	
Access							W	W
Reset							0	0

Bit	7	6	5	4	3	2	1	0
	B_CONSTANT[7:0]							
Access	W	W	W	W	W	W	W	W
Reset	1	0	1	0	0	1	0	1

Bits 9:0 – B_CONSTANT[9:0] Input constant to multiply with BLUE data component

4.6. Common_Constant (Ask a Question)

Name: Common_Constant
Offset: 0x014
Reset: 0xff800
Property: Write-only

Input constant with brightness and contrast

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
					COMMON_CONSTANT[19:16]			
Access					W	W	W	W
Reset					1	1	1	1

Bit	15	14	13	12	11	10	9	8
	COMMON_CONSTANT[15:8]							
Access	W	W	W	W	W	W	W	W
Reset	1	1	1	1	1	0	0	0

Bit	7	6	5	4	3	2	1	0
	COMMON_CONSTANT[7:0]							
Access	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	0

Bits 19:0 – COMMON_CONSTANT[19:0] Input constant with brightness and contrast

4.7. Intensity_Average (Ask a Question)

Name: Intensity_Average
Offset: 0x018
Reset: 0x0
Property: Read-only

Intensity average value of the input frame to the Image Enhancement IP

Bit	31	30	29	28	27	26	25	24
	INTENSITY_AVERAGE[31:24]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	INTENSITY_AVERAGE[23:16]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	INTENSITY_AVERAGE[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	INTENSITY_AVERAGE[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – INTENSITY_AVERAGE[31:0] Intensity average value of the input frame to the Image Enhancement IP

5. Testbench (Ask a Question)

The testbench provides the means to check the functionality of Image Enhancement IP when IP is instantiated. This testbench works only for single channel color depth of 8 bits in 1 pixel mode of operation.

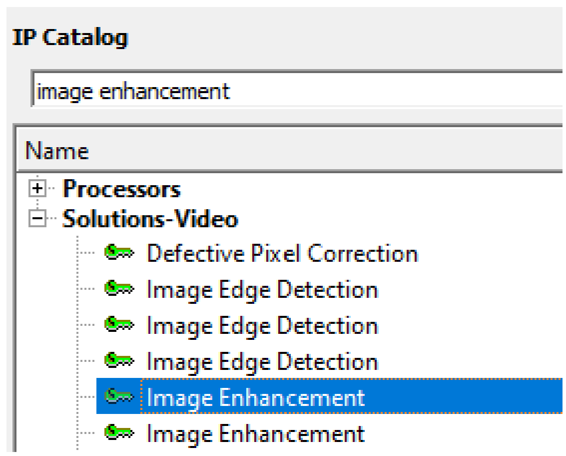
5.1. Simulation (Ask a Question)

To stimulate the core using the testbench, perform the following steps:

1. Go to Libero SoC **Catalog** tab, expand **Solutions-Video**, double-click **Image Enhancement**, and then click **OK**. The documentation associated with the IP are listed under **Documentation**.

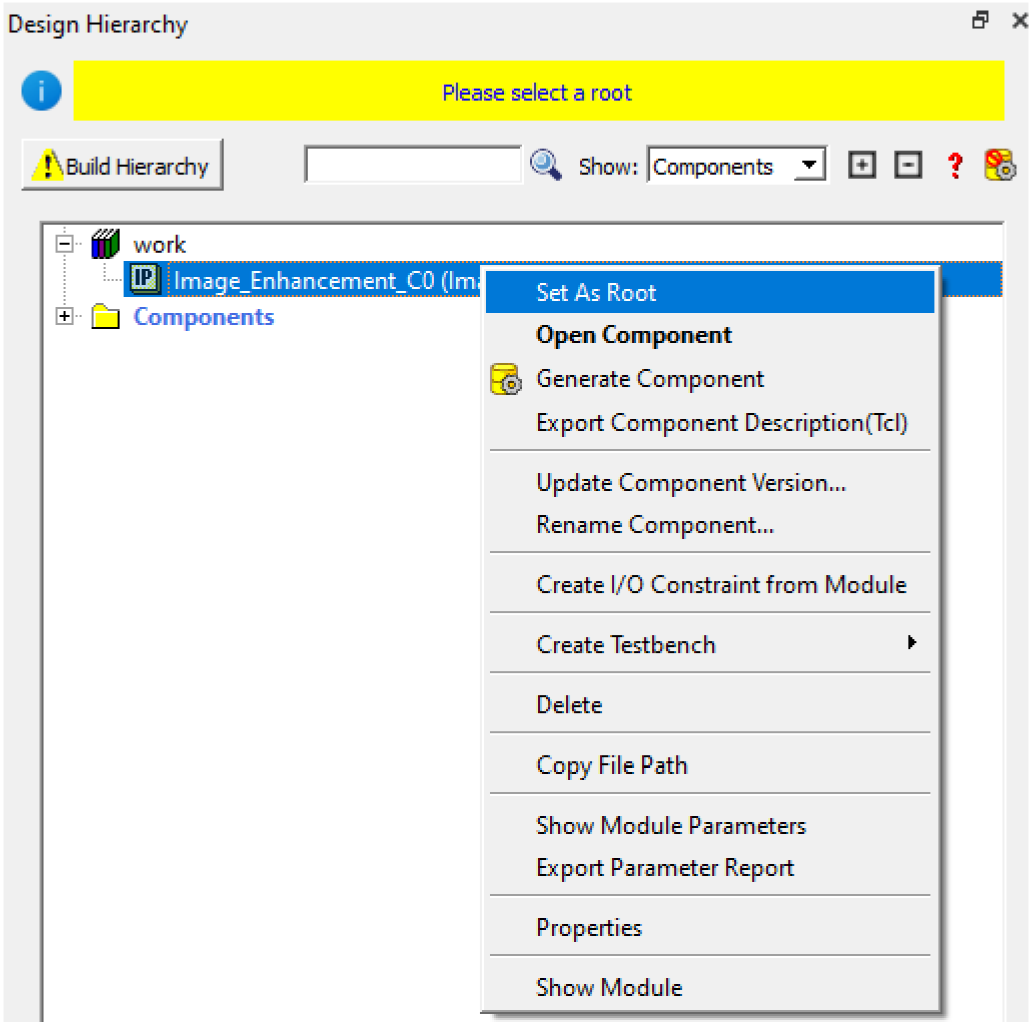
> **Important:** If you do not see the **Catalog** tab, navigate to **View** > **Windows** menu, and click **Catalog** to make it visible.

Figure 5-1. Image Enhancement Core in Libero SoC Catalog



2. In the **Design Hierarchy** tab, select the IP and click **Set As Root** as shown in the figure below.

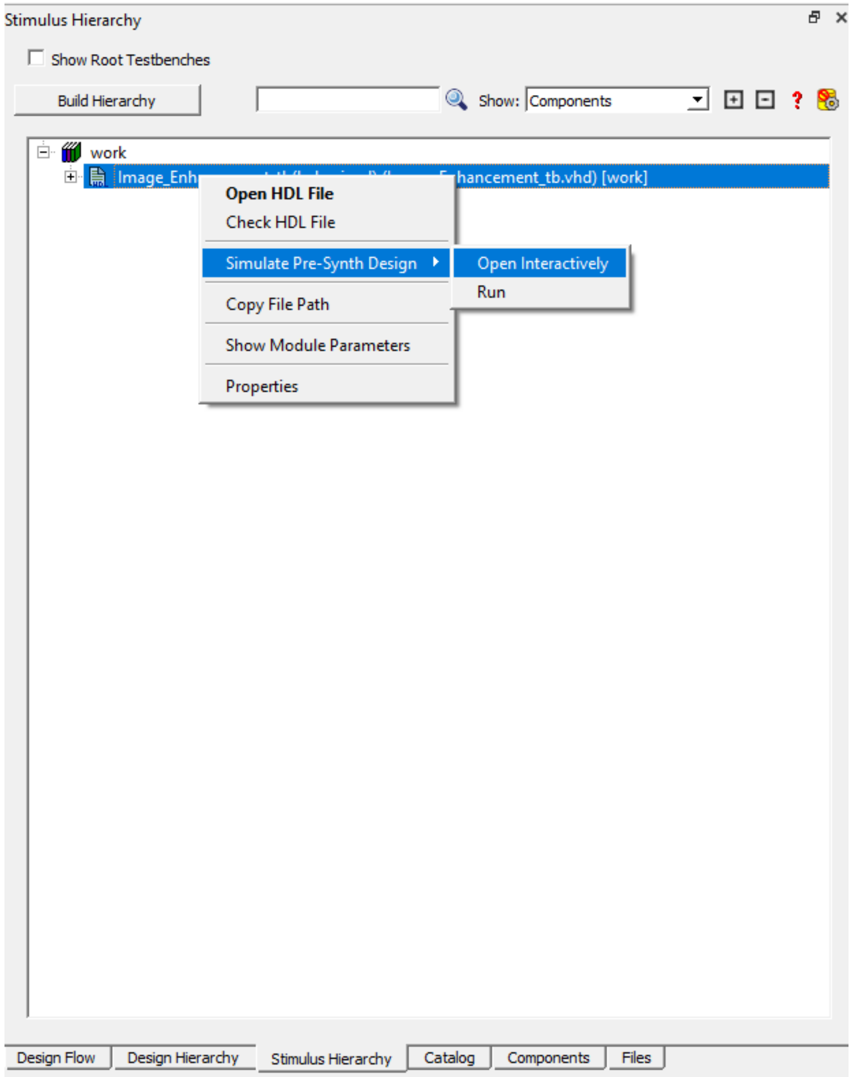
Figure 5-2. Design Hierarchy Tab - Set As Root



3. On the **Stimulus Hierarchy** tab, select the testbench (`Image_Enhancement_tb.v`), right-click, and then click **Simulate Pre-Synth Design** > **Open Interactively**.

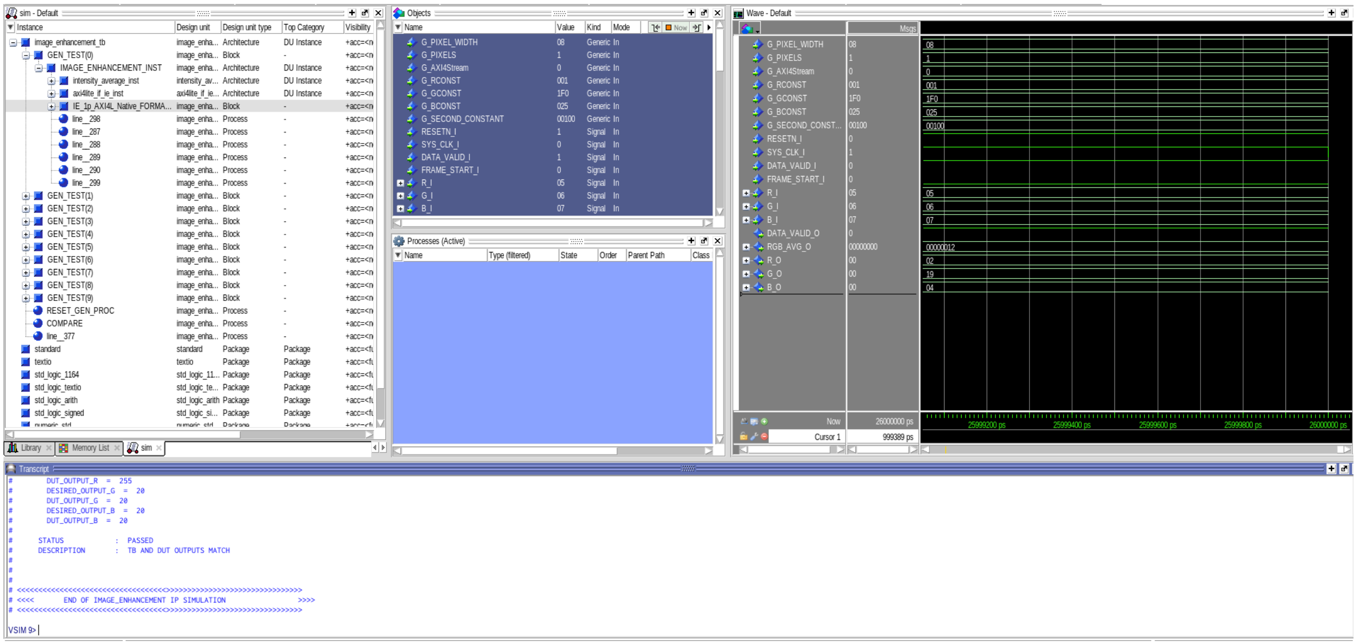
> **Important:** If you do not see the **Stimulus Hierarchy** tab, navigate to **View** > **Windows** menu, and then click **Stimulus Hierarchy** to make it visible.

Figure 5-3. Simulating Pre-Synthesis Design



Simulator opens with the testbench file, as shown in the following figure.

Figure 5-4. Simulation Window



Important: If the simulation is interrupted due to the runtime limit specified in the `.do` file, use the `run -all` command to complete the simulation.

6. Device Utilization (Ask a Question)

Resource utilization for Image Enhancement IP for PolarFire SoC FPGA (MPFS250TS-1FCG1152I), with the following configurations, is listed in the following table:

Table 6-1. Configuration Options

Configuration Parameter	Value
Number of pixels	1
Configuration Interface	AXI4-Lite
Video Interface	Native
Color Depth	8

Table 6-2. Resource Utilization

Resource	Usage
Fabric 4LUT	337
Fabric DFF	368
Interface 4LUT	108
Interface DFF	108
Math (18 x 18)	3
Chip Globals	2

7. Revision History (Ask a Question)

The revision history table describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

Revision	Date	Description
B	02/2025	The following is the list of changes in revision B of the document: • Updated Figure 1-1 in the Functional Description section. • Updated Table 2-1 in the Configuration Settings section. • Updated Table 2-2 and Table 2-3 in the Inputs and Outputs Signals section. • Updated the Register Maps and Descriptions section. • Updated Figure 5-1 in the Simulation section. • Added Table 6-1 and updated Table 6-2 in the Device Utilization section.
A	02/2024	The following is the list of changes in revision A of the document: • The document was migrated to the Microchip template. • The document number was updated to DS50003650A from 50200646.
6.0	—	The following is the list of changes in revision 6.0 of the document: • Updated Figure 1-1 • Added new Testbench section
5.0	—	The following is the list of changes in revision 5.0 of the document: • Updated Figure 1-1 • Updated Table 2-2
4.0	—	The following is the list of changes in revision 4.0 of the document: • Added Key Features and Supported Families • Updated Table 2-1 • Added License, Encrypted, and RTL sections.
3.0	—	The resource utilization reports were updated..
2.0	—	The following is the list of changes in revision 2.0 of the document: • Updated Figure 1-1 • Updated Table 2-2
1.0	—	Initial release

Microchip FPGA Support

Microchip FPGA products group backs its products with various support services, including Customer Service, Customer Technical Support Center, a website, and worldwide sales offices. Customers are suggested to visit Microchip online resources prior to contacting support as it is very likely that their queries have been already answered.

Contact Technical Support Center through the website at www.microchip.com/support. Mention the FPGA Device Part number, select appropriate case category, and upload design files while creating a technical support case.

Contact Customer Service for non-technical product support, such as product pricing, product upgrades, update information, order status, and authorization.

- From North America, call **800.262.1060**
- From the rest of the world, call **650.318.4460**
- Fax, from anywhere in the world, **650.318.8044**

Microchip Information

Trademarks

The “Microchip” name and logo, the “M” logo, and other names, logos, and brands are registered and unregistered trademarks of Microchip Technology Incorporated or its affiliates and/or subsidiaries in the United States and/or other countries (“Microchip Trademarks”). Information regarding Microchip Trademarks can be found at https://www.microchip.com/en-us/about/legal-information/microchip-trademarks.

ISBN: 979-8-3371-0655-7

Legal Notice

Microchip Devices Code Protection Feature

Note the following details of the code protection feature on Microchip products:

- Microchip products meet the specifications contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is secure when used in the intended manner, within operating specifications, and under normal conditions.
- Microchip values and aggressively protects its intellectual property rights. Attempts to breach the code protection features of Microchip products are strictly prohibited and may violate the Digital Millennium Copyright Act.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of its code. Code protection does not mean that we are guaranteeing the product is “unbreakable”. Code protection is constantly evolving. Microchip is committed to continuously improving the code protection features of our products.