

Introduction [\(Ask a Question\)](#)

This guide provides pin and packaging information (such as, bank assignments and mechanical information) for Radiation-Tolerant (RT) PolarFire[®] System-on-Chip (SoC) Field Programmable Gate Arrays (FPGAs).

RT PolarFire SoC FPGAs feature a flexible I/O structure that supports a range of mixed voltages through bank selection. The High Speed Input/Output (HSIO), General-Purpose Input/Output (GPIO) and MSSIO are configured as differential I/Os or two single-ended I/Os. For more information about HSIO, GPIO, MSSIO and supported I/O standards, see [PolarFire Family I/O User Guide](#).



Important: Some of the protocol standard uses the terminology Master and Slave. The equivalent Microchip terminology used in this document is Initiator and Target, respectively.

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1. Packaging Overview [\(Ask a Question\)](#)

RT PolarFire® SoC FPGAs are available in different variations of a hermetically sealed ceramic and plastic ball grid array packages utilizing flip chip interconnect.

The following table lists the RT PolarFire SoC FPGA variant, with user I/O and XCVR lanes.

Table 1-1. RT PolarFire® SoC FPGA Product Family

Components	Features	RTPFS160ZT	RTPFS460ZT
FPGA Fabric	K Logic Elements (4 LUT + DFF)	161	461
	Math Blocks (18 × 18 MACC)	498	1420
	LSRAM Blocks (20 Kb)	520	1460
	μSRAM Blocks (64 × 12)	1494	4260
	Total RAM (Mb)	11.3	31.6
	μPROM (Kb)	415	553
	User DLLs/PLLs	8	8
Microprocessor Subsystem (MSS)	Boot/Monitor Core	1 × E51 core: RISC-V® RV64IMAC, 625 MHz	
	Application Cores	4 × U54 cores; RISC-V RV64GC, 625 MHz	
	L2 Cache	2 MB; configurable as cache, Loosely Integrated Memory (LIM) or Scratchpad	
	Data Security	DPA-resistant Athena TeraFire® crypto coprocessor available in devices with the suffix "S"	
	Ethernet	Yes; 2 × Gigabit Ethernet MAC	
	MAC	Yes; MMC 5.1	
	CAN	Yes; 2 × CAN	
	QSPI	Yes; 1 × QSPI	
	SPI	Yes; 2 × SPI	
	I ² C	Yes; 2 × I ² C	
	UART	Yes; 5 × UART	
High-Speed I/O	250 Mbps to 12.7 Gbps SerDes Lanes	8	20
	PCIe® Gen2 End Points/ Root Ports	2	2
Total FPGA I/O	HSIO + GPIO	312	516
Total MSS I/O	MSS I/O	136	136
MSS DDR DB	MSS DDR Data Bus	32	32
Packaging	Type/Size/Pitch	Total User I/O: MSS-IO/HSIO/GPIO/XCVRs	
	FCV(G)784 (23 × 23, 0.8 mm)	136, 144, 168, 8	—
	FC(G)1509 (40 × 40, 1.0 mm)	—	136, 180, 336, 20
	CG1509 (40 × 40, 1.0 mm)	—	136, 180, 336, 20

The following table lists the packages and its application types.

Table 1-2. Package Product Family Table

Package	Description	Size	Pitch	RTPFS160ZT	RTPFS460ZT	Application
FCV784	Plastic Flip Chip Ball Grid Array Package with Eutectic Tin-Lead Solder Balls	23 mm x 23 mm	0.8 mm	✓	—	Flight Prototyping

Table 1-2. Package Product Family Table (continued)

Package	Description	Size	Pitch	RTPFS160ZT	RTPFS460ZT	Application
FCVG784	Plastic Flip Chip Ball Grid Array Package with Lead-Free Solder Balls	23 mm x 23 mm	0.8 mm	✓	—	Flight Prototyping
CG1509	Hermetically Sealed Ceramic Column Grid Array Package	40 mm× 40 mm	1.0 mm	—	✓	Flight Prototyping
LG1509	Hermetically Sealed Ceramic Land Grid Array Package	40 mm× 40 mm	1.0 mm	—	✓	Flight Prototyping
CB1509	Hermetically Sealed Ceramic Ball Grid Array Package	40 mm× 40 mm	1.0 mm	—	✓	Prototyping
FC1509	Plastic Flip Chip Ball Grid Array Package with Eutectic Tin-Lead Solder Balls	40 mm× 40 mm	1.0 mm	—	✓	Flight
FCG1509	Plastic Flip Chip Ball Grid Array Package with Lead-Free Solder Balls	40 mm× 40 mm	1.0 mm	—	✓	Flight

Note: For more information on the package design, see cross-section drawings for the CG, LG, CB and FC packages in the [Mechanical Drawings](#) section.

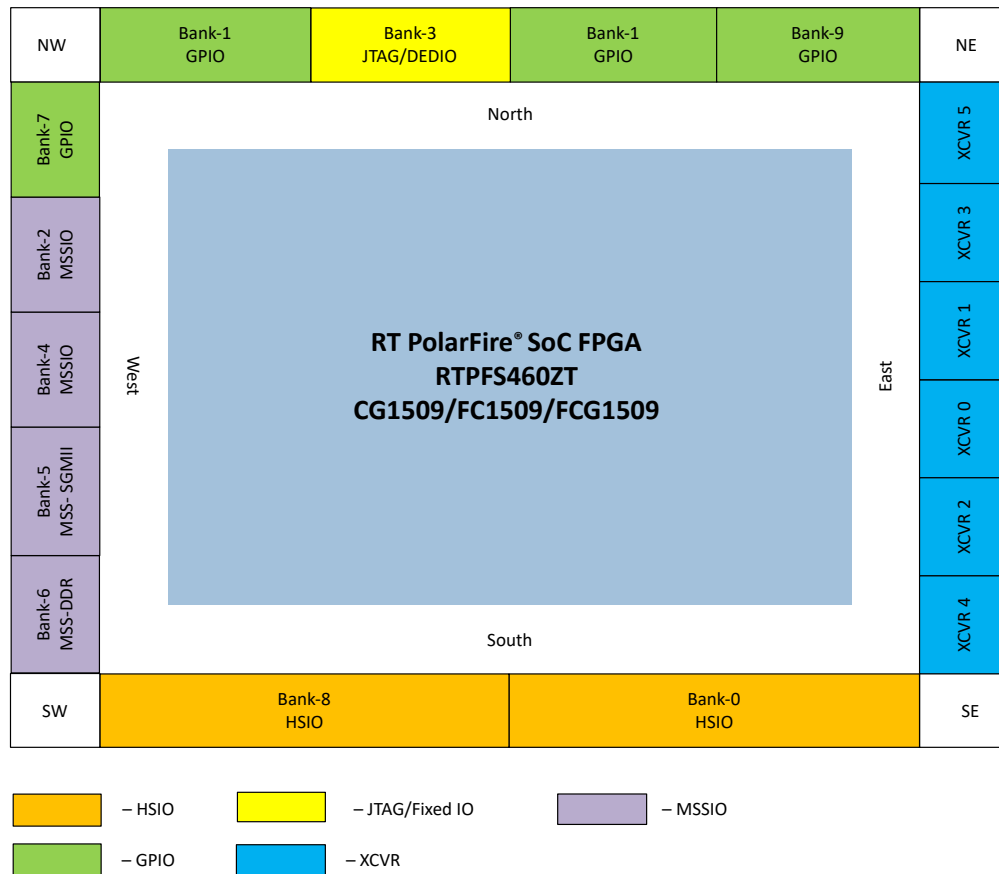
2. Bank Locations [\(Ask a Question\)](#)

RT PolarFire® SoC FPGA I/Os are grouped based on I/O voltage standards and I/O capabilities. Each I/O bank has dedicated I/O supplies and ground voltages. Because of these dedicated supplies, only I/O with compatible standards are assigned to the same I/O voltage bank.

The following illustrations show the bank locations for the RTPFS160ZT and RTPFS460ZT devices with available package combinations.

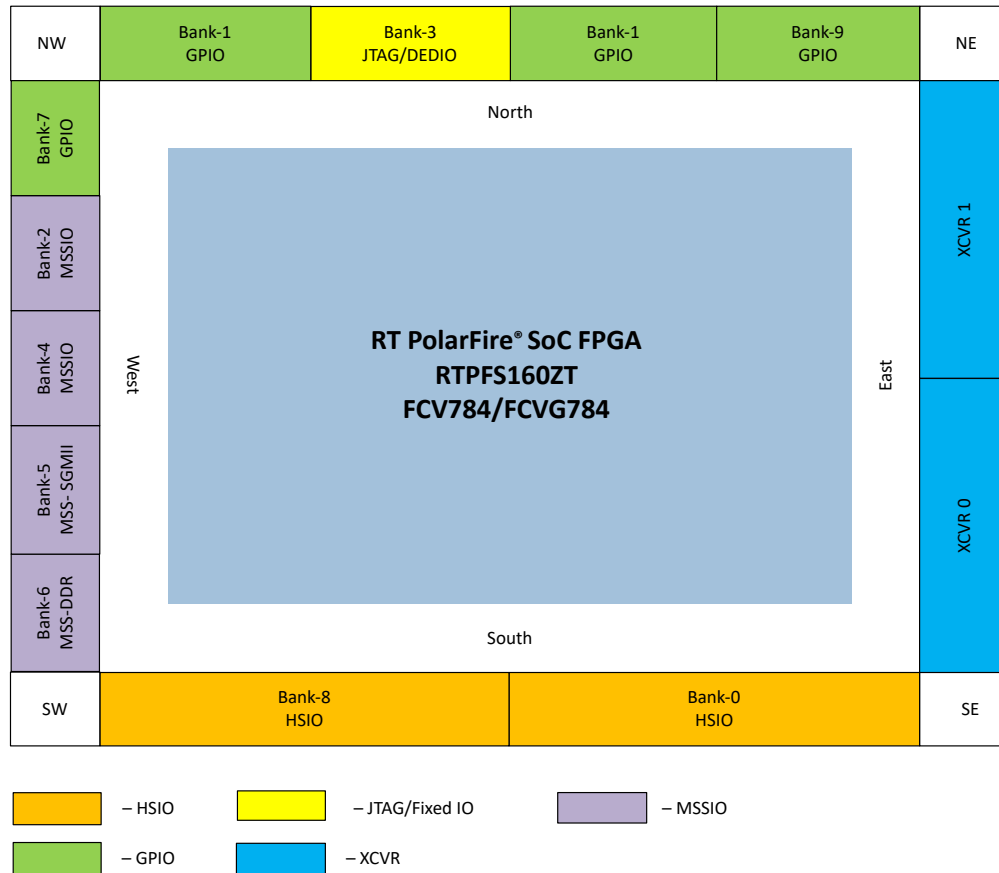
➔ Important: This figure shows the top-view of the package. See the package orientation accordingly when interpreting pin positions or dimensions.

Figure 2-1. RTPFS460ZT-CG1509/FC1509/FCG1509 I/O Bank Locations



➔ Important: This figure shows the top-view of the package. See the package orientation accordingly when interpreting pin positions or dimensions.

Figure 2-2. RTPFS160ZT-FCV784/FCVG784 I/O Bank Locations



➔ Important: RTPFS160ZT in FCV784/FCVG784 is pin compatible with commercial part MPFS160T in FCVG784.

The following table lists the organization of the I/O banks in RT PolarFire SoC FPGAs. Each XCVR supports four lanes in every package. In all the packages, PCIe® is supported only in XCVR0.

Table 2-1. Organization of I/O Banks

Bank Number	FCV784/FCVG784	CG1509/FC1509/FCG1509
	RTPFS160ZT	RTPFS460ZT
Bank 0	HSIO	HSIO
Bank 1	GPIO	GPIO
Bank 2	MSSIO	MSSIO
Bank 3	JTAG/DEDIO	JTAG/DEDIO
Bank 4	MSSIO	MSSIO
Bank 5 (MSS SGMII BANK)	MSSIO	MSSIO
Bank 6 (MSS DDR BANK)	MSSIO	MSSIO
Bank 7	GPIO	GPIO

Table 2-1. Organization of I/O Banks (continued)

Bank Number	FCV784/FCVG784	CG1509/FC1509/FCG1509
	RTPFS160ZT	RTPFS460ZT
Bank 8	HSIO	HSIO
Bank 9	GPIO	GPIO
XCVR 0	Included	Included
XCVR 1	Included	Included
XCVR 2	—	Included
XCVR 3	—	Included
XCVR 4	—	Included
XCVR 5	—	Included

Each I/O bank supports multiple DDR lanes. If CDR/SGMII interface is connected to the I/O bank, the Tx and Rx signal must be within the same DDR Lane. Only one CDR/SGMII is allowed per DDR lane. For more information about the DDR lanes for each package, see [Package Pin Assignment Table \(PPAT\)](#) and Product Family Product Overview.

3. Package Pin Assignment [\(Ask a Question\)](#)

The Package Pin Assignment Table (PPAT) information is available in the Packaging section for [RTPFS460 PPAT](#) and [RTPFS160 PPAT](#). PPAT contains information about recommended DDR pin-outs, PCI Express capability for XCVR-0, DDR Lane information for I/O CDR and generic IOD interface pin placement.

4. Pin Descriptions [\(Ask a Question\)](#)

RT PolarFire® SoC device has user I/O (GPIO/HSIO) pins, dedicated I/O bank pins, memory interface, XCVR interface, clocking pins and supply pins.

4.1. User I/O [\(Ask a Question\)](#)

RT PolarFire® SoC FPGA I/Os are paired up to meet the differential I/O standards and grouped into lanes of 12 buffers with a lane controller for memory interfaces. For more information about the memory controller, see [PolarFire Family Memory Controller User Guide](#).

Two types of I/O buffers are available—HSIO and GPIO. HSIO is optimized for 1.2 Gbps (DDR4) operation with operating supplies between 1.1V and 1.8V. GPIO buffers support a wider range of I/O interfaces with speeds of up to 1066 Mbps when using single-ended standards and 1.25 Gbps when using differential standards. GPIO supports multiple standards with an integrated Clock Data Recovery (CDR) to high-speed serial interfaces such as 1 GbE.

Each RT PolarFire SoC FPGA user I/O uses an IOxyBz naming convention, where:

- IO = Type of I/O
- x = I/O pair number in bank z
- y = P (positive) or N (negative). In Single-ended mode, the I/O pair operates as two separate I/O—P and N. Differential mode is implemented with a fixed I/O pair and cannot be split with an adjacent I/O.
- B = Bank (For more information, see note in [Supported I/O Features](#))
- z = Bank number

GPIOxyBz and HSIOxyBz are bidirectional user I/O pins that are capable of differential signaling.

4.1.1. Supported I/O Features [\(Ask a Question\)](#)

The following table lists the I/O features supported on HSIO and GPIO.

Table 4-1. Supported I/O Features

I/O Feature	HSIO	GPIO	Additional Information
Programmable ON/OFF clamp	—	Yes	—
Hot-plug	—	Yes	—
Cold sparing	Yes	Yes	—
True differential output driver	—	Yes	—
Programmable ON/OFF 100Ω differential termination	—	Yes	—
PVT-compensated output drive	Yes	Yes	—
Programmable slew control	—	Yes	—
PVT compensated slew control	Yes	—	—
Programmable input hysteresis	Yes	Yes	—
Mobile Industry Processor Interface (MIPI) (input)	—	Yes	High-speed and low-power
MIPI (output)	—	Yes	High-speed

Note: HSIO is pseudo-cold spare, that is, it requires the spare device to have its HSIO VDDI banks powered up to prevent I/O leakage through the ESD diodes.

4.2. Supply Pins [\(Ask a Question\)](#)

The following table lists multiple power supply pins required for proper device operation. For more information about unused conditions and power sequence, see [RT PolarFire SoC FPGA Board Design User Guide](#).

Table 4-2. Supply Pins

Name	Description	Operating Voltage
XCVR_VREF	Voltage reference for transceiver	0.9V/1.25V
VDD_XCVR_CLK	Provides common power to all transceiver reference clock buffers	2.5V/3.3V
VDDA25	Transceiver PLL power	2.5V
VDDA	Power for transceiver Tx and Rx lanes 0, 1, 2 and 3	1.05V
VSS	Core digital ground	—
VDD	Device core digital supply	1.0V/1.05V
VDDI5	VDDI5 power for MSS SGMII banks and MSS dedicated clocks	—
VDDI2	VDDI2 power for MSS peripheral banks	—
VDDI4	Power for MSS peripheral banks	—
VDDI6	Power for MSS DDR banks	—
VDDIx	Supply for JTAG, SPI and DEVRST_N pins	1.8V/2.5V/3.3V
VDDIx (GPIO Banks)	Supply for I/O circuits in a bank	1.2V/1.5V/1.8V/2.5V/3.3V
VDDIx (HSIO Banks)	Supply for I/O circuits in a bank	1.2V/1.3V/1.5V/1.8V
VDD25	Power for corner PLLs and PNVM	2.5V
VDD18	Power for programming and HSIO receiver. HSIO auxiliary power supply	1.8V
VDDAUXx	Auxiliary supply for I/O circuits. Auxiliary supply voltage must be set to 2.5V or 3.3V and must be always equal to or higher than VDDIx of GPIO banks VDDAUX = 2.5V for bank voltages 1.2V/1.5V/1.8V and 2.5V VDDAUX = 3.3V for bank voltage 3.3V	Greater than or equal to VDDI

**Important:**

- SSTL25 (stub series terminated logic) I/O standard for 1.25V V_{REF} , SSTL18 I/O standard for 0.9V and HSUL18 I/O standard for 0.9V.
- Designers must be familiar with the latest Single Event Latch-Up radiation test data before choosing GPIO supply voltages.

4.2.1. Packaging Decoupling Capacitors ([Ask a Question](#))

The following table lists the packaging decoupling capacitors contained in the RTPF460T/ZT-CG1509 package. These are decoupling capacitors inside the package for different power lines. For board level decoupling capacitor requirements, see [RT PolarFire SoC Board Design User Guide](#).

Table 4-3. Packaging Decoupling Capacitors—RTPFS460T-CG1509 (1 mm)

Pin	Multi-Layer Ceramic Capacitor (MLCC)									Tantalum
	1 nF	4.7 nF	10 nF	47 nF	0.1 μ F	4.7 μ F	10 μ F	47 μ F	100 μ F	330 μ F
VDD	—	—	10	4	—	7	—	—	1	3
VDDA	2	2	2	—	—	3	—	—	1	—
VDD18	—	—	—	—	—	2	—	—	2	—
VDD25	—	—	—	—	—	3	—	—	1	—
VDDA25	—	—	1	—	—	4	—	—	1	—
VDDI2 (MSSIO)	1	—	—	—	—	—	1	—	1	—
VDDI3 (JTAG)	—	—	—	—	—	—	3	—	—	—
VDDI4 (MSSIO)	1	—	—	—	—	—	1	—	1	—
VDDI5 (MSS SGMII)	1	—	—	—	—	—	1	—	1	—
VDDI6 (MSS DDR)	1	—	—	—	—	—	2	—	1	—
VDDAUX1	—	—	1	—	—	—	2	—	1	—

Table 4-3. Packaging Decoupling Capacitors—RTPFS460T-CG1509 (1 mm) (continued)

Pin	Multi-Layer Ceramic Capacitor (MLCC)										Tantalum
	1 nF	4.7 nF	10 nF	47 nF	0.1 μ F	4.7 μ F	10 μ F	47 μ F	100 μ F	330 μ F	
VDDAUX2	—	—	1	—	—	—	2	—	1	—	
VDDAUX4	—	—	1	—	—	—	2	—	1	—	
VDDAUX7	—	—	1	—	—	—	2	—	1	—	
VDDAUX9	—	—	1	—	—	—	2	—	1	—	
VDDI1 (GPIO Bank)	1	—	—	—	—	—	1	—	1	—	
VDDI7 (GPIO Bank)	1	—	—	—	—	—	1	—	1	—	
VDDI9 (GPIO Bank)	1	—	—	—	—	—	1	—	1	—	
VDDI0 (HSIO Bank)	1	1	—	—	—	1	—	—	1	—	
VDDI8 (HSIO Bank)	1	1	—	—	—	1	—	—	1	—	
VDD_XCVR_CLK	—	—	—	—	—	—	3	—	—	—	
XCVR_VREF	—	—	—	—	—	—	1	—	—	—	

The following table lists the packaging decoupling capacitors contained in the RTPFS160T-FCV784 packages.

Table 4-4. Packaging Decoupling Capacitors— RTPF160T-FCV784 (1 mm)

Pin	Multi-Layer Ceramic Capacitor (MLCC)										Tantalum
	1 nF	4.7 nF	10 nF	47 nF	0.1 μ F	4.7 μ F	10 μ F	47 μ F	100 μ F	330 μ F	
VDD	—	—	10	4	—	7	—	—	1	3	
VDD18	—	—	—	—	—	2	—	—	2	—	
VDD25	—	—	—	—	—	3	—	—	1	—	
VDDA	2	2	2	—	—	3	—	—	1	—	
VDDA25	2	—	1	—	—	2	—	—	1	—	
VDDI2 (MSSIO)	2	—	—	—	—	—	—	—	1	—	
VDDI3 (JTAG)	—	—	—	—	—	—	3	—	—	—	
VDDI4 (MSSIO)	2	—	—	—	—	—	—	—	1	—	
VDDI5 (MSS SGMII)	2	—	—	—	—	—	—	—	1	—	
VDDI6 (MSS DDR)	1	—	—	—	—	—	2	—	1	—	
VDDAUX1	—	—	1	—	—	—	2	—	1	—	
VDDAUX2	—	—	1	—	—	—	2	—	1	—	
VDDAUX4	—	—	1	—	—	—	2	—	1	—	
VDDAUX7	—	—	1	—	—	—	2	—	1	—	
VDDAUX9	—	—	1	—	—	—	2	—	1	—	
VDDI1 (GPIO Bank)	1	—	—	—	—	—	1	—	1	—	
VDDI7 (GPIO Bank)	1	—	—	—	—	—	1	—	1	—	
VDDI9 (GPIO Bank)	1	—	—	—	—	—	1	—	1	—	

Table 4-4. Packaging Decoupling Capacitors— RTPF160T-FCV784 (1 mm) (continued)

Pin	Multi-Layer Ceramic Capacitor (MLCC)									Tantalum
	1 nF	4.7 nF	10 nF	47 nF	0.1 μ F	4.7 μ F	10 μ F	47 μ F	100 μ F	330 μ F
VDDI0 (HSIO Bank)	1	1	—	—	—	1	—	—	1	—
VDDI8 (HSIO Bank)	1	1	—	—	—	1	—	—	1	—
VDD_XCV R_CLK	—	—	—	—	—	—	3	—	—	—
XCVR_VRE F	—	—	—	—	—	—	1	—	—	—

4.3. Memory Interface [\(Ask a Question\)](#)

Valid locations for DDR memory interfaces are shown in PPAT, see [RT PolarFire SoC Packaging Pin Assignment Table](#) webpage. By using the Libero[®] SoC configurator, all individual DDR interface pins are identified from the macro. For more information about the memory interface, see [PolarFire Family Memory Controller User Guide](#).

The following table lists the reference receiver modes of I/O standards.

Table 4-5. Reference Receiver Modes

I/O Standard	VDDIx	VREF	On-Die Termination (ODT) (in Ω)	Bank Type	Application
SSTL18	1.8V	0.9V	40/50/60/80/120/240	GPIO, HSIO	RLDRAM2
SSTL15	1.5V	0.75V	40/50/60/80/120/240	GPIO, HSIO	DDR3
SSTL135	1.35V	0.68V	20/30/40/60/120	HSIO	DDR3L
HSTL15	1.5V	0.75V	40/50/60/80/120/240	GPIO, HSIO	QDRII+
HSTL135	1.35V	0.68V	20/30/40/60/120	HSIO	RLDRAM3
HSUL12	1.2V	0.6V	60/120/40	HSIO	LPDDR3
HSTL12	1.2V	0.6V	60/120/240	HSIO	QDRII+
POD12	1.2V	0.6V	20/30/40/60/120	HSIO	DDR4

4.4. DDR Interface [\(Ask a Question\)](#)

Then DDR subsystems are hardened ASIC blocks for interfacing the LPDDR3, DDR3 and DDR4 memories. It supports 16-bit, 32-bit and 64-bit data bus width modes with ECC support. The DDRIO uses fixed impedance calibration for different drive strengths. These values are programmed using Libero[®] SoC software for the selected I/O standard. The values are fed to the pull-up or pull-down reference network to match the impedance with an external resistor. For more information about DDR signals, see [PolarFire Family Memory Controller User Guide](#).

4.5. Clocking Pins [\(Ask a Question\)](#)

Clock Conditioning Circuit (CCC) blocks, located at each corner of the RT PolarFire[®] SoC FPGAs, contain two PLLs and two DLLs that provide flexible on-chip and off-chip clock management and synthesis capabilities. CCCs are labeled according to their locations in the core. For example, the CCC located in the northeast corner is labeled as CCC_NE. For more information about clocking pins, see [PolarFire Family Clocking Resources User Guide](#). Preferred clock inputs (CLKIN) are located on three sides of the device, with eight preferred clock inputs on the west side, twelve on the north side, and either 12 or 16 inputs on the south side, depending on the package.

The following table lists the clocking pin names and descriptions. For more information about CCC pin voltage, see [Table 4-2](#).

Table 4-6. Clocking Pins

Name	Description	When Unused
CCC_NW_PLL0_OUT[0:1]	Dedicated PLL output clock pins used to drive high-performance clocks in DDR3 and DDR4 applications located in the corners of RT PolarFire® SoC device to route the clocks to and from the PLLs and DLLs.	Do not connect (DNC)
CCC_NW_PLL1_OUT[0:1]		
CCC_NE_PLL0_OUT[0:1]		
CCC_NE_PLL1_OUT[0:1]		
CCC_SE_PLL0_OUT[0:1]		
CCC_SE_PLL1_OUT[0:1]		
CCC_SW_PLL0_OUT[0:1]		
CCC_SW_PLL1_OUT[0:1]		
CCC_SE_CLKIN_S_[8:15]	Preferred clock inputs that connect external clock signals to the CCCs and the global clock network through low-latency paths. It is recommended to use these preferred clock inputs for connecting external clocks to the clock inputs of PLLs, DLLs and fabric logic.	DNC
CCC_SW_CLKIN_S_[0:3]		
CCC_SW_CLKIN_W_[0:3]		
CCC_NW_CLKIN_W_[4:7]		
CCC_NW_CLKIN_N_[0:3]		
CCC_NE_CLKIN_N_[8:11]		
CLKIN_S_[4:7]	Preferred clock inputs directly routed to internal global buffers through MUXes.	DNC
CLKIN_N_[4:7]		

Note: Some of the preferred clock inputs have connections to feedback clock input of the PLL/DLL present in the CCC. It is required to choose a preferred clock input which has connection to the PLL reference clock input for clock frequency synthesis. For preferred clock inputs connectivity to PLLs/DLLs and global clock network, see [PolarFire Family Clocking Resources User Guide](#).

4.6. Dedicated I/O Bank Pins [\(Ask a Question\)](#)

JTAG, SPI and DEVRST_N signals share the same bank 3 supply and are not directly available to the fabric. SPI I/O are, however, dynamically switched over to be used by the fabric whenever the RT PolarFire® SoC controller is not using them. Dedicated I/O bank supplies must be powered up above their operational threshold and enabled before the RT PolarFire SoC controller negates the main power-on reset to the FPGA fabric. The following tables list the JTAG, SPI and DEVRST_N pin names and descriptions. Libero configures unused user I/O as input buffer disabled, output buffer tri-stated with weak pull-up. For more information about unused conditions, see [RT PolarFire SoC FPGA Board Design User Guide](#).

The JTAG bank voltage can be set to operate at 1.8V, 2.5V or 3.3V. The following table lists the JTAG pins.

Table 4-7. JTAG Pins

Pin Names	Direction	Weak Pull-Up/Unused Condition	Description
TMS	Input	DNC	JTAG test mode select
TRSTB	Input	Must be connected to VDDI3 through a 1 kΩ resistor.	JTAG test reset. Must be held low during device operation.
TDI	Input	DNC	JTAG test data in
TCK	Input	Must be connected to VSS through a 10 kΩ resistor	JTAG test clock
TDO	Output	DNC	JTAG test data out

Note: If FPGA is in System Controller Suspend Mode and TRSTB is unused, either an external 1 kΩ pull-down resistor must be connected to TRSTB to override the weak internal pull-up, or TRSTB must be driven low from the external source.

The following table lists the device reset pin.

Table 4-8. Device Reset Pins

Name	Direction	Weak Pull-up	Description
DEVRST_N	Input	22 k Ω	Device reset (asserted low).

The following table lists the SPI interface pins.

Table 4-9. SPI Interface Pins

Name	Direction	Unused Condition	Description
SCK	Bidirectional	Connect to VSS through a 10 k Ω resistor	SPI clock
SS	Bidirectional	Connect to VSS through a 10 k Ω resistor	SPI slave select ¹
SDI	Input	Connect to VDDI3 through a 10 k Ω resistor	SDI input ¹
SDO	Output	DNC	SDO output ¹
SPI_EN	Input	Connect to VSS through a 10 k Ω resistor	SPI enable 0: SPI output tri-stated 1: Enabled Pulled up or down through a resistor or driven dynamically from an external source to enable or tri-state the SPI I/O.
IO_CFG_INTF	Input	Connect to VSS through a 10 k Ω resistor	SPI I/O configuration 0: SPI slave interface 1: SPI master interface Pulled up or down through a resistor or driven dynamically from an external source to indicate whether the shared SPI is a master or slave.

Note:

1. The SCK, SS, SDI, and SDO pins are shared between the system controller and the FPGA fabric. When the system controller's SPI is enabled and configured as a master, the system controller hands over the control of the SPI to the fabric (after device power-up).

The following table lists the special pins.

Table 4-10. Special Pins

Name	Direction	Description	Unused Condition
NC	—	No connect pin. This pin indicates that it is not connected within the circuitry. NC pins can be driven by any voltage or can be left floating with no effect on the operation of the device.	—
DNC	—	Do not connect pin. DNC pins must not be connected to any signals on the PCB, and they must be left unconnected.	—
LPRB_A	Output	Specifies an internal signal for probing (oscilloscope-like feature). The two live probe I/O cells function as either a Live probe or User I/O (GPIO).	Libero-defined DNC
LPRB_B	Output		Libero-defined DNC
FF_EXIT_N	Input	Reserved	—
Shield Signal	Output	Shield signal is required for each DDR data byte signal. It must be driven with maximum drive strength to improve the signal integrity.	Only when DDR controller is in use

4.7. XCVR Interface [\(Ask a Question\)](#)

The transceiver I/O available in the RT PolarFire[®] SoC device is dedicated for high-speed serial communication protocols. Libero Defined DNC pins are pulled up internally when not used in the Libero design. The following table lists the XCVR interface pins.

Table 4-11. XCVR Interface Pins

Name	Direction	Description	Unused Condition
XCVR_xy_REFCLK_P XCVR_xy_REFCLK_N	Input	Differential serial reference clock xy - location x- transceiver number (0, 1, 2 and 3) y- lane number (0, 1, 2 and 3)	DNC
XCVR_x_TxP_P XCVR_x_TxP_N	Output	Differential serial transmit pins. x - transceiver number (0, 1, 2 and 3) y- lane number (0, 1, 2 and 3)	Libero-defined DNC
XCVR_x_RxP_P XCVR_x_RxP_N	Input	Differential serial receive pins. x- transceiver number (0, 1, 2 and 3) y- lane number (0, 1, 2 and 3)	Libero-defined DNC, see PolarFire Family Transceiver User Guide .

5. Package Pin-outs and Pin Compatibility [\(Ask a Question\)](#)

The following table lists the packaging pin-outs of the RT PolarFire® SoC device. Detailed PPAT is available for download, and it contains revision history, device specification, power supplies, pin-outs and BGA graphic. For more information about PPAT, see [RT PolarFire SoC FPGA Pin Package Assignment Table](#).

The following table lists the pin compatible packages of RT PolarFire SoC devices.

Table 5-1. Pin Compatible Packages

Package	Devices
RTPFS460ZT	CG1509
	LG1509
	CB1509
	FC1509
	FCG1509
RTPFS160ZT	FCV784
	FCVG784

Notes:

- FCVG784 is pin compatible between RTPFS160ZT and MPFS160T.
- Pin compatibility does not ensure footprint compatibility. While a single land pad array may be used for prototyping, each package configuration should have their own land pad layout to ensure optimized board level system reliability. Plastic flip chip BGA packages and ceramic column grid packages should not have the same layout for flight modules.

6. Mechanical Drawings [\(Ask a Question\)](#)

The following illustrations show the top-, bottom- and side-views and dimensions of the RT PolarFire® SoC FPGAs.

Figure 6-1. RTPFS460ZT-CG1509 Package Top-View and Side-View

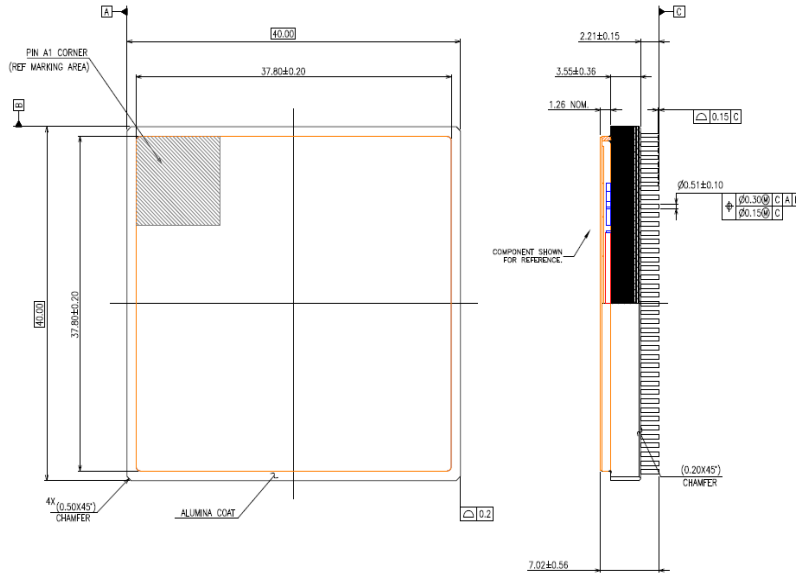


Figure 6-2. RTPFS460ZT-CG1509 Package Bottom-View

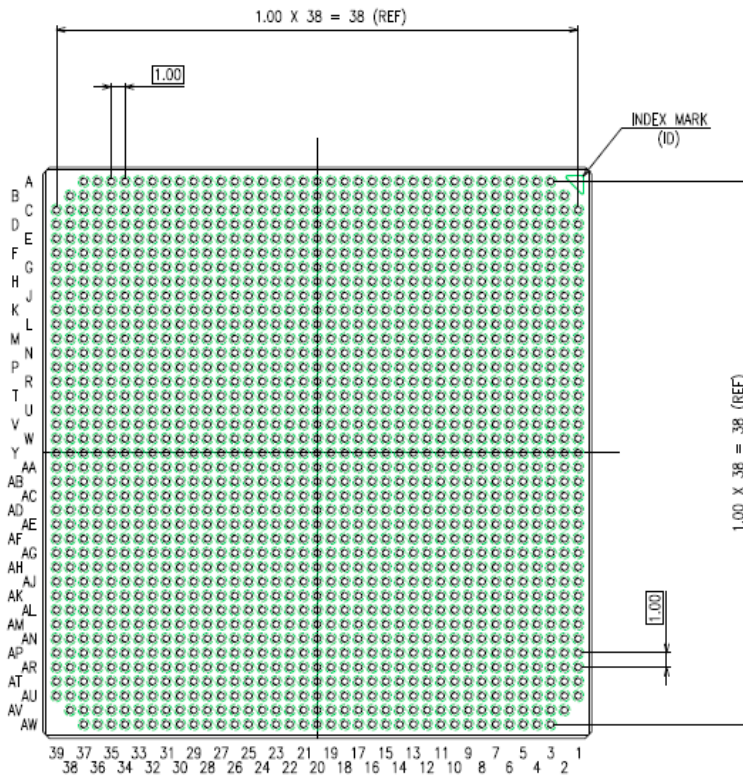


Figure 6-3. RTPFS460ZT-LG1509 Package Top-View and Side-View

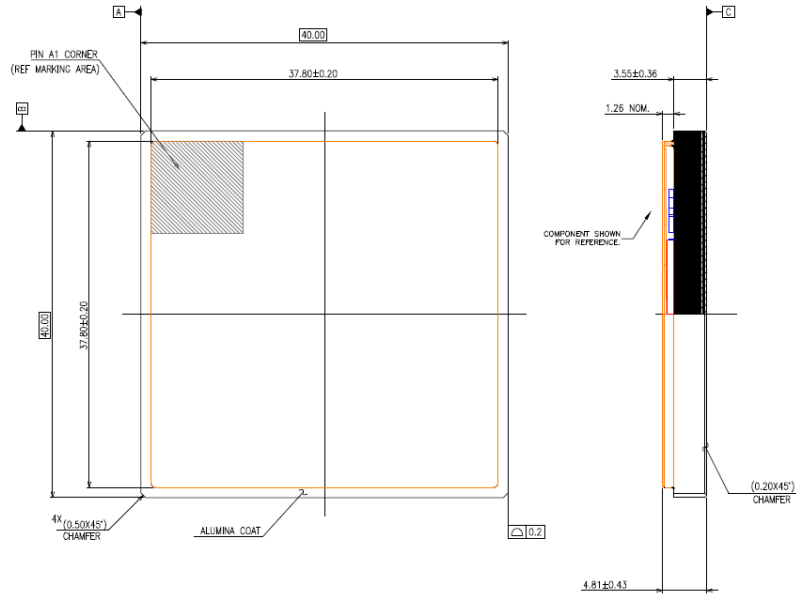


Figure 6-4. RTPFS460ZT-LG1509 Package Bottom-View

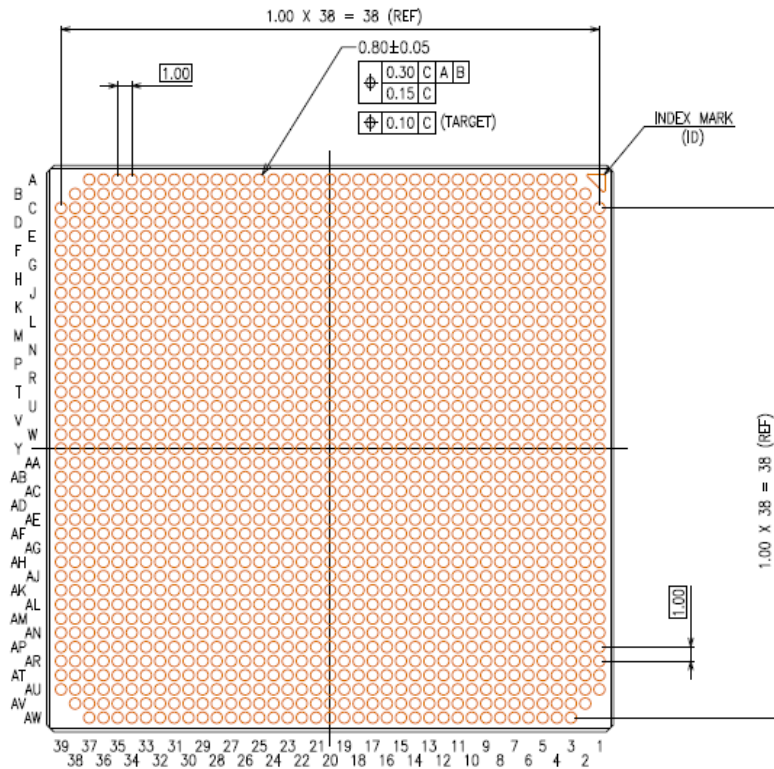


Figure 6-5. RTPFS460ZT-CB1509 Package Top-View and Side-View

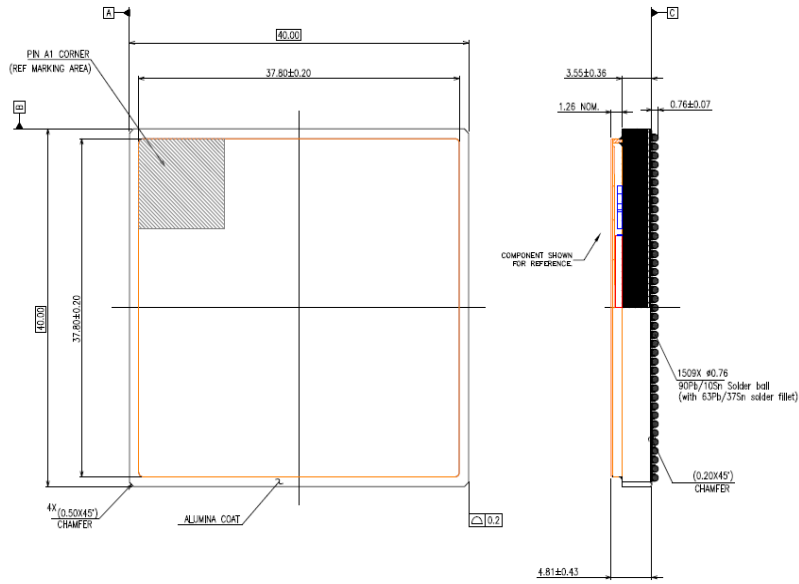


Figure 6-6. RTPFS460ZT-CB1509 Package Bottom-View

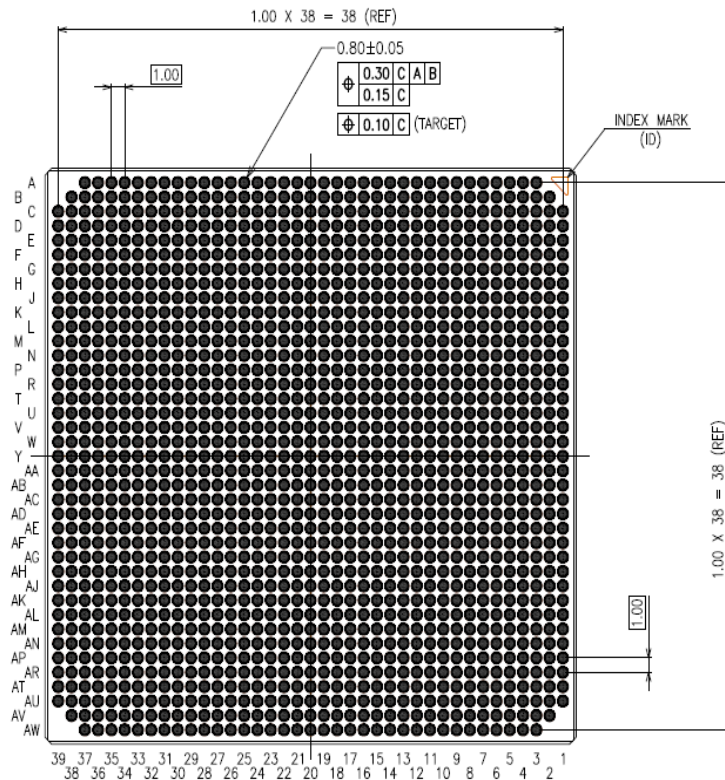


Figure 6-7. RTPFS460ZT-FC1509/FCG1509 Package Top-View and Side-View
To be updated.

Figure 6-8. RTPFS460ZT-FC1509/FCG1509 Package Bottom-View

To be updated.

Figure 6-9. RTPFS160ZT-FCV784/FCVG784 Package Top-View and Side-View

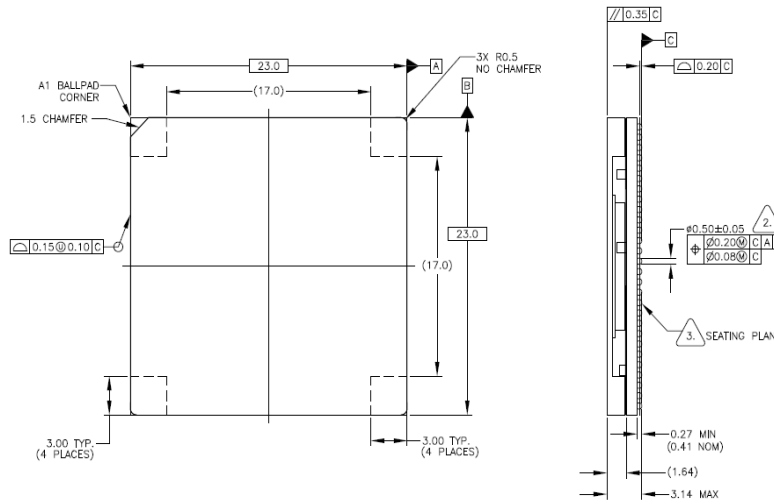
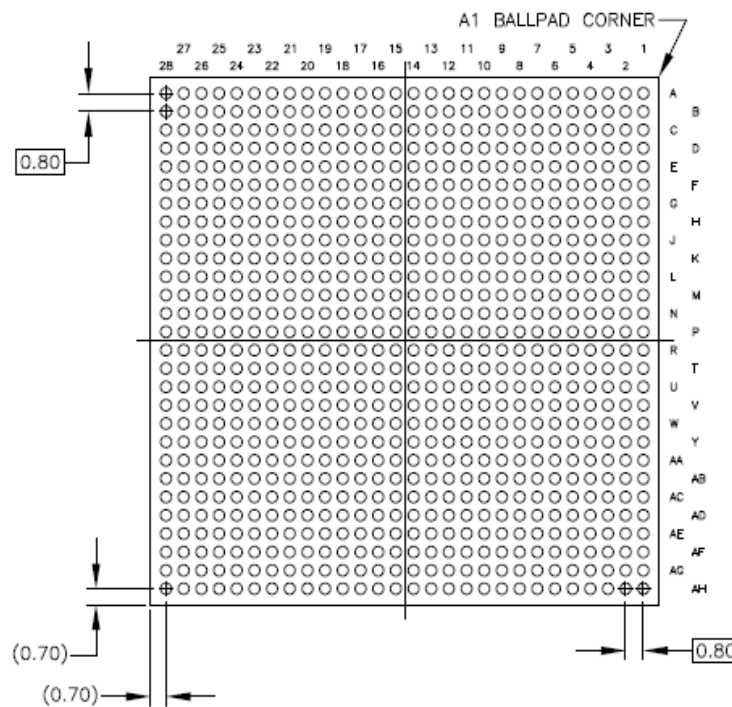


Figure 6-10. RTPFS160ZT-FCV784/FCVG784 Package Bottom-View



7. Package Material Information [\(Ask a Question\)](#)

The following table lists the RT PolarFire® SoC package material information.

Device	RTPFS160ZT		RTPFS460ZT				
Package	FCV784	FCVG784	CG1509	LG1509	CB1509	FC1509	FCG1509
Package Pitch	0.8 mm	0.8 mm	1 mm	1 mm	1 mm	1 mm	1 mm
Substrate Material	Organic Substrate	Organic Substrate	Alumina (ceramic)	Alumina (ceramic)	Alumina (ceramic)	Organic Substrate	Organic Substrate
Solder Ball, Solder Column, or Land Pad Composition	Sn63/Pb37	Sn96.5/Ag3.0/Cu0.5	Sn20/Pb80 columns with spiral copper foil	Gold-Plated Land Pads	Sn20/Pb80	Sn63/Pb37	Sn96.5/Ag3.0/Cu0.5
Solder Bump Composition	Sn98.2/Ag1.8	Sn98.2/Ag1.8	Sn98.2/Ag1.8	Sn98.2/Ag1.8	Sn98.2/Ag1.8	Sn98.2/Ag1.8	Sn98.2/Ag1.8
Lid	AlSiC 4-Post Heat Spreader	AlSiC 4-Post Heat Spreader	Kovar Lid with etched areas	Kovar Lid with etched areas	Kovar Lid with etched areas	AlSiC 12-Post Heat Spreader	AlSiC 12-Post Heat Spreader

8. Thermal Specifications [\(Ask a Question\)](#)

The following table lists the thermal resistances of the RT PolarFire® SoC package device. For information about thermal management, TIM and heat sink removal procedure, see [Thermal Management in Space Applications](#) document.

Table 8-1. RT PolarFire® SoC Package Thermal Resistance

Package	Environment	Theta-JA	Theta-JB	Theta-JC	Psi-JB	Psi-JT	Unit
RTPFS460ZT-CG1509	Still Air	TBD	TBD	TBD	TBD	TBD	°C/W
RTPFS460ZT-FC1509/FCG1509	Still Air	TBD	TBD	TBD	TBD	TBD	°C/W
RTPFS160ZT-FCV784/FCVG784	Still Air	10.55 °C/W	3.66 °C/W	0.359 °C/W	3.50 °C/W	0.103°C/W	°C/W

9. Package Mass [\(Ask a Question\)](#)

The following table lists the package mass information.

Table 9-1. Package Mass Information

Device	Package	Mass Value
RTPFS460ZT	CG1509	TBD
	LG1509	29.57 g
	CB1509	TBD
	FC1509/FCG1509	TBD
RTPFS160ZT	FCV784/FCVG784	3.26 g

10. Package Marking [\(Ask a Question\)](#)

Microchip marks the full ordering part number on the top of each device. The following figures provide details for each character code present on Microchip’s RT PolarFire® SoC FPGA device.

Figure 10-1. RT PolarFire® SoC LG1509/CG1509 Package Marking Format

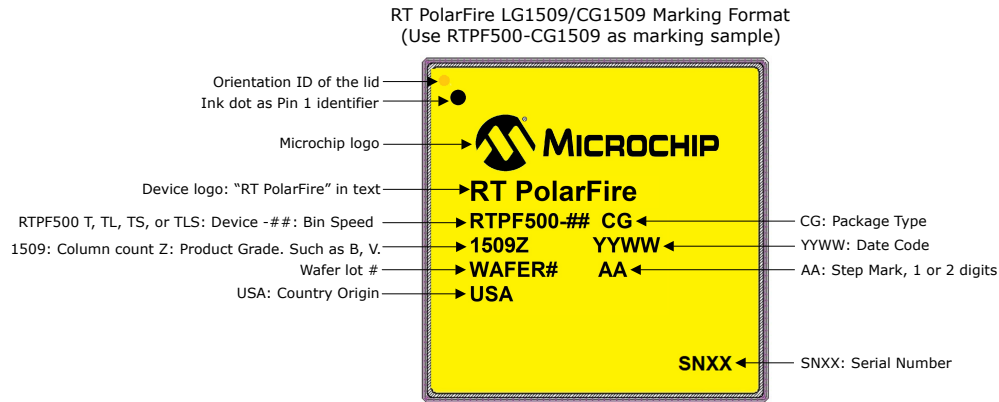


Figure 10-2. RT PolarFire® SoC FCV784/FCVG784 Package Marking Format (M flow)

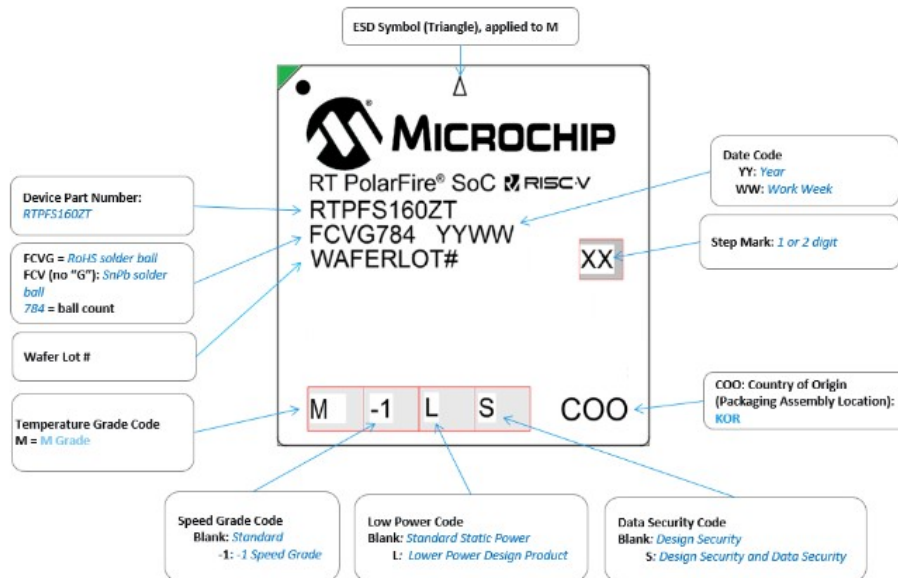
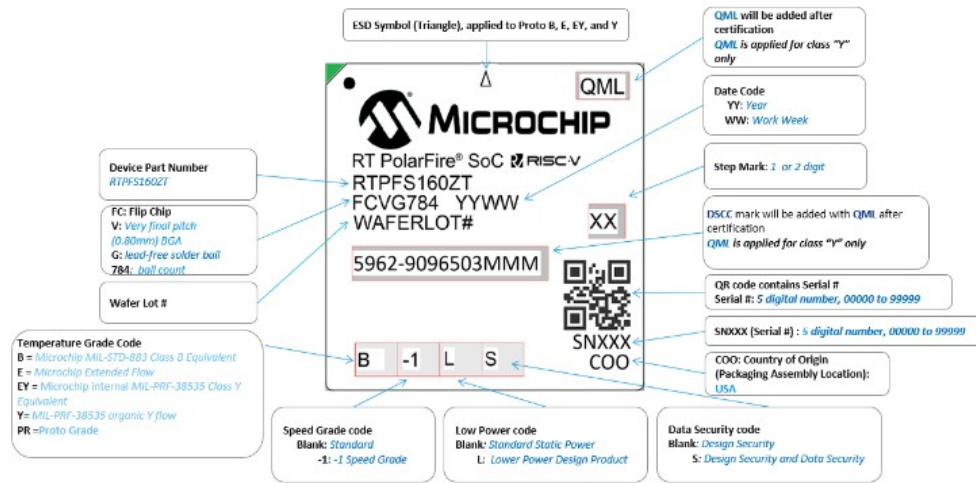


Figure 10-3. RT PolarFire® SoC FCV784/FCVG784 Package Marking Format (Non-M flows)



11. Packing and Shipping [\(Ask a Question\)](#)

The RT PolarFire® SoC device is packed in jewel boxes or trays, which are used to pack most of the Microchip surface-mount devices. Trays provide excellent protection from mechanical damage. In addition, they are manufactured using the anti-static material to provide limited protection against Electrostatic Discharge (ESD) damage. The Moisture Sensitivity Level (MSL) of each of these packages is MSL 4.

For more information on how to pack and ship ceramic column grid array packages, see "Section 3, 4 and 5" of [Ceramic Column Grid Array](#).

The following table lists the maximum number of devices packed in a jewel box.

Table 11-1. Maximum Device Counts per Jewel Box

Package	Maximum Number of Devices per Jewel Box
CG1509	1
LG1509	1
CB1509	1

The following table lists the maximum number of devices packed in a tray.

Table 11-2. Maximum Device Counts per Tray

Package	Maximum Number of Devices per Tray
FC1509	12
FCG1509	12
FCV784	60
FCVG784	60

12. Thermal Management (Ask a Question)

Microchip RT PolarFire[®] SoC FPGA is available in a lidded Flip-Chip BGA (FCBGA) package. Lidded FCBGA features a controlled bond-line Thermal Interface Material (TIM) thickness that reduces the thermal resistance (Θ_{JC}) between the junction and the externally applied thermal solution. The lid or heat spreader also spreads the heat away from the die to the package perimeter and to the printed circuit board. Heat is also dissipated through the bottom of the package through the solder balls. The thermal resistance for this is Θ_{JB} .

For more information on thermal management for both ceramic and plastic packages, see [Thermal Management and Mounting Methods for RTG4™ and RT PolarFire[®] FPGAs in Space Applications](#).

The following figures show the RT PolarFire SoC ceramic and plastic package cross-section.

Figure 12-1. RT PolarFire[®] SoC Ceramic Package Cross-Section

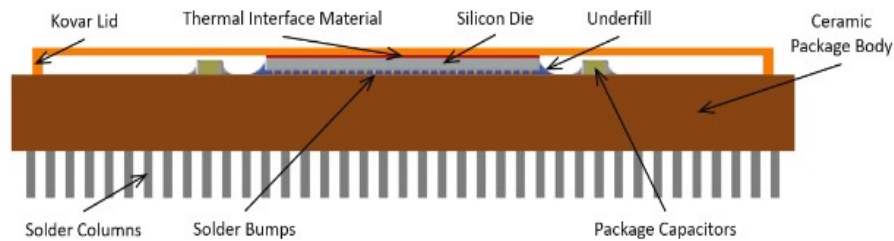
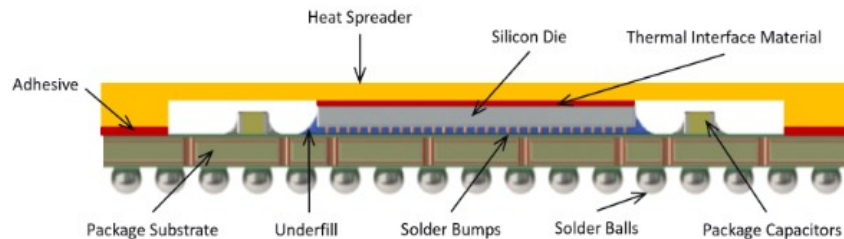


Figure 12-2. RT PolarFire[®] SoC Plastic Package Cross-Section



13. PCB Design (Ask a Question)

When designing the land pad layout for FC/FCG and CG/CGG packages, it is recommended to have the dimensions as listed in the following table.

The following figure shows the RT PolarFire® SoC package land pad layout for both single trace breakout and dual trace breakout.

Figure 13-1. RT PolarFire® SoC Package Land Pad Layout (Single Trace Breakout and Dual Trace Breakout)

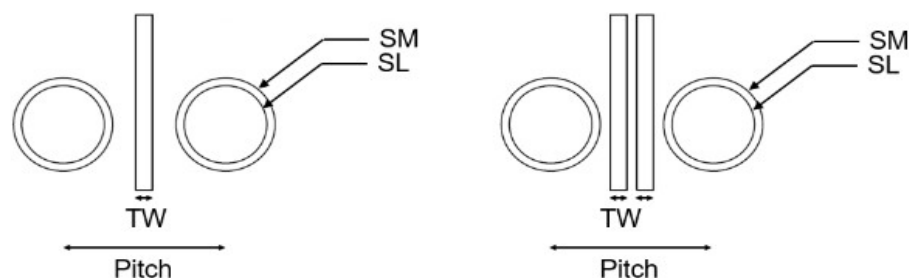


Table 13-1. RT PolarFire® SoC Plastic Flip-Chip BGA and Ceramic Column Grid Array Package Land Pad Layout Dimensions

Package	FC1509/FCG1509	CG1509	FCV784/FCVG784
Solder Column/Ball Pitch	1mm	1 mm	0.8 mm
PCB Pad Diameter (SL)	0.50 mm	0.70 mm	0.40 mm
PCB Solder Mask Opening Diameter (SM)	0.60 mm	0.80 mm	0.50 mm
Trace Width (Single and Dual Trace Breakout) (TW)	Determined by the manufacturer based on the application and the design needs		

Note: The package layout drawings and dimensions are provided for non-solder mask defined BGA pads which are recommended for the devices.

It is not recommended to have a single land pad layout to accommodate both FC/FCG and CG/CGG packages. While a single land pad array might be used for prototyping, each package configuration must have their own land pad layout to ensure optimized board level system reliability. Plastic flip-chip BGA packages and ceramic column grid packages must not have the same layout for flight modules.

For more information about PCB design rules for BGA and CCGA packages, see [AN5672: PolarFire FPGA Package Fanout Application Note](#) and [AN5557: Ceramic Column Grid Array Application Note](#).

14. Revision History [\(Ask a Question\)](#)

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

Table 14-1. Revision History

Revision	Date	Description
A	09/2025	Initial Revision

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