

Introduction [\(Ask a Question\)](#)

Good board design practices are required to achieve expected performance from both Printed Circuit Boards (PCBs) and RT PolarFire® SoC devices. High-quality and reliable results depend on minimizing noise levels, preserving signal integrity, meeting impedance and power requirements and using appropriate transceiver protocols. These guidelines must be treated as a supplement to the standard board-level design practices.

This document is intended for readers who are familiar with the RT PolarFire SoC device, experienced in digital board design and know about the electrical characteristics of systems. It discusses power supplies, high-speed interfaces, various control interfaces and the associated peripheral components of RT PolarFire SoC FPGAs.

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1. Designing the Board (Ask a Question)

RT PolarFire® SoC FPGAs are flash-based FPGAs that support various high-speed memory interfaces such as DDR3/DDR4, lowest power 10 Gbps transceiver (XCVR), built-in low-power dual PCIe® Gen2 and fabric I/O such as High-Speed I/O (HSIO) and General-Purpose I/O (GPIO).

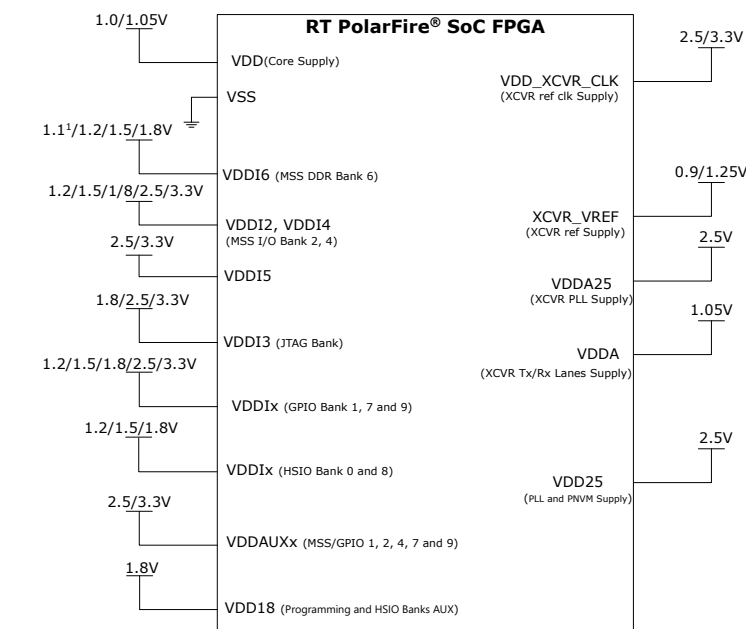
Subsequent sections discuss the following:

- [Power Supplies](#)
- [User I/O](#)
- [Clocks](#)
- [Reset](#)
- [Device Programming](#)
- [Transceiver](#)
- [AC and DC Coupling](#)
- [Brownout Detection](#)

1.1. Power Supplies (Ask a Question)

The following illustration shows the typical power supply requirements for RT PolarFire® SoC devices, and the recommended connections of power rails when every part of the device is used in a system. For information on decoupling capacitors associated with individual power supplies, see [RT PolarFire SoC Decoupling Capacitors](#).

Figure 1-1. Power Supplies



Note:
¹1.1V is for LPDDR4 support. For more information see *PolarFire Family Memory Controller User Guide*.

To calculate the number of decoupling capacitors, it is important to know the target impedance of the power plane. Target impedance is calculated as follows:

$$Z_{Max} = \% \text{ Ripple} \times \frac{V_{supply}}{I_{trans}}$$

Where,

V_{supply}: Supply voltage of the power plane.

% Ripple: Percentage of ripples that is allowed on the power plane. For more information about ripple, see Recommended Operating Conditions table in the [RT PolarFire SoC Datasheet](#).

I_{trans}: Transient current drawn on the power plane. The transient current is half of the maximum current. Maximum current is taken from the power calculator sheet.

Z_{max}: Target impedance of the plane.

For the device to operate successfully, power supplies must be free from unregulated spikes and the associated grounds must be free from noise. All overshoots and undershoots must be within the absolute maximum ratings provided in the [RT PolarFire SoC Datasheet](#).

The following table lists the various power supplies required for RT PolarFire SoC FPGAs.

Table 1-1. Supply Pins

Name	Description
XCVR_VREF	Voltage reference for transceivers
VDD_XCVR_CLK	Power to input buffers for the transceiver reference clock
VDDA25	Power to the transceiver PLL
VDDA ¹	Power to the transceiver TX and RX lanes
VSS	Core digital ground
VDD ²	Device core digital supply
VDDI3 (JTAG Bank) ³	Power to JTAG bank pins
VDDI5 ⁴	VDDI5 power to MSS SGMII banks and MSS dedicated clocks
VDDI2	VDDI2 power to MSS peripheral banks
VDDI4	Power to MSS peripheral banks
VDDI6	Power to MSS DDR banks
VDDIx (GPIO Banks)	Power to GPIO bank pins
VDDIx (HSIO Banks)	Power to HSIO bank pins
VDD25	Power to corner PLLs and PNVN
VDD18	Power to programming and HSIO auxiliary supply
VDDAUXx	Power to GPIO/MSS auxiliary supply

Notes:

1. VDDA Supply Requirements—VDDA must be powered at exactly 1.05V. For complete details, see the "Recommended Operating Conditions" section in the [RT PolarFire SoC Datasheet](#). This is a quiet supply critical to meeting all datasheet specifications. User must strictly follow the decoupling capacitor guidelines in [RT PolarFire SoC Decoupling Capacitors](#). Use a linear regulator if required to guarantee supply quietness—no exceptions.
2. VDD Supply Requirements—VDD must be powered at exactly 1.0V or 1.05V. For complete details, see the "Recommended Operating Conditions" section in the [RT PolarFire SoC Datasheet](#). This is a critical supply for device performance. User must strictly follow the decoupling capacitor guidelines in [RT PolarFire SoC Decoupling Capacitors](#) to ensure performance.
3. VDDI3 must be powered before or at the same time as the other main supplies (VDD, VDD18, and VDD25) for the device to start initialization.

- VDDI5 must be powered-up before or along with VDD. VDDI5 must reach its datasheet minimum value before VDD reaches a functional level and also before the time when MSS is ready to execute its first instruction (referred to as T_{CPU} in the datasheet).
- For information on how to connect the VSS_MONITOR and VDD_MONITOR package pins, see [Voltage Monitor Detector I/Os](#).

VREFx is the reference voltage for DDR3 and DDR4 signals. VREF voltages can be generated internally and externally.

- Internal VREF: It is not subjected to PCB and package inductance and capacitance loss. These changes provide the highest performance and can be programmed as required by the DDR controller.
- External VREF: It is fixed and cannot be programmed as required. The PCB and the package inductance and capacitance impact the VREF performance.

If VDDI and VDDAUX need to be configured to the same voltage (2.5V or 3.3V), ensure both VDDI and VDDAUX are supplied from the same regulator. Do not use different regulators to source these rails. This prevents any voltage variations between VDDI and VDDAUX. In this case, the board must not supply the VDDI and VDDAUX from individual voltage supplies.

When a GPIO bank requires the VDDI to be less than 2.5V (1.2V, 1.5V or 1.8V), the VDDAUX for that bank must be tied to 2.5V supply irrespective of the VDDI supply. The VDDI requires a separate supply for the specific I/O type (1.5V or 1.8V).

Notes:

- The on-chip Power-on-Reset (POR) circuitry mandates that VDD, VDD18, and VDD25 supplies ramp monotonically from 0V to the minimum recommended operating voltage. Any deviation from this strict monotonic ramp will compromise device functionality and its adherence to the datasheet specifications.
- User must initiate the I/O calibration only when both the VDDA and XCVR_VREF supplies are up.

For a detailed pin description, see [RT PolarFire SoC FPGA Packaging and Pin Descriptions User Guide](#).

1.1.1. RT PolarFire SoC Decoupling Capacitors [\(Ask a Question\)](#)

The following table lists the requirement of all decoupling capacitors for the RTPFS460ZT-CG1509 device. This is not a recommendation—it is a strict requirement. Users must implement these capacitors precisely in their schematics and board layouts. Failure to comply will result in unreliable operation, performance degradation and void the device compliance to datasheet specifications.

Table 1-2. Power-Supply Decoupling Capacitors¹ —RTPFS460ZT-CG1509 (1 mm)

Pin	Multi-Layer Ceramic Capacitor (MLCC)							Tantalum
	1 nF	4.7 nF	10 nF	47 nF	4.7 μF	10 μF	100 μF	330 μF
VDD	—	—	10	4	7	—	1	3
VDDA	2	2	2	—	3	—	1	—
VDD18	—	—	—	—	2	—	2	—
VDD25	—	—	—	—	3	—	1	—
VDDA25	—	—	1	—	4	—	1	—
VDDI2 (MSSIO)	1	—	—	—	—	1	1	—
VDDI3 (JTAG)	—	—	—	—	—	3	—	—
VDDI4 (MSSIO)	1	—	—	—	—	1	1	—
VDDI5 (MSS SGMII)	1	—	—	—	—	1	1	—
VDDI6 (MSS DDR)	1	—	—	—	—	2	1	—
VDDAUX1 ²	—	—	1	—	—	2	1	—

Table 1-2. Power-Supply Decoupling Capacitors¹ —RTPFS460ZT-CG1509 (1 mm) (continued)

Pin	Multi-Layer Ceramic Capacitor (MLCC)							Tantalum
	1 nF	4.7 nF	10 nF	47 nF	4.7 μF	10 μF	100 μF	330 μF
VDDAUX2 ²	—	—	1	—	—	2	1	—
VDDAUX4 ²	—	—	1	—	—	2	1	—
VDDAUX7 ²	—	—	1	—	—	2	1	—
VDDAUX9 ²	—	—	1	—	—	2	1	—
VDDI1 (GPIO Bank ³)	1	—	—	—	—	1	1	—
VDDI7 (GPIO Bank ³)	1	—	—	—	—	1	1	—
VDDI9 (GPIO Bank ³)	1	—	—	—	—	1	1	—
VDDI0 (HSIO Bank ⁴)	1	1	—	—	1	—	1	—
VDDI8 (HSIO Bank ⁴)	1	1	—	—	1	—	1	—
VDD_XCVR_CLK	—	—	—	—	—	3	—	—
XCVR_VREF	—	—	—	—	—	1	—	—

Notes:

1. The guidelines are provided on how to effectively decouple only the FPGA device. If the power source is placed on a different PCB or delivered through interconnects (flex cables or connectors), ensure an effective power delivery to the FPGA. Also, follow the recommended operational conditions as per the [RT PolarFire SoC Datasheet](#).
2. Required Decoupling Capacitor for each VDDAUXx.
3. Required Decoupling Capacitor for each GPIO bank.
4. Required Decoupling Capacitor for each HSIO bank.

The following table lists the requirement of all decoupling capacitors for the RTPFS160ZT-FCV784 (1 mm) device. This is not a recommendation—it is a strict requirement. Users must implement these capacitors precisely in their schematics and board layouts. Failure to comply will result in unreliable operation, performance degradation and void the device compliance to datasheet specifications.

Table 1-3. Power-Supply Decoupling Capacitors¹ — RTPFS160ZT-FCV784 (0.8 mm)

Pin	Multi-Layer Ceramic Capacitor (MLCC)							Tantalum
	1 nF	4.7 nF	10 nF	47 nF	4.7 μF	10 μF	100 μF	330 μF
VDD	—	—	10	4	7	—	1	3
VDD18	—	—	—	—	2	—	2	—
VDD25	—	—	—	—	3	—	1	—
VDDA	2	2	2	—	3	—	1	—
VDDA25	2	—	1	—	2	—	1	—
VDDI2 (MSSIO)	2	—	—	—	—	—	1	—
VDDI3 (JTAG)	—	—	—	—	—	3	—	—
VDDI4 (MSSIO)	2	—	—	—	—	—	1	—
VDDI5 (MSS SGMII)	2	—	—	—	—	—	1	—
VDDI6 (MSS DDR)	1	—	—	—	—	2	1	—
VDDAUX1 ²	—	—	1	—	—	2	1	—
VDDAUX2 ²	—	—	1	—	—	2	1	—
VDDAUX4 ²	—	—	1	—	—	2	1	—

Table 1-3. Power-Supply Decoupling Capacitors¹ — RTPFS160ZT-FCV784 (0.8 mm) (continued)

Pin	Multi-Layer Ceramic Capacitor (MLCC)							Tantalum
	1 nF	4.7 nF	10 nF	47 nF	4.7 μ F	10 μ F	100 μ F	330 μ F
VDDAUX7 ²	—	—	1	—	—	2	1	—
VDDAUX9 ²	—	—	1	—	—	2	1	—
VDDI1 (GPIO Bank ³)	1	—	—	—	—	1	1	—
VDDI7 (GPIO Bank ³)	1	—	—	—	—	1	1	—
VDDI9 (GPIO Bank ³)	1	—	—	—	—	1	1	—
VDDI0 (HSIO Bank ⁴)	1	1	—	—	1	—	1	—
VDDI8 (HSIO Bank ⁴)	1	1	—	—	1	—	1	—
VDD_XCVR_CLK	—	—	—	—	—	3	—	—
XCVR_VREF	—	—	—	—	—	1	—	—

Notes:

1. The guidelines are provided on how to effectively decouple only the FPGA device. If the power source is placed on a different PCB or delivered through interconnects (flex cables or connectors), ensure an effective power delivery to the FPGA. Also, follow the recommended operational conditions as per the [RT PolarFire SoC Datasheet](#).
2. Required Decoupling Capacitor for each VDDAUXx.
3. Required Decoupling Capacitor for each GPIO bank.
4. Required Decoupling Capacitor for each HSIO bank.

Alternative decoupling capacitors may only be used if their physical sizes meet or exceed the performance of the specified network. Any substitution mandates rigorous analysis of the resulting power distribution network's impedance versus frequency to eliminate resonant spikes. See [Figure 1-1](#) for power supply design guidelines. Failure to perform this analysis may cause system related voltage ripple and performance issues and instability.

For more information about the internal package capacitance for power supplies associated with RT PolarFire SoC packages, see [RT PolarFire SoC FPGA Packaging and Pin Descriptions User Guide](#).

The following table lists the required decoupling capacitors for RT PolarFire SoC packages.

Table 1-4. Recommended Decoupling Capacitors For RT PolarFire SoC Devices

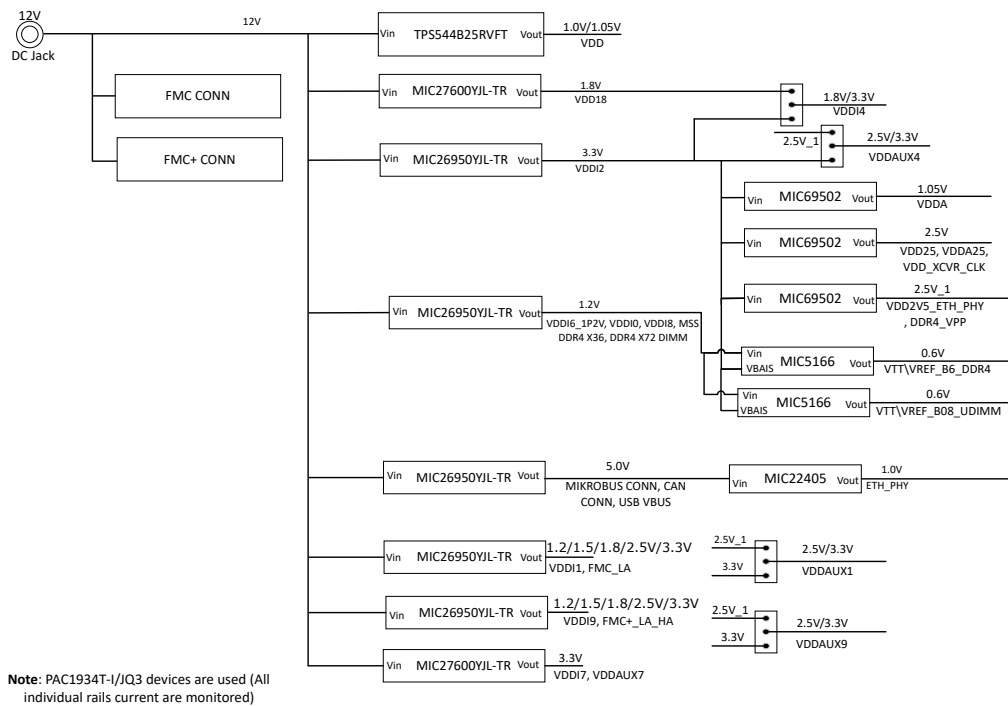
Value	Package
330 μ F	2917
100 μ F	1206
10 μ F	0805
4.7 μ F	0402
47 nF	0402
10 nF	0402
4.7 nF	0402
1 nF	0402

Note: User must use equivalent space-grade decoupling capacitor parts. For more information about Packaging Decoupling Capacitors, see [RT PolarFire SoC FPGA Packaging and Pin Descriptions User Guide](#).

1.1.2. Power-Supply Topology [\(Ask a Question\)](#)

RT PolarFire SoC FPGAs require multiple power supplies. The following figure shows a power supply topology example for generating the required power supplies from a single 12V source. This example is based on the RT PolarFire SoC Development Kit with RTPFS460ZT device, with DDR3 and DDR4 interfaces.

Figure 1-2. Example Power-Supply Topology



The following table lists the suggested Microchip power regulators for RT PolarFire SoC FPGA voltage rails.

Table 1-5. Power Regulators

Voltage Rail	Part Number	Description	Current
VDD (1.0V, 1.05V)	TPS544B25RVFT	IC REG BUCK ADJ 20A 40LQFN	20A
VDD18 (1.8V)	MIC27600YJL-TR	IC REG BUCK ADJUSTABLE 12A 28MLF	7A
VDDI4 (1.8V/3.3V)	MIC27600YJL-TR	IC REG BUCK ADJUSTABLE 12A 28MLF	7A
VDDI1, FMC_LA 1.2V/1.5V/1.8V/2.5V/3.3V	MIC26950YJL-TR	IC REG BUCK ADJUSTABLE 12A 28MLF	12A
VDDI2 (3.3V)	MIC26950YJL-TR	IC REG BUCK ADJUSTABLE 12A 28MLF	12A
VDDI7, VDDAUX7 (3.3V)	MIC27600YJL-TR	IC REG BUCK ADJUSTABLE 12A 28MLF	7A
VDDI9, FMC+_LA_HA 1.2V/1.5V/1.8V/2.5V/3.3V	MIC26950YJL-TR	IC REG BUCK ADJUSTABLE 12A 28MLF	12A
MikroBus Conn, CAN Conn, USB VBUS (5.0V)	MIC26950YJL-TR	IC REG BUCK ADJUSTABLE 12A 28MLF	12A
VDDI6_1P2V, VDDI0, VDDI8, MSS DDR4 X36, DDR4 X72 DIMM (1.2V)	MIC26950YJL-TR	IC REG BUCK ADJUSTABLE 12A 28MLF	12A

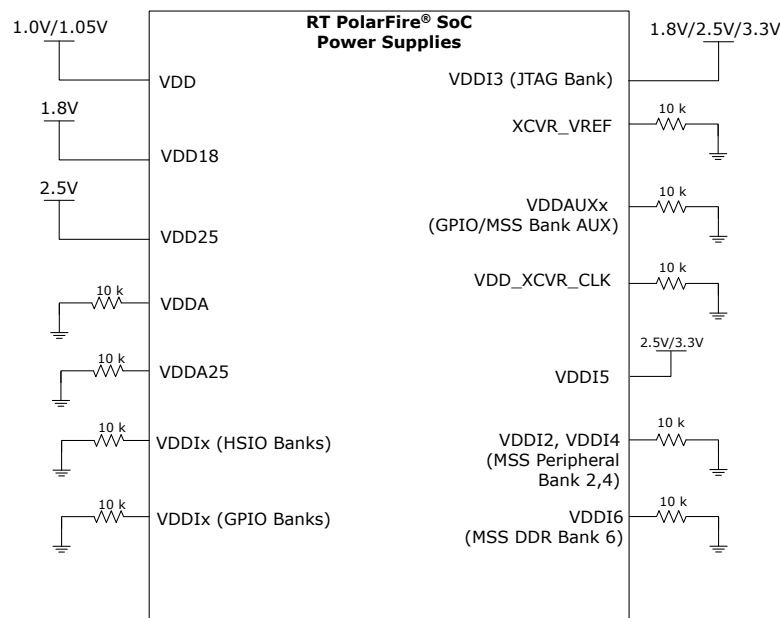
Table 1-5. Power Regulators (continued)			
Voltage Rail	Part Number	Description	Current
VDDA (1.05V)	MIC69502	IC REG LINEAR POS ADJ 5A SPAK-7	5A
VDD25, VDDA25, VDD_XCVR_CLK (2.5V)	MIC69502	IC REG LINEAR POS ADJ 5A SPAK-7	5A
VDD2V5_ETH_PHY, DDR4_VPP (2.5V_1)	MIC69502	IC REG LINEAR POS ADJ 5A SPAK-7	5A
VTTVREF_B6_DDR4 (0.6V)	MIC5166	IC PWR SUP 3A HS DDR TERM 10MLF	3A
VTTVREF_B08_UDIMM (0.6V)	MIC5166	IC PWR SUP 3A HS DDR TERM 10MLF	3A

Note: You must use equivalent hi-reliability parts.

1.1.3. Unused Power Supply [\(Ask a Question\)](#)

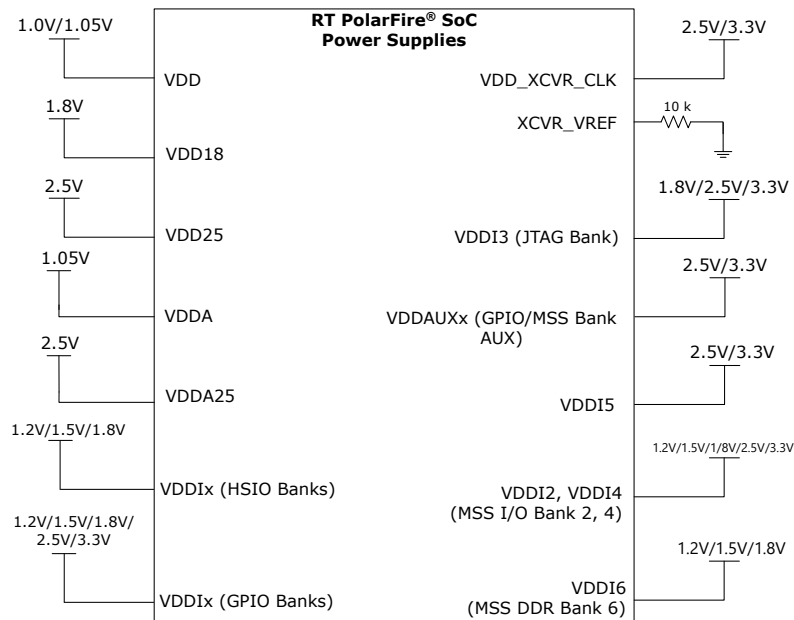
The following figure shows the power configuration of unused supplies when you need to reduce leakage and power for the system.

Figure 1-3. Option 1 for Unused Connections



The following figure shows the power configuration of unused supplies. This option can be used when there is an intent to power-up the various supplies at a later time in the system and the I/Os are not being used.

Figure 1-4. Option 2 for Unused Connections



Tip: To simplify the board-level routing, multiple 10 k Ω resistors can be used as required. The power supplies can also be grouped into a single 10 k Ω resistor and tied-off to VSS.

1.1.4. Pin Assignment Tables [\(Ask a Question\)](#)

The Packaging Pin Assignment Table (PPAT) is available on the [RT PolarFire SoC Documentation](#) web page. PPAT contains information about the recommended DDR pin-outs, PCI EXPRESS capability for XCVR-0, DDR Lane information for IO CDR, generic IOD interface pin placement and unused condition for package pins.

1.2. I/O Glitch [\(Ask a Question\)](#)

A glitch might occur during power-up or power-down for GPIO or HSIO outputs in RT PolarFire[®] SoC devices. The glitch can occur before or after the device reaches a functional state. These glitches are not observed on LVDS outputs or Transceiver I/Os. No reliability issues are caused by either of the glitch types. Following are the types of glitches that can occur.

- Parasitic glitches might occur for GPIOs or HSIOs before the device reaches functional state, with a maximum glitch of 1V with a 0.4 ms width. This type of glitch can typically be ignored. It is recommended to use a 100K pull-down resistor on critical signals¹ of the GPIO or HSIO pins if this type of glitch cannot be ignored. No glitches are observed once mitigation recommendations are placed. This may occur for both erased/blank and programmed units.
- Another type of glitch might occur on GPIOs and HSIOs during power-on sequencing or boot-up. This is due to a weak pull-up resistor being enabled by default on an input, output or bidirectional I/O. To mitigate this glitch, use the Libero[®] SoC I/O Editor or PDC constraint to program a weak pull-down on the output buffer on the specified I/O. This might occur for both erased/blank and programmed units.
- The last type of glitch might occur for both erased/blank and programmed units after the device reaches functional state. This type of glitch is related to the power-up and power-down sequence

¹ Critical outputs such as reset or clock of the HSIO or GPIOs going into another device.

of VDDI and VDDAUX supplies. This occurs only on GPIOs where the VDDI is 1.5V or 1.8V only, with a maximum glitch of 1V with a 0.8 ms width during power-up and a maximum glitch of 1.8V with a 1 ms width during power down. For HSIOs where the VDDI is 1.5V or 1.8V, only a maximum glitch of 600 mV and 1.5 ms width might occur at power-up and a maximum glitch of 220 mV and 200 μ s width might occur at power-down.

To mitigate the post functional state glitch, follow the recommendations in the following tables.

Table 1-6. Power Sequencing¹ (For GPIO)

Use Cases for GPIO		Power-up Sequencing Requirement for Mitigating Glitches ²	Power-down Sequencing Requirements for Mitigating Glitches ²
VDDI	VDDAUX	—	—
1.2V	2.5V	No glitch occurs	No glitch occurs
1.5V	2.5V	Power up VDDAUX before VDDI of that bank	Power down VDDI before VDDAUX of that bank
1.8V	2.5V	Power up VDDAUX before VDDI of that bank	Power down VDDI before VDDAUX of that bank
2.5V	2.5V	Power VDDAUX and VDDI from the same regulator	No glitch occurs
3.3V ³	3.3V ³	Power VDDAUX and VDDI from the same regulator	No glitch occurs

Notes:

1. No glitches are observed once mitigation recommendations are placed.
2. This power sequence does not mitigate any parasitic glitches. As mentioned, add a 100K pull-down resistor to critical signals of GPIO or HSIO pins to mitigate parasitic glitches.
3. You must review and understand the GPIO Single Event Latchup (SEL) data in the RT PolarFire RTPF500ZT Heavy Ion Test Results report before selecting 3.3V for VDDI and VDDAUX supplies. The radiation test reports are available on the [FPGA Radiation and Reliability Data](#) web page.

Table 1-7. Power Sequencing¹ (For HSIO)

Use Cases for HSIO		Power-up Sequencing Requirement for Mitigating Glitches ²	Power-down Sequencing Requirements for Mitigating Glitches ²
VDDI	VDD18	—	—
1.2V	1.8V	No glitch occurs	No glitch occurs
1.5V	1.8V	Power up VDD18 before VDDI of that bank	Power down VDDI before VDD18, VDD, VDD25 of that bank
1.8V	1.8V	Power up VDD18 before VDDI of that bank ³	Power down VDDI before VDD18, VDD, VDD25 of that bank

Notes:

1. No glitches are observed once mitigation recommendations are placed.
2. This power sequence does not mitigate any parasitic glitches. As mentioned, add a 100K pull-down resistor to critical signals of GPIO or HSIO pins to mitigate parasitic glitches.
3. When VDDI = 1.8V and VDD18 = 1.8V, VDDI and VDD18 must be sourced from two separate power sources to meet the power sequencing requirements described in [Table 1-7](#). This mitigates any potential I/O glitch.



Important:

- A glitch can occur on GPIO pins during JTAG programming if power is disrupted. The glitch can be mitigated by powering down VDDI before VDDAUX, VDD and VDDI3.
- During JTAG programming of a blank device, a glitch can occur on the MSS I/O pins. For more information, see [PolarFire Family Programming User Guide](#).

1.3. In-Rush Current [\(Ask a Question\)](#)

During power-down, an in-rush current (including standby current) of 6.5A on RTPFS460ZT, might be observed on VDD for a duration of 10 μ s. This occurs when VDD, VDD18 or VDD25 crosses the Power-On Reset trip point voltage levels during ramp down. This in-rush current on VDD does not impact the device reliability.

To mitigate the in-rush current, assert DEVRST_N before powering down VDD, VDD18 or VDD25. No in-rush current during power-down is observed on VDD once the mitigation recommendation is followed.

For device in-rush current during power-up, see the PolarFire Power Estimator Tab called **Current Breakdown** after setting the appropriate RT PolarFire SoC device settings on the **Summary** Tab. For more information about PolarFire Power Estimator, see [PolarFire FPGA and PolarFire SoC FPGA Power Estimator User Guide](#).

1.4. User I/O [\(Ask a Question\)](#)

RT PolarFire[®] SoC FPGAs have two types of I/O buffers: HSIO and GPIO. HSIO buffers are optimized for single-ended buffers with supplies from 1.2V to 1.8V. GPIO buffers support single-ended and true differential interfaces with supplies from 1.2V to 3.3V. RT PolarFire SoC FPGAs support the following types of I/O Banks:

- GPIO Banks: These Banks support I/O buffers for single-ended and true differential signals from 1.2V to 3.3V.
- HSIO Banks: These Banks support optimized I/O buffers for single-ended and true differential signals from 1.2V to 1.8V.
- MSS I/Os: These banks can support I/O buffer for single-ended signals from 1.2V to 3.3V.
- MSS DDR I/Os: These banks can support I/O buffer for single-ended and differential, per the Pin table signals at 1.2V and 1.5V to 1.8V.
- MSS SGMII I/Os: These banks can support I/O buffer for single-ended and differential, per the Pin table signals at 2.5V or 3.3V.

Notes:

- When the HSIO bank is configured as an LVDS receiver, the concerned I/Os must be connected externally by a 100 Ω resistor.
- For supporting cold sparing application, see [Cold Sparing](#) for guidance on pin assignment.
- Before selecting 3.3V supplies for 3.3V capable I/O banks, you must review and understand the Single Event Latchup (SEL) data in the RT PolarFire RTPF500ZT Heavy Ion Test Results report available on the [FPGA Radiation and Reliability Data](#).

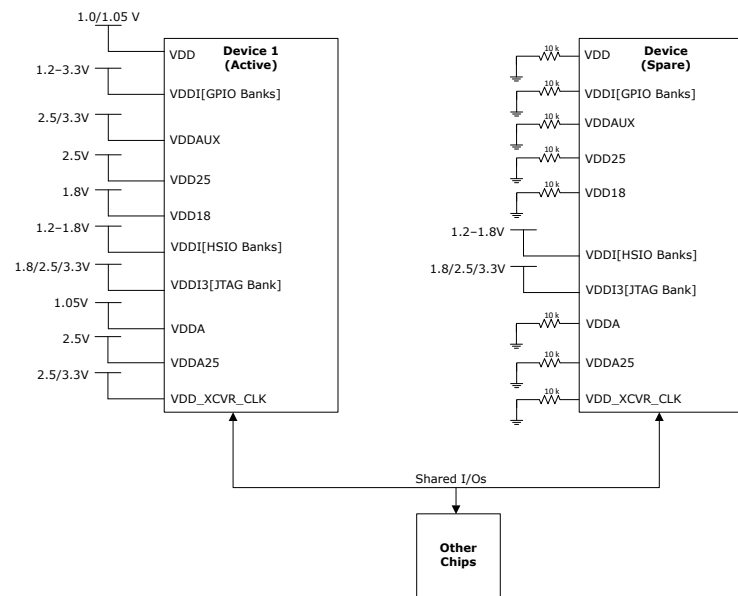
For more information about key features of I/O buffers and supported standards, see [RT PolarFire SoC FPGA Packaging and Pin Descriptions User Guide](#) and [PolarFire Family I/O User Guide](#).

1.4.1. Cold Sparing [\(Ask a Question\)](#)

RT PolarFire[®] SoC devices support cold sparing for GPIO and HSIO. Cold sparing is implemented by connecting the devices as shown in the following figure. The system board has two RT PolarFire SoC devices in parallel, and the devices share I/Os. The spare device has its HSIO VDDI banks powered up to prevent I/O leakage through the ESD diodes. As a result, low power and a protected state for the spare device is established. The spare device can be changed to active device by powering-up all the supplies. The active device can be changed to spare device by powering down all the supplies, except HSIO VDDI banks.

A typical cold sparing application integrates two parallel devices with shared I/O connections, as shown in the following figure.

Figure 1-5. Cold Sparing



For supporting cold sparing applications on GPIO I/Os:

- All GPIO banks support single-ended and differential signaling.

Naming Convention:

- GPIOXXPBY: I/O pair XX, bank Y, P node
- GPIOXXNBY: I/O pair XX, bank Y, N node
- Both nodes of any GPIO pair (for example, GPIO242PB1 and GPIO242NB1) can be used for single-ended signals.

The following points summarize the cold sparing recommendations:

- For a GPIO pair (for example, GPIO242[P/N]B1):
 - Use both as outputs or both as inputs
 - Avoid mixed directions (one input and one output)
- If mixed directions are required:
 - Add 15 kΩ pull-down to VSS on the output node only.
 - GPIO242PB1 (output) + GPIO242NB1 (input): Pull-down on GPIO242PB1
 - GPIO242PB1 (input) + GPIO242NB1 (output): Pull-down on GPIO242NB1
- When adding 15 kΩ pull-down, ensure that no additional external or internal pull-up resistor has been added to the signal. The user must ensure that with the pull-down resistor the signal integrity of the signal has been maintained.
- No pull-down needed if both are inputs or both are outputs.

Note: Transceiver and JTAG pins do not support the cold sparing feature.

1.4.2. Hot Socketing (GPIO Only) [\(Ask a Question\)](#)

Hot socketing (also known as hot swapping or hot plug-in) prevents damage to the RT PolarFire® SoC FPGA if, at any time, voltage is detected at I/O while the device is powered off. It also helps prevent disruptions that may occur in the rest of the system if the I/Os of a device are connected without a valid power supply.

Only GPIOs support hot socketing. In hot socketing, GPIOs are in high-impedance (hi-Z) state.

The GPIO maintains the following high-impedance state until the power supplies are at a valid state.

- VDDAUX is greater than or equal to 1.6V.
- VDDIX is greater than or equal to 0.8V.
- VDD and VDD25 are both high and the RT PolarFire SoC FPGA controller has asserted the global I/O ring signal (IO_EN).

Note: TMS, TDI, TRSTB, DEVRST_N and FF_EXIT_N do not support hot socketing.

1.4.2.1. Overvoltage Tolerance for GPIO [\(Ask a Question\)](#)

If the GPIO is configured with the following settings, the GPIO supports overvoltage tolerance, ensuring that the I/O signal at the pad is at a higher potential than the VDDIX power supply.

Table 1-8. Overvoltage Tolerance

Standard	OE	Clamp Diode	VREF (Input)	Weak Pull-Up/Pull-Down	Termination	Hot-plug
PCI	x	ON	ON	ON	ON	Disabled
GPIO	1	ON	ON	ON	ON	Disabled
	0	OFF	OFF	OFF	OFF	Enabled

For recommended operating conditions about overvoltage tolerance, see [RT PolarFire SoC Datasheet](#).

1.5. MSS I/Os [\(Ask a Question\)](#)

RT PolarFire® SoC FPGAs support the following types of MSS I/O buffers:

- [MSS DDR I/Os](#)
- [MSS SGMII I/Os](#)
- [MSS-Specific I/O](#)

1.5.1. MSS DDR I/Os [\(Ask a Question\)](#)

The MSS DDR I/Os are a dedicated set of pins for x32 width DDR interface with ECC support. The dedicated set of pins are as follows:

- MSS_DDR_DQ[0:35]
- MSS_DDR_DQSP[0:4], MSS_DDR_DQSN[0:4]
- MSS_DDR_DM[0:4]
- MSS_DDR_A[0:16]
- MSS_DDR_CK_0, MSS_DDR_CK_N0
- MSS_DDR_CK_1, MSS_DDR_CK_N1
- MSS_DDR_RAM_RST_N
- MSS_DDR_VREF_IN
- MSS_DDR_BA0, MSS_DDR_BA1
- MSS_DDR_BG0, MSS_DDR_BG1
- MSS_DDR_CS0, MSS_DDR_CS1
- MSS_DDR_CKE0, MSS_DDR_CKE1
- MSS_DDR_ODT0, MSS_DDR_ODT1
- MSS_DDR_ACT_N
- MSS_DDR_WE_N

- MSS_DDR_ALERT_N
- MSS_DDR_PARITY

The interface supports the following types of DDR memories:

- DDR4 – Single and Dual Rank
- DDR3 – Single and Dual Rank
- LPDDR4
- LPDDR3

For more details about pin mapping and DDR user models, see *RT PolarFire SoC Packaging Pin Assignment Table (PPAT)* and [PolarFire Family Memory Controller User Guide](#).

1.5.2. MSS SGMII I/Os [\(Ask a Question\)](#)

The MSS SGMII I/Os are a dedicated set of pins. Two sets of pins are for the transceiver and one set for sourcing the reference clock. The MSS SGMII pins are listed as follows:

- MSS_SGMII_TXP0, MSS_SGMII_TXN0
- MSS_SGMII_RXP0, MSS_SGMII_RXN0
- MSS_SGMII_TXP1, MSS_SGMII_TXN1
- MSS_SGMII_RXP1, MSS_SGMII_RXN1
- MSS_REFCLK_IN_P, MSS_REFCLK_IN_N

1.5.3. MSS-Specific I/O [\(Ask a Question\)](#)

There are 38 MSS I/Os that can be configured using Libero® SoC to interface with various peripherals (see [Figure 1-6](#)). For the MSS I/Os pinout information, see [PolarFire SoC Packaging Pin Assignment Table](#). The PPAT lists the MSS I/Os and the peripherals they support. MSS I/Os are configured using Libero SoC > PFSOC_MSS SgCore IP Configurator.

Figure 1-6. Peripherals

BANK	IO MUX	Package Pin	EMMC	USB	SD	MAC	QSPI	SPI	MMUART	I2C	CAN	GPIO	
BANK 4	0	AE3	EMMC_CLK		SD_CLK		QSPI_CLK	SPI_0_CLK				GPIO_0_0	
	1	AE4	EMMC_CMD		SD_CMD				MMUART_3_RXD	I2C_0_SCL		GPIO_0_1	
	2	AE11	EMMC_DATA0		SD_DATA0				MMUART_3_TXD	I2C_0_SDA		GPIO_0_2	
	3	AE9	EMMC_DATA1		SD_DATA1				MMUART_4_RXD		CAN_0_TXBUS	GPIO_0_3	
	4	AF4	EMMC_DATA2		SD_DATA2				MMUART_4_TXD		CAN_0_RXBUS	GPIO_0_4	
	5	AG1	EMMC_DATA3		SD_DATA3				MMUART_0_RXD (A)		CAN_0_TX_EBL_N	GPIO_0_5	
	6	AE8	EMMC_STRB		SD_CD				MMUART_0_TXD (A)			GPIO_0_6	
	7	AE7	EMMC_RSTN		SD_WP	MAC_1_MDC			MMUART_2_RXD	I2C_1_SCL		GPIO_0_7	
	8	AF3	EMMC_DATA4		SD_POW	MAC_1_MDIO	QSPI_SS0		MMUART_2_TXD	I2C_1_SDA		GPIO_0_8	
	9	AF1	EMMC_DATA5		SD_VOLT_SEL	MAC_0_MDC	QSPI_DATA0		MMUART_0_RXD (B)			GPIO_0_9	
	10	AD11	EMMC_DATA6		SD_VOLT_EN	MAC_0_MDIO	QSPI_DATA1		MMUART_0_TXD (B)			GPIO_0_10	
	11	AE6	EMMC_DATA7		SD_VOLT_CMD_DIR		QSPI_DATA2	SPI_0_DO	MMUART_1_RXD		CAN_1_TXBUS	GPIO_0_11	
	12	AE2			SD_VOLT_DIR_0		QSPI_DATA3	SPI_0_DI	MMUART_1_TXD		CAN_1_RXBUS	GPIO_0_12	
	13	AE1			SD_VOLT_DIR_1_3			SPI_0_SS0			CAN_1_TX_EBL_N	GPIO_0_13	
BANK 2	14	AD5		USB_CLK			QSPI_CLK (A)	SPI_1_CLK (A)				GPIO_1_0	
	15	AD6		USB_DIR		MAC_1_MDC (A)		SPI_1_DO (A)	MMUART_4_RXD			GPIO_1_1	
	16	AD9		USB_NXT		MAC_1_MDIO (A)		SPI_1_DI (A)	MMUART_4_TXD			GPIO_1_2	
	17	AD7		USB_STP				SPI_1_SS0 (A)	MMUART_0_RXD (A)			GPIO_1_3	
	18	AD4		USB_DATA0					MMUART_0_TXD (A)			GPIO_1_4	
	19	AD2		USB_DATA1					MMUART_1_RXD			GPIO_1_5	
	20	AD10		USB_DATA2					MMUART_1_TXD	I2C_0_SCL (A)		GPIO_1_6	
	21	AC9		USB_DATA3					MMUART_2_RXD	I2C_0_SDA (A)	CAN_0_TX_EBL_N (A)	GPIO_1_7	
	22	AC4		USB_DATA4					MMUART_2_TXD		CAN_0_TXBUS (A)	GPIO_1_8	
	23	AC10		USB_DATA5				SPI_0_SS0	MMUART_3_RXD		CAN_0_RXBUS (A)	GPIO_1_9	
	24	AD1		USB_DATA6			MAC_0_MDC (A)	SPI_0_DI	MMUART_3_TXD	I2C_1_SCL (A)		GPIO_1_10	
	25	AC7		USB_DATA7			MAC_0_MDIO (A)		SPI_0_DO	I2C_1_SDA (A)		GPIO_1_11	
	26	AC5			SD_LED (A)					I2C_1_SCL (B)		GPIO_1_12	
	27	AB2			SD_VOLT_0 (A)					I2C_1_SDA (B)	CAN_1_TX_EBL_N (A)	GPIO_1_13	
	28	AB10			SD_VOLT_1 (A)	MAC_1_MDC (B)			MMUART_0_RXD (B)		CAN_1_TXBUS (A)	GPIO_1_14	
	29	AC8			SD_VOLT_2 (A)	MAC_1_MDIO (B)			MMUART_0_TXD (B)		CAN_1_RXBUS (A)	GPIO_1_15	
	30	AB5						QSPI_CLK (B)	SPI_1_CLK (B)				GPIO_1_16
	31	AC3						QSPI_SS0	SPI_1_SS0 (B)			CAN_0_TXBUS (B)	GPIO_1_17
	32	AB8			SD_CLE			QSPI_DATA0	SPI_1_DO (B)			CAN_0_RXBUS (B)	GPIO_1_18
	33	AB6			SD_LED (B)			QSPI_DATA1	SPI_1_DI (B)			CAN_0_TX_EBL_N (B)	GPIO_1_19
34	AB3			SD_VOLT_0 (B)			QSPI_DATA2				CAN_1_TXBUS (B)	GPIO_1_20	
35	AB11			SD_VOLT_1 (B)	MAC_0_MDC (B)	QSPI_DATA3		MMUART_0_RXD (C)	I2C_0_SCL (B)	CAN_1_RXBUS (B)	GPIO_1_21		
36	AC2			SD_VOLT_2 (B)	MAC_0_MDIO (B)			MMUART_0_TXD (C)	I2C_0_SDA (B)	CAN_1_TX_EBL_N (B)	GPIO_1_22		
37	AB7						QSPI_CLK (C)	SPI_0_CLK				GPIO_1_23	

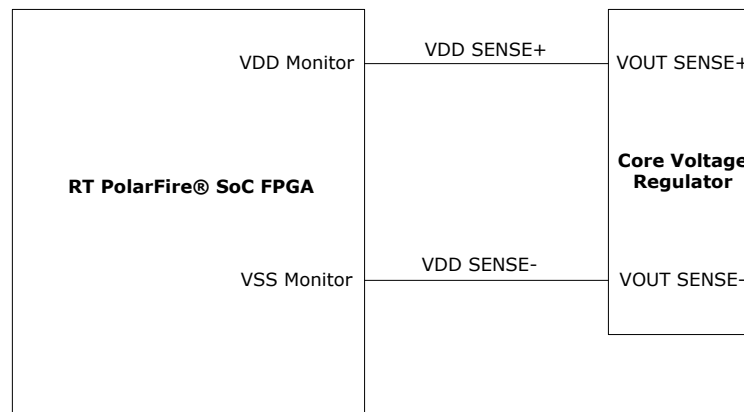
1.6. Voltage Monitor Detector I/Os [\(Ask a Question\)](#)

RT PolarFire® SoC FPGAs integrate numerous on-chip tamper detectors, enabling users to monitor the environment and the operating parameters of the design. Voltage monitor detectors are one of the Tamper flags, which indicate that a tamper event has occurred. These Tamper flags are available as signals to the FPGA fabric for users to process and respond.

The following two types of Voltage Monitor Detector I/O pins are shown in the following figure.

- VDD Monitor
- VSS Monitor

Figure 1-7. Voltage Monitor Pins for SENSE Operation



These two pins are used to connect SENSE+ and SENSE- of the silicon core voltage power regulator to sense the core voltage at silicon. These pins are connected directly to the VDD and VSS supply planes on the die. This differential pair provides the best measurement points for the voltage of the silicon die and the best point to connect to the remote sense pins on DC-DC power converters. Using a power supply with a differential remote sense input is the best practice to ensure proper Internal Resistance (IR) voltage compensation within the device and package.

Ensure that these traces are isolated from fast switching signals and high current paths on the final PCB layout, because these traces can add differential-mode noise.

➔ Important: Remote sensing is required for the RTPFS460ZT-CG1509 device to meet all device performance specifications. For more information about pin outs, see the [Packaging Pin Assignment Table \(PPAT\)](#).

1.7. Clocks [\(Ask a Question\)](#)

RT PolarFire® SoC devices offer two on-chip RC oscillators (2 MHz and 160 MHz) to generate free-running clocks. The clocks do not have any I/O pads and do not require external components to operate.

The following table lists the number of RC oscillators available in RT PolarFire SoC devices.

Table 1-9. RC Oscillator Count

Resource	Supported Range (MHz)	RTPFS160ZT	RTPFS460ZT
On-chip RC oscillator	2	1	1
	160	1	1

You must understand the regional clock implications when targeting designs that might be migrated to different device sizes. It is important that you go through the pin planning before finalizing it on the board while targeting a die. For more information about clocking in PolarFire devices, see [PolarFire Family Clocking Resources User Guide](#).

For more information about the preferred clock inputs connectivity to PLLs, DLLs and the global clock network, see the Packaging Pin Assignment Table (PPAT) on the [RT PolarFire SoC](#) web page.

1.8. Reset [\(Ask a Question\)](#)

For designing a robust system, users may use the dedicated DEVRST_N pin or a general-purpose reset signal, using any GPIO/HSIO as a global system level reset.

For the following cases, the users must use the DEVRST_N as a warm reset for the device:

- A user design modifies auto-initialized fabric RAMs or PCIe configuration during operation.
 - A user design is using PCIe, transceivers or user crypto.
- For all other use cases, it is recommended to use a general-purpose reset signal using any GPIO/HSIO I/O because they take much shorter time for the design to come out of reset.

If the dedicated DEVRST_N is not used for warm resets, the DEVRST_N pin must be configured using one of the following methods:

- Drive the signal with a POR chip or an external device and keep the DEVRST_N asserted till the system/clocks are stable and the chip is properly powered up.
- Connect DEVRST_N to VDDI3 through a 1 kΩ resistor per pin without sharing with any other pins.
 - In this case, the user needs to ensure that all clocks are stable going to the device before the user design is released from power-on reset. The details of the minimum time taken for the fabric design to be activated after power-on is specified in the Power-Up To Functional section of [RT PolarFire SoC Datasheet](#).

1.9. DDR Interface Requirements [\(Ask a Question\)](#)

RT PolarFire SoC devices support DDR3, LPDDR4, LPDDR3 and DDR4. For complete DDR support details, see the [RT PolarFire SoC Datasheet](#).

DDR interface reliability demands impeccable signal layout and power plane design. You must strictly follow [RT PolarFire SoC Decoupling Capacitors](#), including precise power coupling capacitor selection. For board layout and routing requirements, see the [PolarFire Family Memory Controller User Guide](#). Non-compliance will result in interface failure.

1.10. Device Programming [\(Ask a Question\)](#)

The RT PolarFire[®] SoC device can be programmed using one of the two dedicated interfaces: JTAG or SPI. These two interfaces support the following programming modes:

- JTAG programming
- SPI Initiator mode programming
- SPI Target mode programming

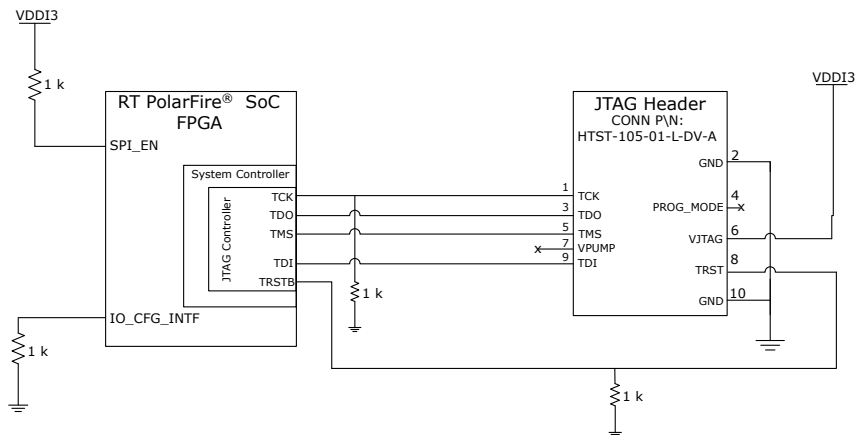
The RT PolarFire SoC FPGA supports programming modes through an internal system controller, using SPI Initiator mode or an external initiator, using JTAG or SPI interfaces. For detailed information on hardware connections for each programming mode, see [PolarFire FPGA and PolarFire SoC FPGA Programming User Guide](#).

1.10.1. JTAG Programming [\(Ask a Question\)](#)

The JTAG interface is used for device programming and testing, or for debugging the firmware. When the device reset (DEVRST_N) is asserted, JTAG I/Os are not accessible. JTAG I/Os are powered by Bank 3 VDDI.

The following figure shows the board-level connectivity for JTAG Programming mode in RT PolarFire[®] SoC devices.

Figure 1-8. JTAG Programming



The following table lists the JTAG pin names and descriptions.

Table 1-10. JTAG Pins

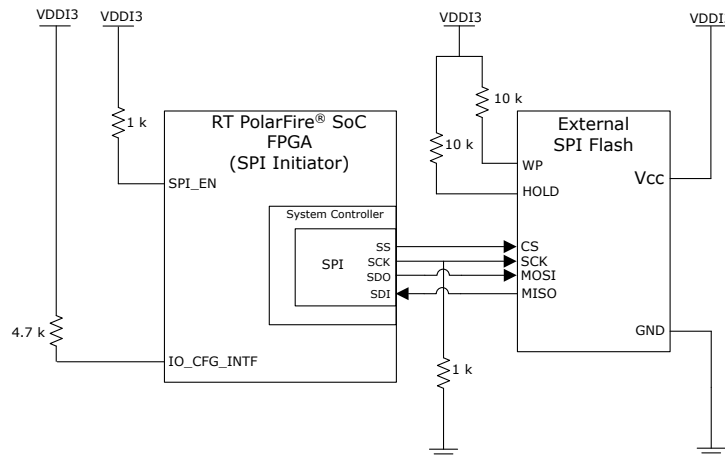
Pin Names	Direction	Unused Condition	Description
TMS	Input	DNC	JTAG test mode select
TRSTB	Input	Must be connected to VDDI3 through a 1 kΩ resistor	JTAG test reset <ul style="list-style-type: none"> If JTAG is not used, an external pull-down resistor can be included to ensure that the TAP is held in Reset mode Must be held low during device operation
TDI	Input	DNC	JTAG test data in
TCK	Input	Must be connected to VSS through a 10 kΩ resistor	JTAG test clock
TDO	Output	DNC	JTAG test data out

1.10.2. SPI Initiator Mode Programming [\(Ask a Question\)](#)

The embedded system controller contains a dedicated SPI block for programming, which can operate in Initiator or Target mode. In Initiator mode, the RT PolarFire® SoC device interfaces are used to download programming data through the external SPI Flash. In Target mode, the SPI block communicates with a remote device that initiates download of programming data to the device.

The following figure shows the board-level connectivity for SPI Initiator mode programming in RT PolarFire SoC devices.

Figure 1-9. SPI Initiator Mode Programming



The following table lists the SPI initiator mode programming pins.

Table 1-11. SPI Initiator Mode Programming Pins

SPI Pin Name	Direction	Unused Condition	Description
SCK	Bidirectional	Connect to VSS through a 10 kΩ resistor	SPI clock ¹
SS	Bidirectional	Connect to VSS through a 10 kΩ resistor	SPI target select ¹
SDI	Input	Connect to VDDI3 through a 10 kΩ resistor	SDI input ¹
SDO	Output	DNC	SDO output ¹
SPI_EN	Input	Connect to VSS through a 10 kΩ resistor	SPI enable: <ul style="list-style-type: none"> • 0: SPI output tri-stated • 1: Enabled • Pulled up or down through a resistor or driven dynamically from an external source to enable or tri-state the SPI I/O
IO_CFG_INTF	Input	Connect to VSS through a 10 kΩ resistor	SPI I/O configuration: <ul style="list-style-type: none"> • 0: SPI target interface • 1: SPI initiator interface • Pulled up or down through a resistor or driven dynamically from an external source to indicate whether the shared SPI is a Initiator or Target

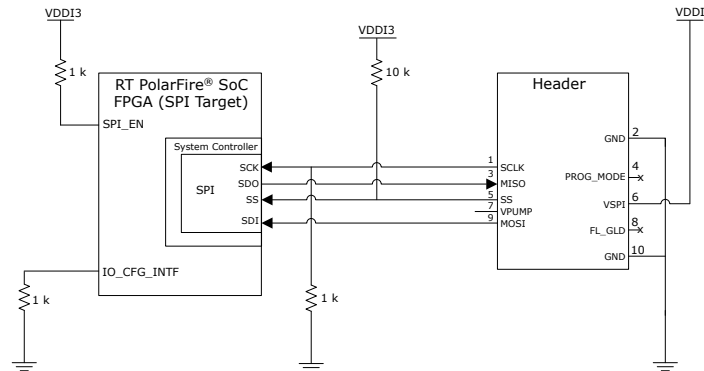
Note:

1. The SCK, SS, SDI and SDO pins are shared between the system controller and the FPGA fabric. When the system controller’s SPI is enabled and configured as a initiator, the system controller hands over the control of the SPI to the fabric (after device power-up).

1.10.3. SPI Target Mode Programming [\(Ask a Question\)](#)

The following figure shows the board-level connectivity for SPI Target mode programming in RT PolarFire® SoC devices.

Figure 1-10. SPI Target Mode Programming



1.10.4. Special Pins [\(Ask a Question\)](#)

For information about special pins, see [RT PolarFire SoC FPGA Packaging and Pin Descriptions User Guide](#).

1.11. Transceiver [\(Ask a Question\)](#)

The following table lists the transceiver features supported in RT PolarFire® SoC devices. The transceiver blocks are located on the east corner of the device. RT PolarFire SoC devices support PCIe interface only on Transceiver quad 0.

For more information about implementing PCIe interfaces, see [PolarFire Family PCI Express User Guide](#). For more information about implementing other transceiver-based interfaces and power supplies, see [PolarFire Family Transceiver User Guide](#).

The following table lists the number of transceivers supported in RT PolarFire SoC devices.

Table 1-12. Transceiver Support in RT PolarFire Devices

Device	Transceiver Lanes
RTPFS160ZT	8
RTPFS460ZT	20

1.11.1. Reference Clock [\(Ask a Question\)](#)

A transceiver reference clock is delivered to each transmit PLL for transmit functions and to each receiver lane for receive Clock Data Recovery (CDR).

1.11.1.1. Transceiver Reference Clock Requirements [\(Ask a Question\)](#)

The following are requirements for the transceiver reference clock:

- When differential clock input is provided to the reference clock:
 - ODT must be enabled for transceiver reference clock pins
 - It must be within the range of 20 MHz to 400 MHz
- It must be within the tolerance range of I/O standards. The reference input buffer is provided and is expected to support these input standards directly without external components on the board. The reference I/O standards such as LVCMOS25, SSTL18, LVDS25 and HCSL25 are supported. For more information, see the “Reference Clock Input Buffer Standards” table in [PolarFire Family Transceiver User Guide](#).

For detailed PHY specifications, see the *PCI Express Base specification Rev 2.1* and the *PCIe Add-in Card Electro-Mechanical (CEM) Specifications*.

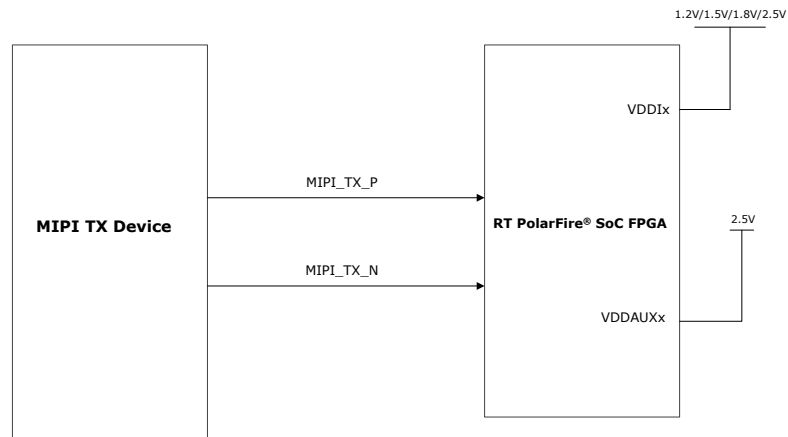
1.12. MIPI Hardware Design Guidelines [\(Ask a Question\)](#)

The following sections discuss the guidelines for MIPI RX and TX interface with RT PolarFire® SoC device.

1.12.1. MIPI RX [\(Ask a Question\)](#)

The MIPI RX interface is supported only in GPIO Bank. The corresponding Bank voltage (VDDI and VDDAUX voltage) must be connected as shown in the following figure.

Figure 1-11. MIPI RX Connection



MIPI RX signal connections are as follows:

- Four data and clock must be within one DDR_Lane.
- The data signals must be connected to adjacent DDR_Lanes, if more than four data signals are available.
- The MIPI RX clock must be connected to a CLKIN pin.

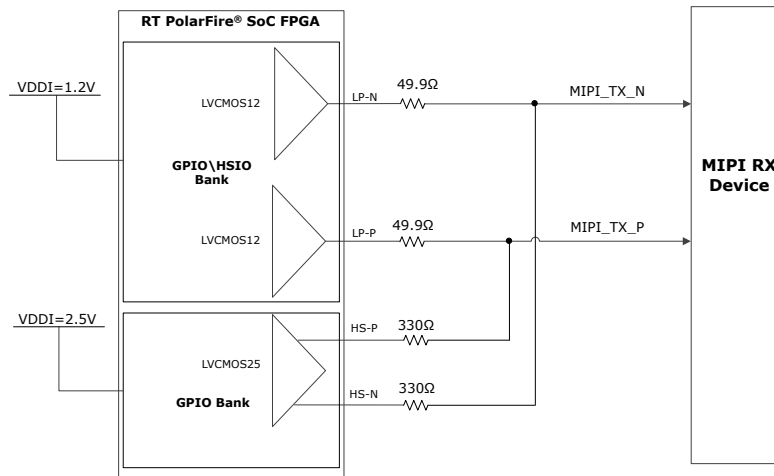
For more information about DDR_Lane, see [RT PolarFire SoC Packaging Pin Assignment Table](#).

1.12.2. MIPI TX [\(Ask a Question\)](#)

The MIPI Low-Power (LP) signals should be connected to a 1.2V GPIO/HSIO Bank supply. High-Speed (HS) signals should be connected to a 2.5V GPIO Bank supply. Select the HS and LP pins in adjacent pins to minimize the LP stub. The HS data and clock signals should be in one DDR_Lane. For more information about DDR_Lane, see [RT PolarFire SoC Packaging Pin Assignment Table](#).

The MIPI TX standard can be implemented by using the resistor divider network for LP and HS signals, as shown in the following figure. The resistor values mentioned in the following figure provide a throughput of up to 1 Gbps.

Figure 1-12. MIPI TX Connections



➔ Important: Run the PDC verification in the Libero® SoC tool before moving to layout. To know about MIPI RX electrical characteristics, see [RT PolarFire SoC Datasheet](#).

For information about the MIPI layout guidelines, see [MIPI](#).

1.13. AC and DC Coupling [\(Ask a Question\)](#)

Each transmit channel of a PCIe lane must be AC-coupled to allow link detection. Capacitors used for AC coupling must be external to the device and large enough to avoid excessive low-frequency drops, when the data signal contains a long string of consecutive identical bits. For non-PCIe applications, Microchip recommends that an RT PolarFire SoC device receives inputs that are AC-coupled to prevent common-mode mismatches between devices. Suitable values (for example, 0.1 μ F) for AC-coupling capacitors must be used to maximize link signal quality and must conform to [RT PolarFire SoC Datasheet](#) electrical specifications.

For lower data rates, as per the datasheet, DC coupling is supported by RT PolarFire SoC Transceiver TX and RX interfaces through a configuration option. If an RT PolarFire SoC transmitter is used to drive an RT PolarFire SoC receiver in DC-coupled mode, select the lowest common mode settings for the transmitter.

1.14. Brownout Detection [\(Ask a Question\)](#)

The RT PolarFire® SoC FPGA functionality is guaranteed only if VDD is above the recommended level specified in the datasheet. Brownout occurs when VDD drops below the minimum recommended operating voltage. When this occurs, the device operation may not be reliable. The design might continue to malfunction even after the supply is brought back to the recommended values because parts of the device might have lost functionality during brownout.

➔ Important: For brownout detection on any RT PolarFire SoC supply (including VDD, VDD18 and VDD25), use external brownout detection circuits.

2. Board Design Checklist [\(Ask a Question\)](#)

The following sections provide a set of hardware board design checks for designing hardware using Microchip RT PolarFire® SoC FPGAs. The checklists provided in [Design Checklist](#) and [Layout Checklist](#) sections are a high-level summary checklist to assist the design engineers in the design process.

2.1. Prerequisites [\(Ask a Question\)](#)

Ensure that you have gone through the following sections before reading the checklists:

- [Designing the Board](#)
- [General Layout Design Practices](#)

The following checklists are intended as a guideline only. The RT PolarFire® SoC family consists of SoC FPGAs with 160K and 460K Logic Elements (LEs).

2.2. Design Checklist [\(Ask a Question\)](#)

The following table lists the various checks that design engineers must consider while designing the system.

Table 2-1. Design Checklist

Guideline	Yes/No	Remarks
Prerequisites		
<ul style="list-style-type: none"> • See RT PolarFire SoC Datasheet • See RT PolarFire SoC FPGA Packaging and Pin Descriptions User Guide • See CG1509 Package Pin Assignment Table 		
See the board-level schematics of <i>RT PolarFire® SoC Development Kit</i> .		
Device Selection		
<ul style="list-style-type: none"> • Check for available device variants for RT PolarFire SoC FPGA. • Select a device based on I/O pin count, transceivers, package, Phase-Locked Loops (PLLs) and speed grade. 		
Check device errata in the RT PolarFire SoC FPGA Errata .		
Design Checklist		
Power Analysis		
Download the PolarFire and PolarFire SoC FPGA Power Estimator User Guide and check for the power budget.		
Power Supply Checklist		
For information about used power rails, see Power Supplies .		
Decoupling Capacitors		
Strictly implement the RT PolarFire SoC Decoupling Capacitors as specified in RT PolarFire SoC Decoupling Capacitors . Device performance and adherence to datasheet specifications depend entirely on these requirements being met without exception.		
Any deviation from the specified capacitors requires Power Integrity (PI) analysis.		
Clocks		
For more information about dynamic phase shift ports, see Table 4-4 of PolarFire Family Clocking Resources User Guide . The XCVR reference clock ranges from 20 MHz to 400 MHz.		

Table 2-1. Design Checklist (continued)

Guideline	Yes/No	Remarks
<p>The global clock network can be driven by any of the following:</p> <ul style="list-style-type: none"> Preferred clock inputs (CLKIN_z_w) On-chip oscillators CCC (PLL/DLL) XCVR interface clocks <p>For information about the preferred clock inputs connectivity to PLLs, DLLs and the global clock network, see the Packaging Pin Assignment Table (PPAT) on the RT PolarFire SoC documentation web page.</p> <p>High-Speed I/O Clocks</p> <p>High-speed I/O clock networks can be driven by I/O or CCCs. The high-speed I/O clocks can feed reference clock inputs of adjacent CCCs through hardwired connections.</p> <p>CCC</p> <p>The CCC can be configured to have a PLL or DLL clock output, driving a high-speed I/O clock network.</p>		
<p>Global Buffer (GB) can be driven through the dedicated global I/O, CCC or fabric (regular I/O) routing. The global network is composed of GBs to distribute low-skew clock signals or high-fanout nets.</p> <p>Dedicated global I/O drives the GBs directly and are the primary source for connecting external clock inputs (to minimize the delay) to the internal global clock network.</p> <p>For more information about the global clock network, see PolarFire Family Clocking Resources User Guide.</p>		
<p>Reset</p> <p>For more information about DEVRST_N and user reset, see Reset.</p>		
<p>DDR Interface</p> <p>For more information about DDR routing and topology, see PolarFire Family Memory Controller User Guide.</p>		
<p>Programming and Debugging Scheme</p> <p>For programming and debugging information, see Device Programming.</p>		
<p>XCVR</p> <p>For more information about XCVR, see PolarFire Family Transceiver User Guide.</p> <p>For I/O gearing interfaces, place the clocks and data based on the defined requirements, by selecting the correct I/O. For more information about the placement of User I/O, see PolarFire Family I/O User Guide.</p> <p>There is one IO_CFG_INTF pin available, which can be used as input.</p> <p>See the bank location diagrams in the RT PolarFire SoC FPGA Packaging and Pin Descriptions User Guide to assess the preliminary placement of major components on PCB.</p>		

2.3. Layout Checklist [\(Ask a Question\)](#)

The following table lists the layout checklist.

Table 2-2. Layout Checklist

Guideline	Yes/No
Power	
Are the 0402 or lesser size capacitors used for all decoupling capacitors?	
Is the required copper shape provided to core voltage?	
Are the required copper shape and sufficient vias provided to voltages?	

Table 2-2. Layout Checklist (continued)

Guideline	Yes/No
Are VREF planes for the DDRx reference supply isolated from the noisy planes?	
Are sufficient number of decoupling capacitors used for the DDRx core and VTT supply?	
Is one 0.1 μ F capacitor for two VTT termination resistors used for DDRx?	
Is the VTT plane width sufficient?	
DDR Memories	
Is the length-match recommended by the DDR manufacturer followed for DDR memories?	
Are the traces with the correct controlled impedance required for DDR memories?	
XCVR	
Are the length-match recommendations for XCVR followed?	
Are DC blocking capacitors required for the PCIe [®] interface?	
Is tight-controlled impedance maintained along the XCVR traces?	
Are differential vias well designed to match XCVR trace impedance?	
Are DC blocking capacitor pads designed to match XCVR trace impedance?	
Dielectric Material	
Is proper PCB material selected for critical layers?	

3. General Layout Design Practices [\(Ask a Question\)](#)

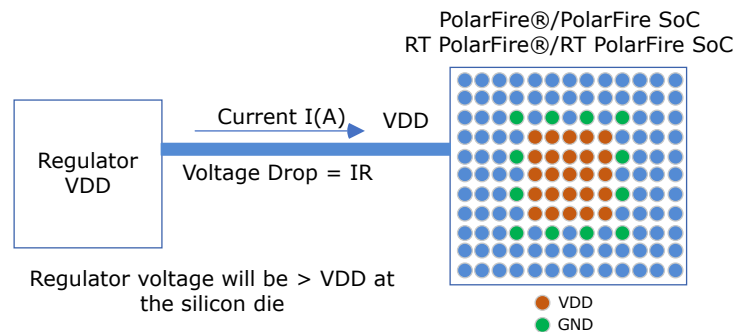
This section provides guidelines for the hardware board layout that incorporates RT PolarFire® SoC devices. Good board layout practices are essential to achieve the expected performance from PCBs and RT PolarFire SoC devices. They help achieve high-quality and reliable results such as low-noise levels, signal integrity, impedance and power requirements. The guidelines mentioned in this document act as a supplement to the standard board-level layout practices.

This section is intended for readers who are familiar with the RT PolarFire SoC FPGA chip, experienced in digital board layout and know about line theory and signal integrity.

3.1. Powering Core VDD [\(Ask a Question\)](#)

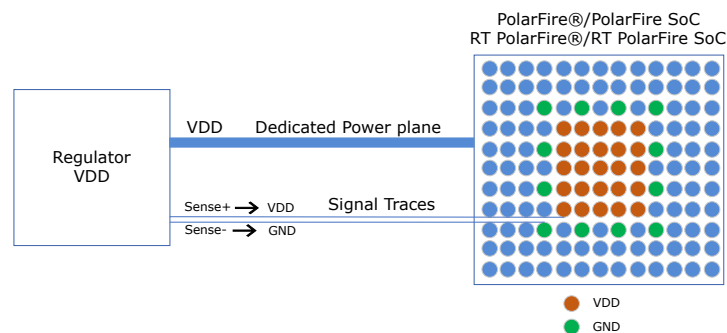
The PolarFire product family requires the VDD to meet a tight tolerant specification for min/max, per the datasheet. To ensure this is designed correctly, users can use standard regulators placed very close to the device, with good layout practices, so the IR drop of the VDD power rail is very minimal. If the regulator is kept further away and a higher IR drop is suspected (especially with high current consumption), it is a good practice to use a regulator which supports closed loop compensation with sense line detectors to power the VDD. This allows the regulator to compensate for the IR drop being seen by silicon, if the current consumption is high.

Figure 3-1. Powering VDD with Standard Regulator



If the regulator is kept further away, the sense lines from the silicon can be fed back to the regulator to compensate for the IR drop by the regulator. This is done by regulators which support closed loop compensation and remote sensing. In this design, the sense lines need to be routed as signal traces back to the regulator. They can be routed as loosely coupled differential transmission lines.

Figure 3-2. Powering VDD with Regulator Supporting Closed Loop Compensation with Remote Sensing

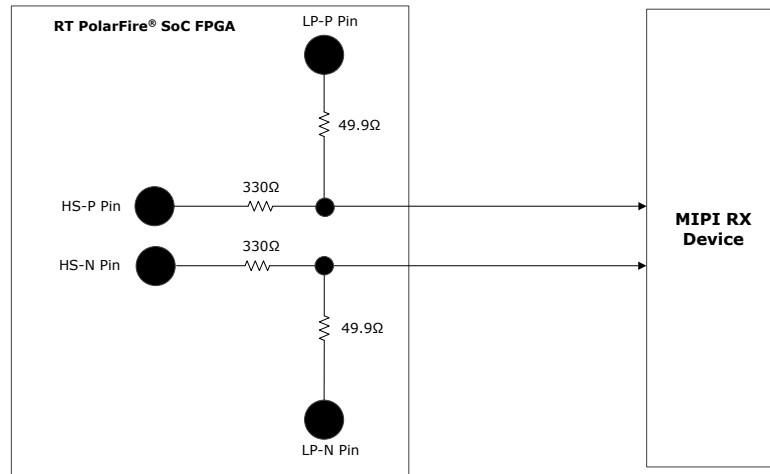


Note: Always follow the sense line recommendations from the VRM vendors.

3.2. MIPI [\(Ask a Question\)](#)

- MIPI RX Layout Guidelines: The data and clock must be matched within 20 mils in the PCB.
- MIPI TX Layout Guidelines: As shown in the following figure, the LP and HS resistors must be close to the RT PolarFire® SoC device pin. The HS signals should be routed to the LP resistors to minimize the LP signals PCB stub length. The LP signals stub should be less than 500 mils. The data lane and clock should be length matched within 20 mils. Eight inches are the maximum length supported.

Figure 3-3. MIPI TX Layout



3.3. Transceiver [\(Ask a Question\)](#)

Collateral material of the RT PolarFire® SoC FPGA transceiver makes the system implementation easier for the designer by providing the system solution. Transceivers provide high-speed serial connectivity with built-in, multi-gigabit, multi-protocol transceivers from 250 Mbps to 10.3125 Gbps. For these transceiver-based interfaces, the system designer must be familiar with the industry specifications, transceivers technology or RF/microwave PCB design. However, the PCB design can be evaluated by a knowledgeable high-speed digital PCB designer.

3.3.1. Layout Considerations [\(Ask a Question\)](#)

This section describes differential traces and skew matching, which must be taken care of while designing the PCB layout.

3.3.1.1. Differential Traces [\(Ask a Question\)](#)

A well-designed differential trace must have the following qualities:

- No mismatch in impedance
- Insertion loss and return loss
- Skew within the differential traces

The following points must be considered while routing the high-speed differential traces to meet the previous qualities.

- The traces must be routed with tight length matching (skew) within differential traces. Asymmetry in length causes conversion of differential signals into common mode signals.
- The differential pair must be routed such that the skew within differential pairs is less than 5 mils. The length match must be used by matching techniques.

3.3.1.2. Skew Matching (Ask a Question)

The length of differential lanes must be matched within the TX and RX group. This applies only to specific protocols such as XAUI.

Differential pairs must be routed symmetrically into and out of structures, as shown in [Figure 3-5](#).

The following figure shows the skew matching.

Figure 3-4. Skew Matching

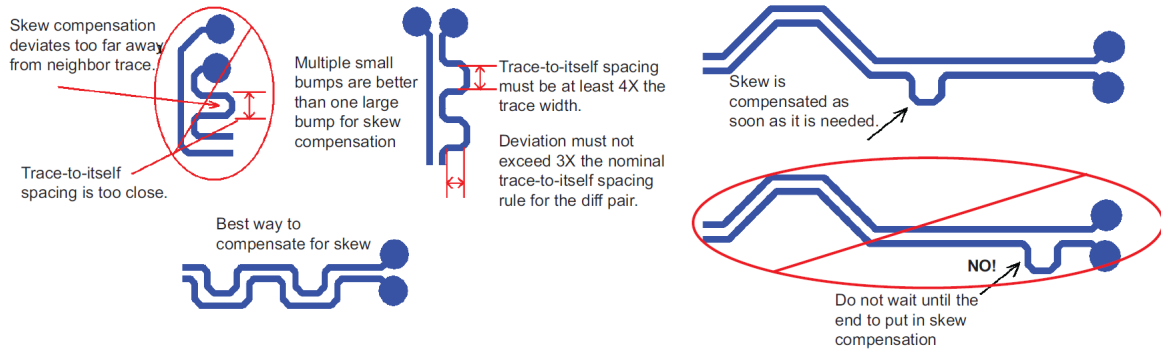


Figure 3-5. Example of Asymmetric and Symmetric Differential Pairs Structure



Skin effect dominates as the speed increases. To reduce the skin effect, the width of the trace must be increased (loosely coupled differential traces). Increase in trace width causes increase in dielectric losses. To minimize dielectric loss, use low Dissipation Factor (DF) PCB materials such as Nelco 4000-13EP SI. The cost of these materials is significantly higher than FR4 PCB material, but FR4 PCB material cannot provide increased eye-opening when longer trace interconnections are required. Ensure that a 85–100Ω differential impedance is maintained. This is an important guideline to be followed if the data rate is 5 Gbps or higher.

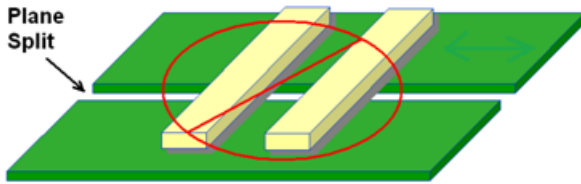
Far end crosstalk is eliminated by using stripline routing. However, this type of routing in stripline causes more dielectric loss. In order to minimize dielectric loss, it is better to route as a microstrip if there is enough space between differential pairs (>4 times the width of the conductor). Simulations are recommended to see the best possible routing.

Instruct the fabrication vendor to use these PCB materials before manufacturing.

Transceiver traces must be kept away from the aggressive nets or clock traces. For example, on RTPF500 devices, the transceiver and DDR traces must not be adjacent to each other. Trace stubs must be avoided.

It is recommended to use low roughness, that is, smooth copper. As the speed increases, insertion loss due to the copper roughness increases. The attenuation due to skin effect is increased in proportion to the square root of frequency. Microchip recommends instructing the PCB fabrication house to use smooth copper, if the frequency exceeds 2 Gbps.

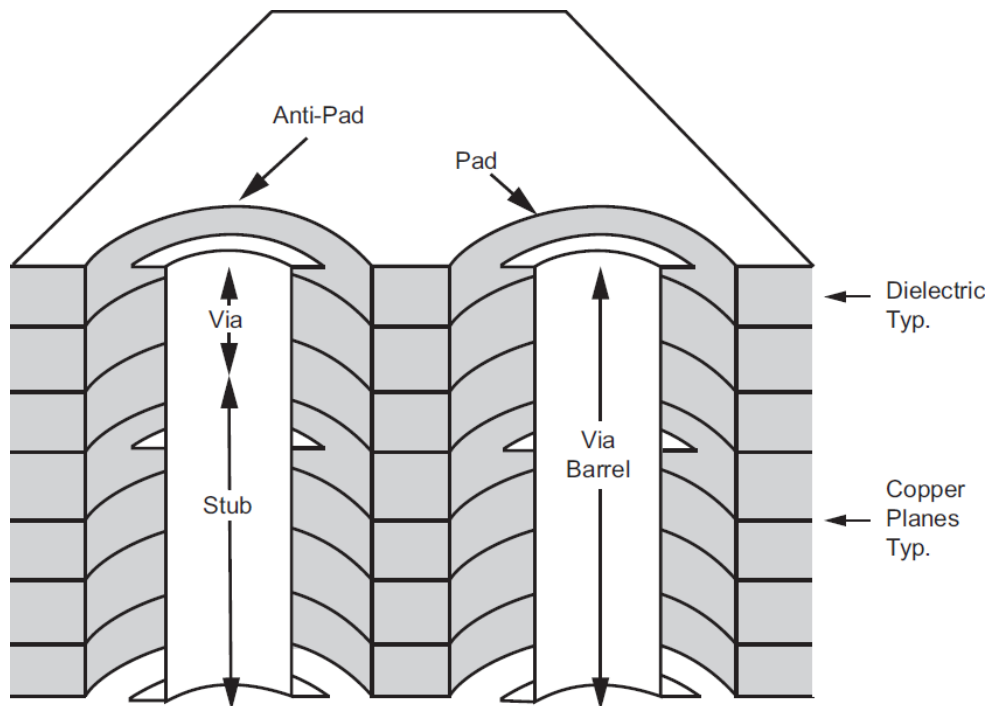
Split reference planes must be avoided. Ground planes must be used for reference for all transceiver lanes.



3.3.1.3. Via [\(Ask a Question\)](#)

The target impedance of vias are designed by adjusting the pad clearance (anti-pad size). Field solver must be used to optimize the via according to the stack-up.

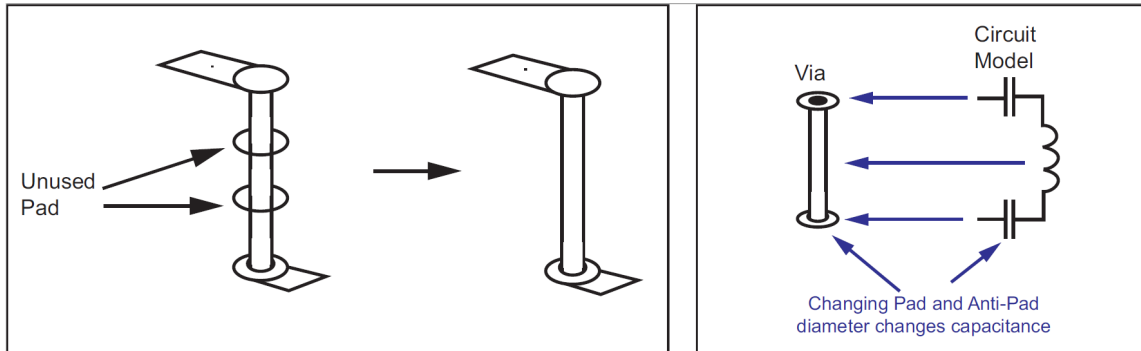
Figure 3-6. Via Illustration



Consider the following points:

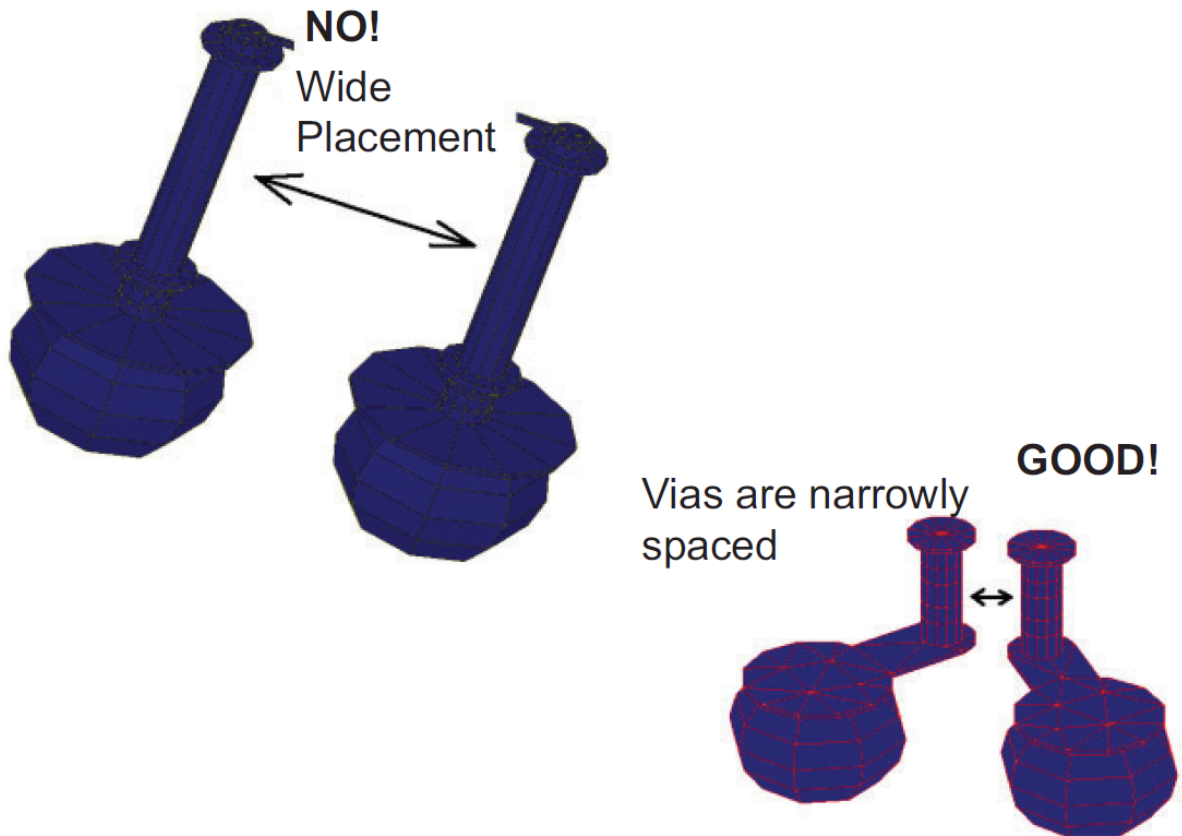
- Many vias on different traces must be avoided or minimized as much as possible.
- The length of via stubs must be minimized by back-drilling the vias, routing signals from the near-top to the near-bottom layer or using blind or buried vias. Using blind-vias and back drilling are good methods to eliminate via stubs and reduce reflections.
- If feasible, non-functional pads must be removed. Non-functional pads on-via are the pads where no trace is connected. This reduces the via capacitance and stub effect of pads.

Figure 3-7. Non-Functional Pads of Via

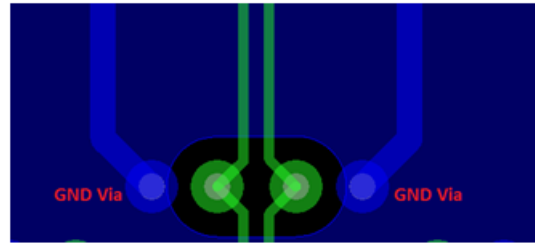


Using tight via-to-via pitches helps in reducing the effect of crosstalk, as shown in the following figure.

Figure 3-8. Via-to-Via Pitch

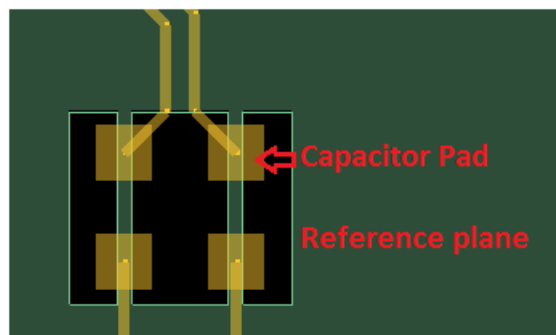


Symmetrical ground vias (return vias) must be used to reduce discontinuity for Common mode signal components, as shown in the following figure. Common mode of part of the signal requires continuous return path for TX and RX to GND. Return vias help maintain the continuity.

Figure 3-9. GND Via or Return Via

3.3.2. DC Blocking Capacitors [\(Ask a Question\)](#)

The plane underneath the pads of the DC blocking capacitors must be removed, as shown in the following figure, to match the impedance of the pad to 50Ω.

Figure 3-10. Capacitor Pad Reference Plane

4. Revision History [\(Ask a Question\)](#)

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

Table 4-1. Revision History

Revision	Date	Description
B	03/2026	<ul style="list-style-type: none"> • The following changes were made in Power Supplies: <ul style="list-style-type: none"> - Updated VDDA, VDD, VDDI5 supply requirement information. - Updated the information on VDD, VDD18, and VDD25 monotonic ramp by clearly stating the monotonic ramp of these power supplies must be followed strictly. See note. • The following changes were made in RT PolarFire SoC Decoupling Capacitors: <ul style="list-style-type: none"> - Updated the introductory paragraph to clearly state that the decoupling capacitors list must be followed strictly. - Updated the information on the guidelines to use alternative decoupling capacitor parts other than listed in Table 1-4. • Added a note in the User I/O section to cross-reference the Cold Sparing section. • Added cold sparing recommendations on GPIOs in Cold Sparing and updated the supply connection of VDDI3 in Figure 1-5. • Updated DDR Interface Requirements. • Updated Table 2-1 in the Design Checklist section for decoupling capacitors. • Updated Table 2-2 in the Layout Checklist section for DDR memory. • Added Powering Core VDD.
A	12/2025	Initial Revision

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ISBN: 979-8-3371-2974-7

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