RTG4™ FPGA

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Introduction (Ask a Question)

RTG4™ FPGAs integrate Microchip's fourth-generation Flash-based FPGA fabric and high-performance interfaces, such as SerDes on a single chip, while maintaining the resistance to radiation-induced configuration upsets in the harshest radiation environments, such as space flight (LEO, MEO, GEO, HEO, and deep space), high-altitude aviation, medical electronics, and nuclear power plant control. The RTG4 family offers up to 151,824 registers, which are hardened by design against radiation-induced SEUs.

Export Control Classification Number (ECCN)

For ECCN, visit the Microchip web page for Export Control Data.

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1. Features and Benefits (Ask a Question)

The following features are supported in RTG4 FPGAs.

1.1. Radiation Tolerance (Ask a Question)

- Configuration memory upsets immunity to LET > 103 MeV.cm^2/mg
- Single-Event Latch-up (SEL) immunity to LET > 103 MeV.cm^2/mg
- SEU-hardened registers eliminate the need for Triple-Module Redundancy (TMR)
  - Immune to Single-Event Upsets (SEU) to LET > 37 MeV.cm^2/mg
  - SEU rate < 10^{-12} errors/bit-day (GEO Solar Min)
- SRAM has a built-in Error Detection And Correction (EDAC)
  - Upset rate < 10^{-11} errors/bit-day (GEO Solar Min)
  - Single Error Correction and Double Error Detection (SECDED)
- Single-Event Transient (SET) upset rate < 10^{-8} errors/bit-day (GEO Solar Min) with optional SET filter
- Total Ionizing Dose (TID) > 100 krad

1.2. High-Performance FPGA (Ask a Question)

- Efficient four-input Look-Up Tables (LUTs) with carry chains for high system performance up to 300 MHz without SET filter
- 209 blocks of dual-port 24.5 Kbits SRAM (Large SRAM) with 250 MHz synchronous performance (512 × 36, 1 Kbit × 18)
- 462 DSP mathblocks with 18-bit × 18-bit input signed multiplication and 44-bit output accumulator
  - High-performance, 300 MHz (without SET filter) across military temperature: –55 °C to 125 °C
- Up to 16 Spacewire clock and data recovery circuitry instances, allowing Spacewire interface up to 200 Mbps

Note: The Spacewire interface protocol is not included but can be implemented in the FPGA fabric.

1.3. High-Speed Serial Interfaces (Ask a Question)

Up to 24 lanes of 3.125 Gbps serialization/deserialization (SerDes) support the following.

- XGXS/XAUI extension (to implement a 10 Gbps XGMII Ethernet PHY interface)
- Native SerDes interface facilitates implementation of Serial RapidIO (SRIO) in FPGA fabric or an SGMII interface to a soft Ethernet MAC
- PCI Express (PCIe) Gen1 hard IP core
  - ×1, ×2, and ×4 lane(s) PCI Express core
  - Up to 2 Kbytes maximum payload size
  - 64-bit/32-bit AXI/AHB initiator and target interfaces to the application layer

1.4. High-Speed Memory Interfaces (Ask a Question)

Up to two high-speed DDR2/DDR3 memory controllers supporting the following.

- DDR2 and DDR3 at 333 MHz (667 Mbps) and LPDDR at 133 MHz (266 Mbps) at the maximum clock rate
- EDAC option with SECDED
- ×9, ×12, ×18, and ×36 bus widths

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1.5. Specifications (Ask a Question)

- 1.2V nominal core voltage
- Single-ended I/Os—LVCMOS 1.2V to 3.3V, LVTTL, and PCI
- Voltage reference I/Os with performance at 600+ Mbps
  – SSTL2, SSTL18, SSTL15, HSTL18, and HSTL15
- True LVDS (600+ Mbps) differential receiver and true current-mode driver, with a built-in termination.
- Clock sources include high-precision 50 MHz embedded RC oscillator
- Eight clock conditioning circuits (CCCs) with PLLs
  – Frequency: Input 10 MHz to 200 MHz and output 0.078 MHz to 425 MHz

The following table lists the peripherals and features of the RTG4.

Table 1-1. RTG4 FPGA Product Family

Peripherals	Features	RT4G150		
	Packages	CG1657/LG1657 **CGG1657/LGG1657**	CQ352/CQG352	FCG1657/FC1657
Logic/DSP	Maximum logic elements (LUT4 + TMR flip-flop)[1]	151,824	151,824	151,824
	Mathblocks (18-bit × 18-bit)	462	462	462
	Radiation-tolerant PLLs	8	8	8
Memory	LSRAM 24.5 Kbits blocks	209	209	209
	µSRAM 1.5 Kbits blocks	210	210	210
	Total SRAM Mbits	5.2	5.2	5.2
	µPROM Kbits	374	374	374
High-Speed Interface	SerDes lanes (4 lanes / SerDes block)	24	4	24
	PCIe endpoints	2	1	2
	DDR SDRAM controllers with ECC	2	0	2
	SpaceWire clock and data recovery circuits	16	4	16
User I/Os	MSIO (3.3V)	240	166	240
	MSIOD (2.5V)	300	0	300
	DDRIO (2.5V)	180	0	180
	Total user I/Os (Non-SerDes)	720	166	720

Note:

1. The maximum number of logic elements varies on the basis of the utilization of DSP and memories in the design.

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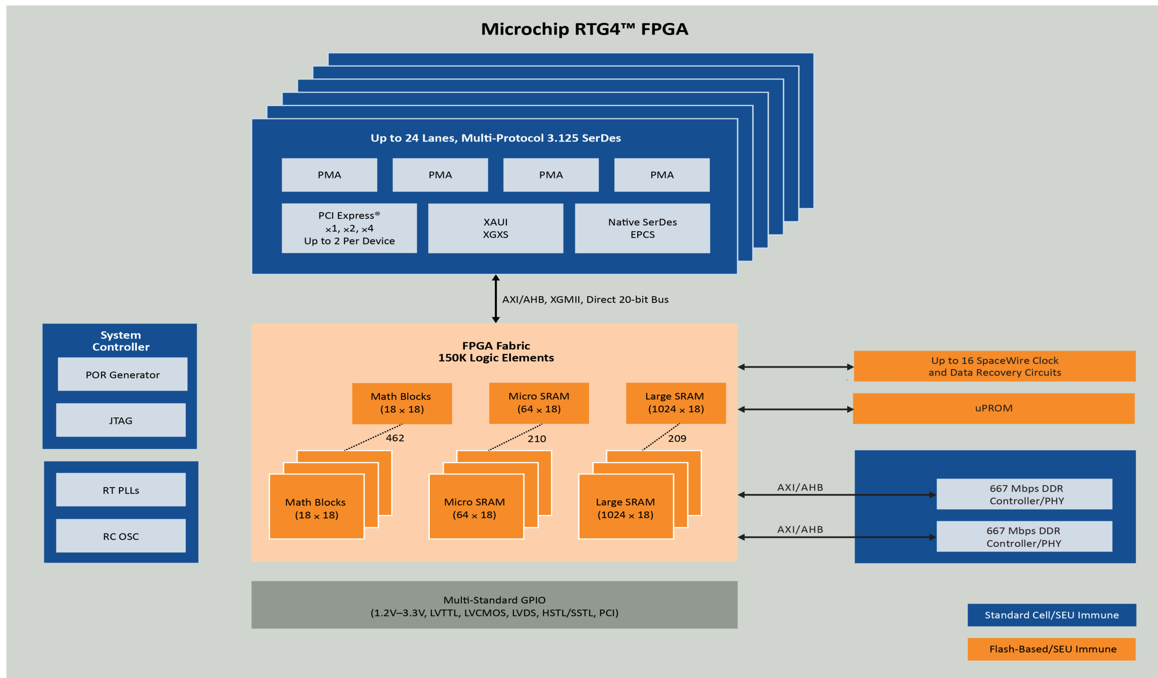
2. RTG4 Device Block Diagram (Ask a Question)

The following figure shows the RTG4 FPGA block diagram.

Figure 2-1. RTG4 Device Block Diagram



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3. RTG4 Ordering Information (Ask a Question)

The following figures show the various ordering codes.

Figure 3-1. Ordering Information for Ceramic Packages

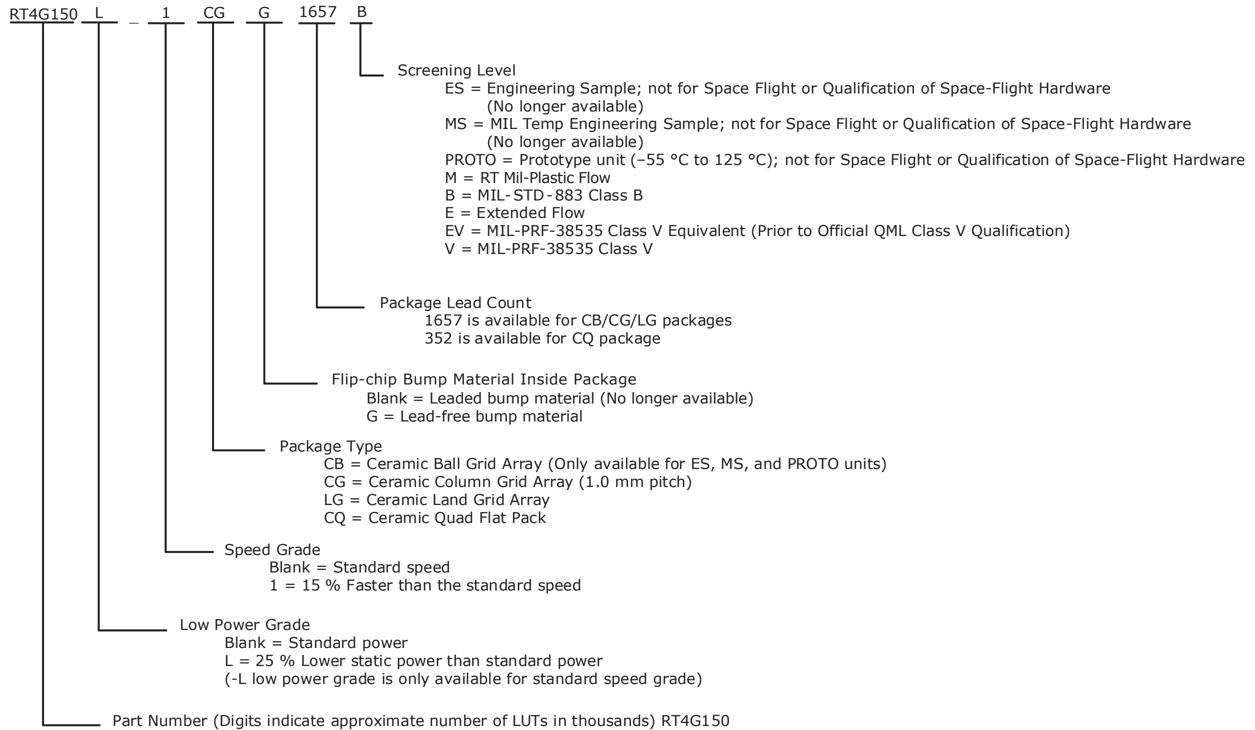
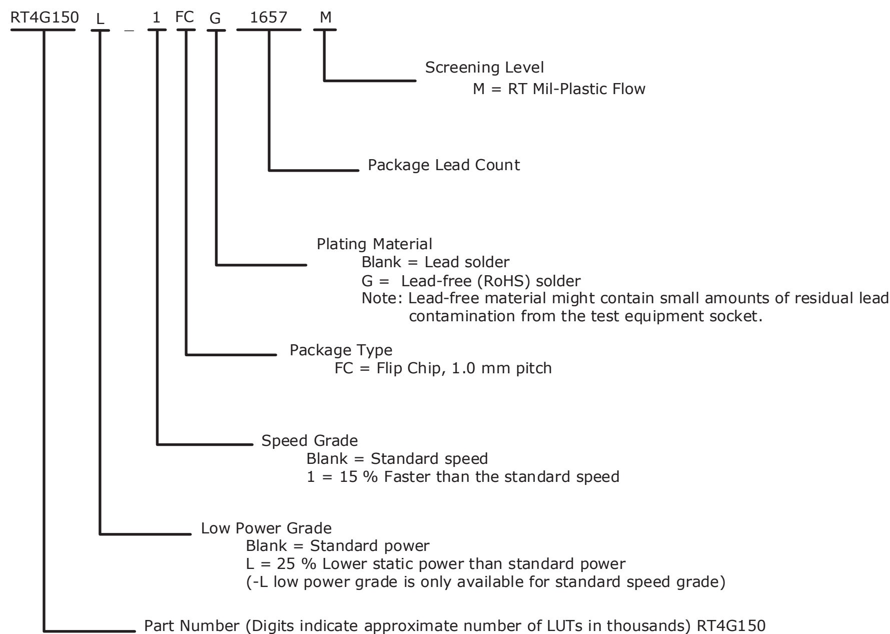


Figure 3-2. Ordering Information for Plastic Packages



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Contact your local Microchip SoC Products Group representative for device availability. For more information about device status, see DS0131: RTG4 FPGA Datasheet.

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4. Marking Specifications (Ask a Question)

Microchip marks the part number on the top of every RTG4 device along with other device specifications, as shown in the following figures.

Figure 4-1. RTG4 Ceramic Device Marking Specifications

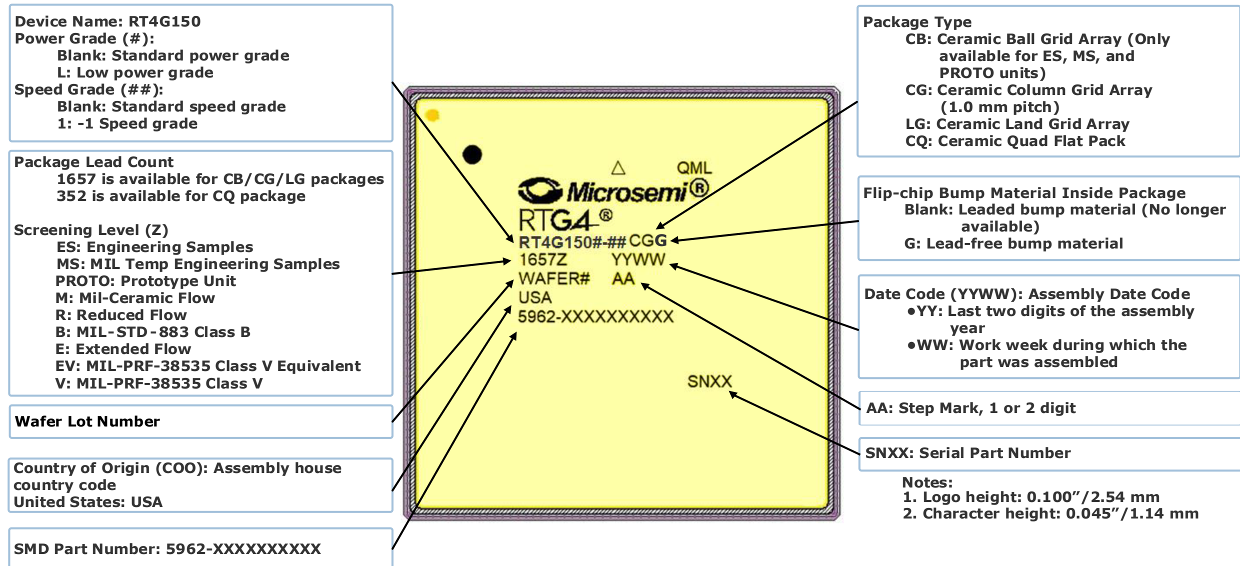
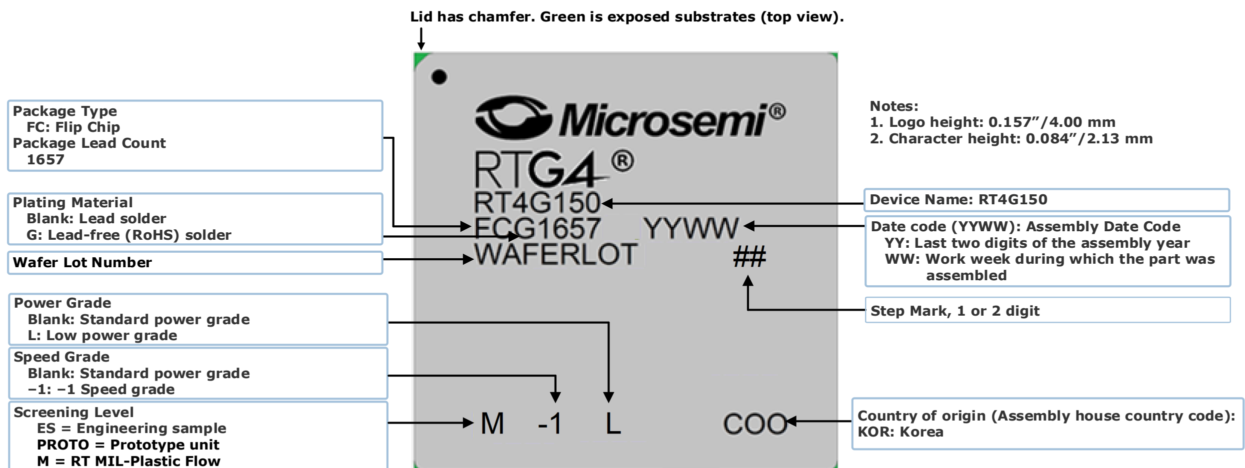


Figure 4-2. RTG4 Plastic Device Marking Specifications



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5. Screening Flows (Ask a Question)

The following tables describe the screening flows of the RTG4 FPGAs.

Table 5-1. RTG4 V Flow (QML Class V, MIL-PRF-38535)

Step	Screen	Test Method	Requirement
1	Internal Visual	2010, Condition A	100%
2	Serialization	In accordance with applicable Microchip device specification	100%
3	Temperature Cycling	1010, Condition C, 10 cycles minimum	100%
4	Constant Acceleration	Not required for RTG4 flip chip technology	N/A
5	Particle Impact Noise Detection (PIND)	Not required for RTG4 flip chip technology	N/A
6	Fine and Gross Leak	1014	100%
7	Radiographic (X-Ray)	Not required for RTG4 package with seam seal welding	N/A
8	Pre-Burn-In Electrical Parameters	In accordance with applicable Microchip device specification, with data Read and Record	100%
9	Dynamic Burn-In	1015, Condition D, 240 hours at 125 °C or 120 hours at 150 °C minimum	100%
10	Post-Dynamic-Burn-In Electrical Parameters	In accordance with applicable Microchip device specification, with data Read and Record	100%
11	Static Burn-In	1015, Condition C, 144 hours at 125 °C or 72 hours at 150 °C minimum	100%
12	Post-Static-Burn-In Electrical Parameters	In accordance with applicable Microchip device specification, with data Read and Record	100%
13	Percent Defective Allowable (PDA) Calculation	5004, 5% Overall, 3% Functional Parameters at 25 °C	All Lots, 100%
14	Final Electrical Test	In accordance with applicable Microchip device specification, with data Read and Record. Microchip device specification includes a, b, and c:	100%
	a. Static Tests (1) 25 °C (2) –55 °C and +125 °C	— 5005, Table 1, Subgroup 1 5005, Table 1, Subgroup 2, 3	
	b. Functional Tests (1) 25 °C (2) –55 °C and +125 °C	— 5005, Table 1, Subgroup 7 5005, Table 1, Subgroup 8a, 8b	
	c. Switching Tests at 25 °C	5005, Table 1, Subgroup 9	
15	Fine and Gross Leak	1014	100%
16	External Visual	2009	100%
17	Wafer Lot Specific Life Test (Group C)	MIL-PRF-38535, Appendix B, sec. B.4.2.c	All Lots
18	Assembly Lot Specific Destructive Physical Analysis (DPA)	MIL-STD-1580	All Lots

Note:

1. For CG(G)A devices, all Assembly, Screening, and TCI testing are performed at LGA level. Only QA electrical and mechanical visual are performed after solder column attachment.
2. RT4G150 and RT4G150L devices have the same silicon and are distinguished by screening the IDC current (measured on the VDD core supply voltage) limits at 125 °C final electrical test.

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Table 5-2. RTG4 E Flow (Microchip Extended Flow)

Step	Screen	Test Method	Requirement
1	Internal Visual	2010, Condition A	100%
2	Serialization	In accordance with applicable Microchip device specification	100%
3	Temperature Cycling	1010, Condition C, 10 cycles minimum	100%
4	Constant Acceleration	Not required for RTG4 flip chip technology	N/A
5	Particle Impact Noise Detection (PIND)	Not required for RTG4 flip chip technology	N/A
6	Fine and Gross Leak	1014	100%
7	Radiographic (X-Ray)	Not required for RTG4 package with seam seal welding	N/A
8	Pre-Burn-In Electrical Parameters	In accordance with applicable Microchip device specification, with data Read and Record	100%
9	Dynamic Burn-In	1015, Condition D, 240 hours at 125 °C or 120 hours at 150 °C minimum	100%
10	Post-Dynamic-Burn-In Electrical Parameters	In accordance with applicable Microchip device specification, with data Read and Record	100%
11	Static Burn-In	1015, Condition C, 144 hours at 125 °C or 72 hours at 150 °C minimum	100%
12	Post-Static-Burn-In Electrical Parameters	In accordance with applicable Microchip device specification, with data Read and Record	100%
13	Percent Defective Allowable (PDA) Calculation	5004, 5% Overall, 3% Functional Parameters at 25 °C	All Lots, 100%
14	Final Electrical Test	In accordance with applicable Microchip device specification, which includes a, b, and c:	100%
	a. Static Tests (1) 25 °C (2) –55 °C and +125 °C	— 5005, Table 1, Subgroup 1 5005, Table 1, Subgroup 2, 3	
	b. Functional Tests (1) 25 °C (2) –55 °C and +125 °C	— 5005, Table 1, Subgroup 7 5005, Table 1, Subgroup 8a, 8b	
	c. Switching Tests at 25 °C	5005, Table 1, Subgroup 9	
15	Fine and Gross Leak	1014	100%
16	External Visual	2009	100%

Note:

1. For CG(G)A devices, all Assembly, Screening, and TCI testing are performed at LGA level. Only QA electrical and mechanical visual are performed after solder column attachment.
2. RT4G150 and RT4G150L devices have the same silicon and are distinguished by screening the IDC current (measured on the VDD core supply voltage) limits at 125 °C final electrical test.
3. Microchip offers E Flow for users requiring additional screening beyond MIL-STD-833 Class B requirement. E Flow incorporates the majority of the screening procedures as outlined in Method 5004 of MIL-STD-883, Class S.
4. The Quality Conformance Inspection (QCI) for E Flow devices still comply with MIL-STD-833 Class B requirement.

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Table 5-3. RTG4 B Flow (MIL-STD-883 Class B)

Step	Screen	Test Method	Requirement
1	Internal Visual	2010, Condition B	100%
2	Serialization	In accordance with applicable Microchip device specification	100%
3	Temperature Cycling	1010, Condition C, 10 cycles minimum	100%
4	Constant Acceleration	Not required for RTG4 flip chip technology	N/A
5	Particle Impact Noise Detection (PIND)	Not required for RTG4 flip chip technology	N/A
6	Fine and Gross Leak	1014	100%
7	Pre-Burn-In Electrical Parameters	In accordance with applicable Microchip device specification	100%
8	Dynamic Burn-In	1015, Condition D, 160 hours at 125 °C or 80 hours at 150 °C minimum	100%
9	Percent Defective Allowable (PDA) Calculation	5004, 5%	All Lots, 100%
10	Final Electrical Test	In accordance with applicable Microchip device specification, which includes a, b, and c:	100%
	a. Static Tests (1) 25 °C (2) –55 °C and +125 °C	— 5005, Table 1, Subgroup 1 5005, Table 1, Subgroup 2, 3	
	b. Functional Tests (1) 25 °C (2) –55 °C and +125 °C	— 5005, Table 1, Subgroup 7 5005, Table 1, Subgroup 8a, 8b	
	c. Switching Tests at 25 °C	5005, Table 1, Subgroup 9	
11	External Visual	2009	100%

Note:

1. For CG(G)A devices, all Assembly, Screening, and TCI testing are performed at LGA level. Only QA electrical and mechanical visual are performed after solder column attachment.
2. RT4G150 and RT4G150L devices have the same silicon and are distinguished by screening the IDC current (measured on the VDD core supply voltage) limits at 125 °C final electrical test.

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Table 5-4. RTG4 Mil-Plastic Flow

Step	Screen	Test Method	Requirement
1	Final Electrical Test	In accordance with applicable Microchip device specification, which includes a, b, and c:	100%
	a. Static Tests (1) 25 °C (2) –55 °C and +125 °C	— 5005, Table 1, Subgroup 1 5005, Table 1, Subgroup 2, 3	
	b. Functional Tests (1) 25 °C (2) –55 °C and +125 °C	— 5005, Table 1, Subgroup 7 5005, Table 1, Subgroup 8a, 8b	
	c. Switching Tests at 25 °C	5005, Table 1, Subgroup 9	
2	External Visual	2009	QA Sample

Note:

1. All Assembly and Screening are performed at LGA level. Only QA electrical and mechanical visual are performed after solder ball attachment.
2. RT4G150 and RT4G150L devices have the same silicon and are distinguished by screening the IDC current (measured on the VDD core supply voltage) limits at 125 °C final electrical test.
3. More details on Mil-Plastic flow terms and conditions can be found in RT Mil-Plastic Overview.
4. RTG4 plastic package is non-hermetic.

Table 5-5. RTG4 PROTO Flow (Microchip RT-PROTO Flow)

Step	Screen	Test Method	Requirement
1	Final Electrical Test	In accordance with applicable Microchip device specification, which includes a, b, and c:	100%
	a. Static Tests (1) 25 °C (2) –55 °C and +125 °C	— 5005, Table 1, Subgroup 1 5005, Table 1, Subgroup 2, 3	
	b. Functional Tests (1) 25 °C (2) –55 °C and +125 °C	— 5005, Table 1, Subgroup 7 5005, Table 1, Subgroup 8a, 8b	
	c. Switching Tests at 25 °C	5005, Table 1, Subgroup 9	
2	Dimple Process	In accordance with applicable Microchip device specification	100%
3	External Visual	2009	QA Sample

Note:

1. For column and ball grid array packages, all Assembly and Screening are performed at LGA level. Only QA electrical and mechanical visual are performed after solder column and ball attachment.
2. RT4G150 and RT4G150L devices have the same silicon and are distinguished by screening the IDC current (measured on the VDD core supply voltage) limits at 125 °C final electrical test.
3. RTG4 PROTO follows Microchip RT-PROTO guidelines which can be found in RT-PROTO FPGA Description.
4. RTG4 PROTO FPGAs are offered in ceramic. The hermeticity of the lid seal is not guaranteed.

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6. RTG4 Device Family Overview (Ask a Question)

RTG4 FPGAs integrate Microchip's fourth-generation Flash-based FPGA fabric and high-performance interfaces, such as SerDes on a single chip, while maintaining the resistance to radiation-induced configuration upsets in harsh radiation environments. For example, space flight (LEO, MEO, GEO, HEO, and deep space), high-altitude aviation, medical electronics, and nuclear power plant control. The RTG4 family offers up to 151,824 registers, which are hardened by design against radiation-induced SEUs.

Each RTG4 logic element includes an LUT4 with fast carry chains providing high-performance FPGA fabric up to 300 MHz. There are multiple embedded memory options and embedded multiply-accumulate blocks for digital signal processing (DSP) up to 300 MHz. A high-speed serial interface provides 3.125 Gbps native SerDes communication, while double data rate DDR2/DDR3/LPDDR memory controllers provide high-speed memory interfaces.

6.1. High-Performance FPGA Fabric (Ask a Question)

Built on 65 nm process technology, the RTG4 FPGA fabric is composed of the logic module, LSRAM, µSRAM, and mathblocks. The logic module is the basic logic element and supports the following advanced features.

- A fully permutable four-input LUT optimized for lowest power.
- A dedicated carry chain based on carry look-ahead technique.
- A separate SEU-hardened flip-flop that can be used independently from LUT. Each flip-flop has its own synchronous reset. There are up to 206 asynchronous resets that drive RTG4 flip-flops devices.

The four-input LUTs are configured either to implement a four-input combinatorial function, or to implement an arithmetic function, where the LUT output is XORed with the carry input to generate the SUM output.

6.1.1. Dual-Port LSRAM (Ask a Question)

LSRAM block is targeted for storing large amounts of data for use with various operations. Each LSRAM block stores up to 24,576 bits. It contains port A and port B data ports. The LSRAM block is synchronous for read and write operations. Operations are triggered on the rising edge of the clock. The data output ports of the LSRAM have pipeline registers, which have control signals that are independent of the SRAM's control signals. An optional EDAC is built-in based on single error correction and double error detection. EDAC is enabled to mitigate the impact of SEU in the LSRAM.

6.1.2. Three-Port µSRAM (Ask a Question)

µSRAM block is the second type of SRAM block that is embedded in the fabric of the RTG4 devices. The µSRAM block is a three-port SRAM. It has port A and port B for read operations and port C for write operations. The two read ports are independent of each other and perform read operations in both synchronous and asynchronous modes. The write port is always synchronous. The µSRAM block stores up to 1,536 bits. These µSRAM blocks are primarily targeted for building embedded FIFOs to be used by any embedded fabric initiator. The µSRAM block is also used to store DSP coefficients. Optional built-in EDAC is enabled to mitigate the impact of SEU in the µSRAM.

6.1.3. µPROM Non-Volatile Memory (Ask a Question)

µPROM is a non-volatile Flash memory, which uses the same Flash technology as the FPGA configuration cells. µPROM is immune to memory upsets and has a TID performance beyond 100 krad, similar to the FPGA Flash configuration cells. RTG4 devices have up to 374 Kbits of µPROM memory. µPROM can be used for power-on initialization of RAMs and embedded IPs, as well as storage for DSP coefficients. The µPROM has a read performance of 50 MHz.

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6.1.4. Mathblocks for DSP Applications (Ask a Question)

The fundamental building block in any DSP algorithm is the Multiply Accumulate (MACC) function. The RTG4 FPGA device implements a custom 18-bit × 18-bit MACC (18 × 18 MACC) block for efficient implementation of complex DSP algorithms, such as Finite Impulse Response (FIR) filters, Infinite Impulse Response (IIR) filters, and Fast Fourier Transform (FFT) for filtering and image processing applications.

Each mathblock has the following capabilities.

- Supports 18 × 18 signed multiplications natively (A[17:0] × B[17:0])
- Supports dot product, and the multiplier computes: (A[8:0] × B[17:9] + A[17:9] × B[8:0]) × 29
- Built-in addition, subtraction, and accumulation units to combine multiplication results efficiently

In addition to the basic MACC function, DSP algorithms need small amounts of RAM for coefficients and larger RAMs for data storage. RTG4 μSRAMs are suited to serve the needs of coefficient storage, while the LSRAMs are used for data storage.

6.2. High-Speed Serial Interfaces (Ask a Question)

This section describes the high-speed interfaces of the RTG4 FPGAs.

6.2.1. SerDes Interface (Ask a Question)

RTG4 has up to six 3.125 Gbps quad SerDes transceivers, each supporting the following.

- Four SerDes/EPCS lanes (24 total SerDes lanes)
- The native SerDes interface facilitates implementation of SRIO in fabric or a 10 Gigabit media independent interface (SGMII) for a soft Ethernet

6.2.2. PCI Express (Ask a Question)

PCI Express (PCIe) is a high-speed, packet-based, point-to-point, low pin count, and serial interconnect bus. The RTG4 family has embedded high-speed serial interface blocks. Each SerDes block contains a PCIe system block. The PCIe system is connected to the SerDes block, and following are the main features supported.

- Supports ×1, ×2, and ×4 lane configuration
- Endpoint configuration only
- PCIe Base Specification Revision 2.0 (at Gen1 rate of 2.5 Gbps only)
- 5 Gbps compliant
- Embedded receive (2 Kbytes), transmit (1 Kbyte), and retry (1 Kbyte) buffer dual-port RAM implementation
- Up to 2 Kbytes maximum payload size
- 64-bit AXI or 32-bit/64-bit AHBL initiator and target interface to the application layer
- 32-bit APB interface to access configuration and status registers of PCIe system
- Up to 3 bit × 64 bit base address registers
- One Virtual Channel (VC)

6.2.3. XAUI/XGXS Extension (Ask a Question)

The XAUI/XGXS extension uses four SerDes channels, operating at 3.125 Gbps to allow the user to implement a 10 Gbps (XGMII) Ethernet PHY interface by connecting the XGMII fabric interface through an appropriate soft IP block in the fabric.

6.3. High-Speed Memory Interfaces: DDR2/3 Memory Controllers (Ask a Question)

RTG4 devices have up to two Fabric DDR (FDDR) subsystems in them. Each subsystem consists of a DDR controller, PHY, and a wrapper. Each FDDR block provides an interface to/from the FPGA fabric.

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The following are the main features supported by the FDDR blocks.

- Support for LPDDR, DDR2, and DDR3 memories
- Simplified DDR command interface to standard AMBA AXI/AHB interface
- Up to 667 Mbps (333 MHz double data rate) performance for DDR2 and DDR3
- Up to 266 Mbps (133 MHz double data rate) performance for LPDDR
- Supports different DRAM bus width modes: ×8, ×16, and ×32 (or ×9, ×18, and ×36 with SECDED enabled)
- Supports DRAM burst length of 4 or 8 in full bus-width mode; supports DRAM burst length of 4, 8, or 16 in half bus-width mode
- Supports memory densities up to 2 GB
- Supports a maximum of 8 memory banks
- SECDED enable/disable feature
- Embedded physical interface (PHY)
- Read and write buffers in fully associative CAMs, configurable in powers of 2, up to 64 reads plus 64 writes
- Support for dynamically changing clock frequency while in self-refresh
- Supports command reordering to optimize memory efficiency
- Supports data reordering, returning critical word first for each command

Each FDDR subsystem has an interface to the DDR memories. This is a multiplexed interface from the FPGA fabric, which is configured as either a single AXI 64-bit bus or two 32-bit AHB-Lite buses. There is also a 16-bit APB configuration bus, which is used to initialize the majority of the internal registers within the FDDR subsystem after Reset. This APB configuration bus is initiated by an initiator in the FPGA fabric.

6.4. Clock Sources: On-Chip Oscillators, PLLs, and CCCs (Ask a Question)

The RTG4 devices have an on-chip 50 MHz RC oscillator, which is available to the user for generating clocks to the on-chip resources and the logic built on the FPGA fabric array. The oscillator is used in conjunction with the integrated user Phase-Locked Loops (PLLs) and CCCs to generate clocks of varying frequency and phase. In addition to being available to the user, this oscillator is used by the system controller and Power-On-Reset (POR) circuitry.

The RTG4 devices have up to eight fabric CCC blocks and a dedicated PLL associated, with each CCC to provide flexible clocking to the FPGA fabric portion of the device. Each of the PLL and oscillator clock sources are radiation hardened to provide glitch free clocks in the system. The user can use any of the eight PLLs and CCCs to generate fabric clocks from the base fabric clock (CLK_BASE).

6.5. Programming (Ask a Question)

The RTG4 FPGAs support JTAG programming using an external programmer, such as the FlashPro4/5/6. In-system programming is supported through DirectC software, which enables a microprocessor to program the RTG4 device through the JTAG interface. For guidance on reprogramming in a radiation environment, see the UG0602: RTG4 FPGA Programming User Guide.

6.6. Radiation and Reliability (Ask a Question)

The RTG4 FPGAs are manufactured on a low-power 65 nm process with substantial reliability heritage.

The RTG4 FPGAs are immune to radiation-induced (SEU-induced) changes in configuration, due to the robustness of the Flash cells used to connect and configure logic resources and routing tracks.

No background scrubbing or reconfiguration of the FPGA is required to mitigate changes in configuration due to radiation effects. Data errors, due to radiation, are mitigated by hardwired

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SEU-resistant flip-flops in the logic cells and in the mathblocks. SECDED protection is optional for the embedded SRAM (LSRAM and µSRAM) and the DDR memory controllers. So, if a one-bit error is detected, it is corrected automatically. Errors of more than one-bit are detected only, but not corrected. SECDED error signals are brought to the FPGA fabric to allow the user to monitor the status of these protected internal memories.

For RTG4 radiation and reliability reports, see the web pages at Radiation and Reliability Data.

6.7. RTG4 Development Tools (Ask a Question)

This section describes the RTG4 development tools of the RTG4 device.

6.7.1. Design Software (Ask a Question)

Microchip's Libero® SoC is a comprehensive software toolset to design applications using the RTG4 device. Libero SoC manages the entire design flow from design entry, synthesis and simulation, place-and-route, timing, and power analysis, with enhanced integration of the embedded design flow. System designers leverage the easy-to-use Libero SoC that includes the following features.

- Synthesis, DSP, and debug support from Synopsys
- Simulation from Mentor Graphics
- Push-button design flow with power analysis and timing analysis
- SmartDebug for access to non-invasive probes within RTG4 devices. For more information about design software, see Libero SoC.

6.7.2. Design Hardware (Ask a Question)

Microchip's RTG4 development kit provides designers with an evaluation and development platform for applications, such as data transmission, serial connectivity, bus interface, and high-speed designs using RTG4 devices. The development board features an RT4G150 device, offering 151,824 logic elements in a ceramic package with 1,657 pins.

The RTG4 development board includes two 1 GB DDR3 and 2 GB of SPI Flash memories. The board also has several standard and advanced peripherals such as PCIe×4 edge connector, two FMC connectors for using several off-the-shelf daughter cards, USB, Philips Inter-Integrated Circuit (I2C), gigabit Ethernet port, Serial Peripheral Interface (SPI), and UART. A high precision operational amplifier circuitry on the board helps to measure the core power consumption by the device. There is a FlashPro programmer embedded on the board, allowing programming of the RTG4 FPGA through the JTAG interface.

For more information about kits and boards, see the web pages at RTG4 Development Kits.

6.7.3. IP Cores (Ask a Question)

Microchip offers many soft peripherals that can be placed in the FPGA fabric of the device. These include Core1553, CoreJESD204BRX/TX, CoreFIR, CoreFFT, and other DirectCores.

For more information about IP cores, see IP Cores.

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7. Revision History (Ask a Question)

Revision	Date	Description
E	01/2026	• Updated Screening Level information in Figure 3-1. Ordering Information for Ceramic Packages and Figure 3-2. Ordering Information for Plastic Packages. • Updated the step mark information in Figure 4-1. RTG4 Ceramic Device Marking Specifications and Figure 4-2. RTG4 Plastic Device Marking Specifications. • Removed Table 5-4. RTG4 R Flow and Table 5-5. RTG4 Mil-Ceramic Flow. • Updated Table 5-4. RTG4 Mil-Plastic Flow to reflect RT Mil-Plastic information. • Updated Table 5-5. RTG4 PROTO Flow (Microchip RT-PROTO Flow) to reflect end of plastic package offering.
D	01/2024	• Added Export Control Classification Number web page link to the Introduction section. • Added three steps to Table 5-5. RTG4 Mil-Ceramic Flow.
C	04/2023	• Updated Packages Table Headers to add CGG1657 and CQG352 in Table 1-1. • Replaced RTG4 Device Block Diagram in Figure 2-1. • Added information on Flip-chip Bump Material to Ordering Information for Ceramic Packages in Figure 3-1. • Added information on Flip-chip Bump Material to RTG4 Ceramic Device Marking Specifications in Figure 4-1. • Updated RT-PROTO FPGA Description with Microchip's link in Screening Flows section. • Updated UG0602: RTG4 FPGA Programming User Guide with Microchip's link in Programming section. • Updated Libero SoC with Microchip's link in Design Software section. • Updated RTG4 Development Kits with Microchip's link in Design Hardware section. • Updated IP Cores with Microchip's link in IP Cores section.
B	10/2021	• Updated in Screening Level "ES" to "No longer available" in Figure 3-2. Ordering Information for Plastic Packages. • Added row 18 for Assembly Lot Specific Destructive Physical Analysis (DPA) to Table 5-1. RTG4 V Flow (QML Class V, MIL-PRF-38535). • Updated "4 GB" to "2 GB" in bullet "Supports memory densities up to 2 GB" under High-Speed Memory Interfaces: DDR2/3 Memory Controllers section. • Included support for FlashPro6 in Programming section. • Deleted Note and added link RTG4 Programming User Guide in Radiation and Reliability section. • Added link to reports under Radiation and Reliability section. • Updated "2 GB × 1 GB DDR3" to "two 1 GB DDR3" in Design Hardware section.
A	11/2020	• Updated document to Microchip template. • Updated document number from 55700051 to DS90003294. • Added FCG/FC1657 column to Table 1-1. • Updated Figure 2-1 with information for ceramic packages. • Added Figure 2-2. • Updated Figure 3-1 with information for ceramic packages. • Added Figure 3-2. • Added Screening Flows section.

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Revision History (continued)

Revision	Date	Description
11.0	05/2019	• Added Marking Specifications section and figure RTG4 Device Marking Specifications. • Updated the High-Performance FPGA section. • Updated the Specifications section and CQ352 package details in table RTG4 FPGA Product Family. • Added Low Power Grade details to the figure RTG4 Ordering Information. • Changed the performance details for LPDDR in section High-Speed Memory Interfaces: DDR2/3 Memory Controllers. • Changed the RTG4 FPGA qualifications in the section Radiation and Reliability. • Added the Programming section.
10.0		• For the CQ352 package, the MSIO and total number of user I/O are updated. For more information, see table RTG4 FPGA Product Family. • Updated the RTG4 FPGA Block Diagram.
9.0		• Radiation Tolerance is updated. • Added CQ352 package details in table RTG4 FPGA Product Family. • Added packages and package type entries in figure RTG4 Ordering Information. • High-Performance FPGA Fabric, is updated for the number of asynchronous resets that are supported in RTG4 devices. • Removed the supported rank memory and DRAM burst length of two under High-Speed Memory Interfaces: DDR2/3 Memory Controllers.
8.0		• Removed reference to RT4G075 device (SAR 70694). • Table RTG4 FPGA Product Family was updated for uPROM kbits (SAR 66983). • Specifications section was updated for LVDS I/O standards information (SAR 69465). • RTG4 Device Block Diagram was updated (SAR 70694).
7.0		Figure RTG4 Device Block Diagram and uPROM Non-Volatile Memory were updated (SAR 66992).
6.0		• Removed all references to the RT4G200 device and the CG/LG2092. • Added User I/Os break-down information to table RTG4 FPGA Product Family. • Added software, hardware and IP information to the RTG4 Development Tools. • Removed the Device Status table (Table 2) and replaced it with the DS0131: RTG4 FPGA Datasheet as a reference. • Removed two references to the SII bus (SAR 65824).
5.0		Table RTG4 FPGA Product Family was updated (SAR 62641) and minor language edits were made.
4.0		Added TM symbol to RTG4 logo.
3.0		Clarified Military temp testing in figure RTG4 FPGA Block Diagram and space environments in the section RTG4 Device Family Overview.
2.0		Section High-Performance FPGA updated. Total SRAM information updated in table RTG4 FPGA Product Family.
1.0		Initial Revision

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ISBN: 979-8-3371-2565-7

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