PolarFire SoC FPGA Board Design Guidelines

Introduction (Ask a Question)

Good board design practices are required to achieve expected performance from both PCBs and PolarFire® SoC devices. High-quality and reliable results depend on minimizing noise levels, preserving signal integrity, meeting impedance and power requirements, and using appropriate transceiver protocols. These guidelines must be treated as a supplement to the standard board-level design practices.

This document is intended for readers who are familiar with the PolarFire SoC device, experienced in digital board design, and know about the electrical characteristics of systems. It discusses power supplies, high-speed interfaces, various control interfaces, and the associated peripheral components of PolarFire SoC FPGAs.

Table of Contents

1. Designing the Board (Ask a Question)

The PolarFire SoC family offers the industry's first RISC-V® based SoC FPGAs. The PolarFire SoC family combines a powerful 64-bit 5x core RISC-V Microprocessor Subsystem (MSS) with the FPGA fabric in a single device. Packed with this powerful combination, PolarFire SoC devices offer the scalable features of FPGAs and high-performance of ASICs like DDR3/DDR4, 12.7G Transceiver, PCIe Gen2 and HSIO/GPIO, and a highly configurable MSS.

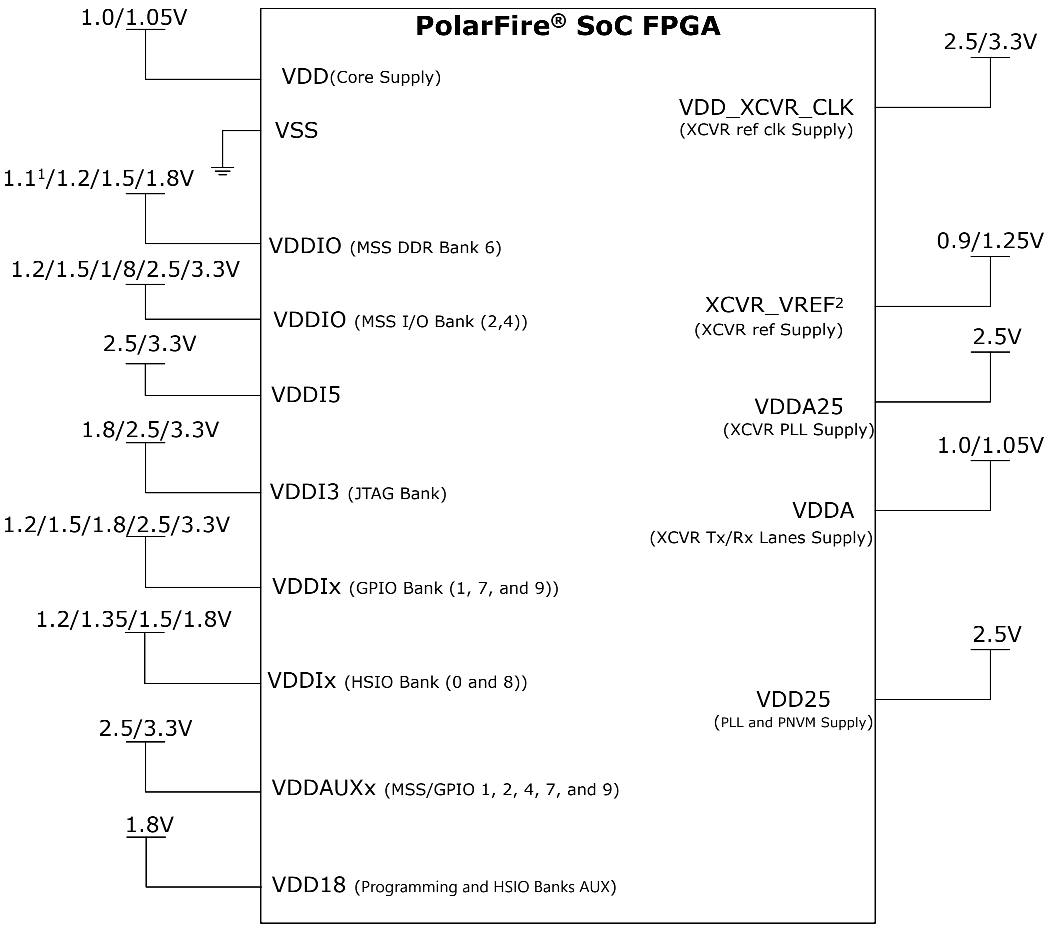
Subsequent sections discuss the following:

- Power Supplies
- I/O Glitch
- User I/O
- Clocks
- Reset
- DDR
- Device Programming
- Special Pins
- Transceiver
- AC and DC Coupling
- Brownout Detection

1.1. Power Supplies (Ask a Question)

The following illustration shows the typical power supply requirements for PolarFire SoC devices, and the recommended connections of power rails when every part of the device is used in a system. For more information on decoupling capacitors associated with individual power supplies, see PolarFire SoC Decoupling Capacitors.

Figure 1-1. Power Supplies



Notes:

1. 1.1V is for LPDDR4 support.
2. XCVR_VREF can be powered up internally or externally. In typical application using the internal VREF generator is good enough. If you use the internal VREF generator, no external supply needed to be provided and the pins only need to be connected to the decoupling caps on the board.

   External voltage is only recommended if the voltage needs to be tuned outside the range of what the internal VREF can provide.

   The XCVR_VREF is only required when the reference clock used is a voltage reference input standard (that is, SSTL). The XCVR_VREF is not required when the reference clock is differential (that is, LVDS or LVCMOS).

   If the XCVR_VREF is unused, follow Unused Power Supply.

Important: VDDIO (MSS DDR Bank 6) can also be operated at 1.1V to support LPDDR4. For more information about the board design recommendations for LPDDR4, see PolarFire Family Memory Controller User Guide.

To calculate the number of decoupling capacitors, it is important to know the target impedance of the power plane. Target impedance is calculated as follows:

$$Z_{Max} = \% \text{ Ripple} \times \frac{V_{supply}}{I_{trans}}$$

Where,

V_{supply}: Supply voltage of the power plane.

% Ripple: Percentage of ripples that is allowed on the power plane. See PolarFire SoC Datasheet for more information about ripple in Recommended Operating Conditions table.

I_{trans}: Transient current drawn on the power plane. The transient current is half of the maximum current. Maximum current is taken from the power calculator sheet.

Z_{max}: Target impedance of the plane.

For the PolarFire SoC device to operate successfully, power supplies must be free from unregulated spikes and the associated grounds must be free from noise. All overshoots and undershoots must be within the absolute maximum ratings provided in the PolarFire SoC Datasheet.

The following table lists the various power supplies required for PolarFire SoC FPGAs.

Table 1-1. Supply Pins

Name	Description
XCVR_VREF	Voltage reference for transceivers
VDD_XCVR_CLK	Power to input buffers for the transceiver reference clock
VDDA25	Power to the transceiver PLL
VDDA[1]	Power to the transceiver TX and RX lanes
VSS	Core digital ground
VDD[2]	Device core digital supply
VDDI3 (JTAG Bank)[3]	Power to JTAG bank pins
VDDI5[4]	VDDI5 power to MSS SGMII banks and MSS dedicated clocks.
VDDI2	VDDI2 power to MSS peripheral banks
VDDI4	Power to MSS peripheral banks
VDDI6	Power to MSS DDR banks
VDDIx (GPIO Banks)	Power to GPIO bank pins
VDDIx (HSIO Banks)	Power to HSIO bank pins
VDD25	Power to corner PLLs and PNVM
VDD18	Power to programming and HSIO auxiliary supply
VDDAUXx	Power to GPIO auxiliary supply

Notes:

1. VDDA Supply Requirements—VDDA must be powered at exactly 1.0V or 1.05V. For the complete details, see the "Recommended Operating Conditions" section in the PolarFire SoC Datasheet. This is a quiet supply critical to meeting all datasheet specifications. Users must strictly follow the decoupling capacitor guidelines in PolarFire SoC Decoupling Capacitors. Use a linear regulator if required to guarantee supply quietness—no exceptions.
2. VDD Supply Requirements—VDD must be powered at exactly 1.0V or 1.05V. For the complete details, see the "Recommended Operating Conditions" section in the PolarFire SoC Datasheet. This is a critical supply for device performance. Users must strictly follow the decoupling capacitor guidelines in PolarFire SoC Decoupling Capacitors to ensure performance.
3. VDDI3 must be powered before or at the same time as the other main supplies (VDD, VDD18, and VDD25) for the device to start initialization.

4. VDDI5 must be powered-up before or along with VDD. VDDI5 must reach its datasheet minimum value before VDD reaches a functional level and also before the time when MSS is ready to execute its first instruction (referred to as T_{CPU} in the datasheet).

VREFx—is the reference voltage for DDR3 and DDR4 signals. VREF voltages can be generated internally and externally.

- Internal VREF—is not subjected to PCB, package inductance, and capacitance loss. These changes provide the highest performance and can be programmed as required by DDR controller.
- External VREF—is fixed and cannot be programed as required. The PCB, package inductance, and capacitance impact the VREF performance.
  If VDDI and VDDAUX must be configured to the same voltage of 2.5V or 3.3V, ensure both VDDI and VDDAUX are supplied from the same regulator. Do not use different regulators to source these rails. This prevents any voltage variations between VDDI and VDDAUX. In this case, the board must not supply the VDDI and VDDAUX from individual voltage supplies.

  When a GPIO bank requires the VDDI to be less than 2.5V (1.2V, 1.5V, or 1.8V), the VDDAUX for that bank must be tied to 2.5V supply irrespective of the VDDI supply. VDDI requires a separate supply for the specific I/O type such as 1.5V or 1.8V.

  Notes:

  - The on-chip Power-on-Reset (POR) circuitry mandates that VDD, VDD18, and VDD25 supplies ramp monotonically from 0V to the minimum recommended operating voltage. Any deviation from this strict monotonic ramp will compromise device functionality and its adherence to the datasheet specifications.
  - You must initiate the I/O calibration only when both the VDDA and XCVR_VREF supplies are up.

  For a detailed pin description, see PolarFire SoC FPGA Packaging and Pin Descriptions User Guide.

1.1.1. PolarFire SoC Decoupling Capacitors (Ask a Question)

The following tables list the requirement of all decoupling capacitors for the MPFS460TS-FCG1152, MPFS250TS- FCG1152, MPFS250TS-FCVG484, MPFS250TS-FCSG536, MPFS250TS-FCVG784, and MPFS095T/MPFS025T-FCS325 devices. This is not a recommendation—it is a strict requirement. Users must implement these capacitors precisely in their schematics and board layouts. Failure to comply will result in unreliable operation, performance degradation and void the device compliance to datasheet specifications.

Table 1-2. Power-Supply Decoupling Capacitors[1]—MPFS460TS - FCG1152 (1 mm)

Pin Name	Ceramic										Tantalum
	1 nF	4.7 nF	22 nF	10 nF	47 nF	0.1 µF	1 µF	4.7 µF	10 µF	47 µF	330 µF
VDD	—	—	—	—	—	4	—	—	—	—	3
VDD18	—	—	—	—	—	2	—	—	—	2	—
VDDA	—	3	—	1	—	6	—	—	—	2	—
VDDA25	—	—	—	—	—	4	—	—	—	1	—
VDD25	—	—	—	—	—	5	—	—	1	—	—
VDDAUXGPIO	—	—	—	—	—	2	—	—	—	1	—
GPIO	—	—	—	—	—	2	—	—	—	1	—
HSIO	—	—	—	—	—	2	—	—	—	1	—
VDD_XCVR_CLK	—	—	—	—	—	2	—	—	1	—	—
SERDES_VREF	—	—	—	—	—	2	—	—	—	—	—
VDDI3	—	—	—	—	—	2	—	—	1	—	—
Bank 2	—	—	—	—	—	2	—	—	1	—	—

Table 1-2. Power-Supply Decoupling Capacitors[1]—MPFS460TS - FCG1152 (1 mm) (continued)

Pin Name	Ceramic										Tantalum
	1 nF	4.7 nF	22 nF	10 nF	47 nF	0.1 µF	1 µF	4.7 µF	10 µF	47 µF	330 µF
Bank 4	—	—	—	—	—	2	—	—	1	—	—
Bank 5	—	—	—	—	—	2	—	—	1	—	—
Bank 6 MSS DDR	—	—	—	1	—	1	—	—	—	1	—

Note: 1. The guidelines are provided on how to effectively decouple only the PolarFire SoC device. If the power source is placed on a different PCB or delivered through interconnects (flex cables or connectors), ensure an effective power delivery to the PolarFire SoC device. Follow the recommended operational conditions as per PolarFire SoC Datasheet.

Table 1-3. Power-Supply Decoupling Capacitors[1]—MPFS250TS - FCG1152 (1 mm)

Pin Name	Ceramic									Tantalum
	1 nF	4.7 nF	22 nF	10 nF	47 nF	0.1 µF	1 µF	10 µF	47 µF	330 µF
VDD	—	—	2	5	2	1	1	—	1	2
VDD18	—	—	—	1	—	1	—	—	2	—
VDDA	—	3	—	1	—	6	—	—	2	—
VDDA25	2	—	—	—	—	2	—	—	1	—
VDD25	1	—	—	2	—	2	—	—	1	—
VDDAUX (GPIO)	—	1	—	1	—	1	—	—	1	—
GPIO Bank	1	—	—	—	—	—	—	—	1	—
HSIO Bank	—	—	—	—	—	2	—	—	1	—
VDD_XCVR_CLK	—	—	—	—	—	2	—	1	—	—
SERDES_VREF	—	—	—	—	—	2	—	—	—	—
VDDI3	—	—	—	—	—	2	—	1	—	—
Bank 2	—	—	—	—	—	2	—	1	—	—
Bank 4						2		1		
Bank 5	—	—	—	—	—	2	—	1	—	—
Bank 6 MSS DDR	—	—	—	1	—	1	—	—	1	—

Note:

1. The guidelines are provided on how to effectively decouple only the PolarFire SoC device. If the power source is placed on a different PCB or delivered through interconnects (flex cables or connectors), ensure an effective power delivery to the PolarFire SoC device. Follow the recommended operational conditions as per PolarFire SoC Datasheet.

Table 1-4. Power-Supply Decoupling Capacitors[1]—MPFS250TS/MPFS160TS/MPFS095TS/MPFS025TS - FCVG484 (0.8 mm)

Pin Name	Ceramic										Tantalum
	1 nF	4.7 nF	22 nF	10 nF	47 nF	0.1 µF	1 µF	4.7 µF	10 µF	47 µF	330 µF
VDD	—	—	2	5	2	1	—	—	—	—	2
VDD18	—	—	—	1	—	1	—	—	1	1	—
VDDA	—	2	—	—	—	6	—	—	—	1	—
VDDA25	—	—	—	—	2	2	—	—	1	1	—
VDD25	4	—	—	1	—	3	—	—	—	1	—
VDDAUX (GPIO)	—	—	—	2	1	2	—	—	—	1	—
GPIO	—	—	—	—	—	—	—	—	—	2	—
HSIO	—	—	—	—	—	—	—	—	—	1	—
VDD_XCVR_CLK	—	—	—	—	—	2	—	—	1	—	—

Table 1-4. Power-Supply Decoupling Capacitors[1]—MPFS250TS/MPFS160TS/MPFS095TS/MPFS025TS - FCVG484 (0.8 mm) (continued)

Pin Name	Ceramic										Tantalum
	1 nF	4.7 nF	22 nF	10 nF	47 nF	0.1 µF	1 µF	4.7 µF	10 µF	47 µF	330 µF
SERDES_VREF	—	—	—	—	—	2	—	—	—	—	—
VDDI3	—	—	—	—	—	2	—	—	1	—	—
Bank 2	—	—	—	—	—	2	—	—	1	—	—
Bank 4	—	—	—	—	—	2	—	—	1	—	—
Bank 5	—	—	—	—	—	2	—	—	1	—	—
Bank 6 MSS DDR	—	—	—	—	—	1	1	—	—	1	—

Note:

1. The guidelines are provided on how to effectively decouple only the PolarFire SoC device. If the power source is placed on a different PCB or delivered through interconnects (flex cables or connectors), ensure an effective power delivery to the PolarFire SoC device. Follow the recommended operational conditions as per PolarFire SoC Datasheet.

Table 1-5. Power-Supply Decoupling Capacitors[1]—MPFS250TS/MPFS160TS/MPFS095TS - FCSG536 (0.5 mm)

Pin Name	Ceramic										Tantalum	
	1 nF	4.7 nF	22 nF	10 nF	47 nF	0.1 µF	1 µF	4.7 µF	10 µF	47 µF	100 µF	330 µF
VDD	—	—	—	—	—	—	—	—	—	2	1	2
VDD18	—	—	—	1	—	1	—	—	—	2	—	—
VDDA	3	—	—	—	—	1	—	—	—	2	—	—
VDDA25	2	—	—	—	—	2	—	—	—	1	—	—
VDD25	—	—	—	—	—	3	—	—	—	1	—	—
VDDAUX (GPIO)	—	1	—	1	—	1	—	—	—	1	—	—
GPIO Bank	—	—	—	—	4	4	—	—	—	2	—	—
HSIO Bank	—	—	—	—	—	2	—	—	—	2	—	—
VDD_XCVR_CLK	—	—	—	—	—	2	—	—	1	—	—	—
SERDES_VREF	—	—	—	—	—	2	—	—	—	—	—	—
Bank 3 JTAG	—	—	—	—	—	2	—	—	1	—	—	—
Bank 2	—	—	—	—	—	2	—	—	1	—	—	—
Bank 4	—	—	—	—	—	2	—	—	1	—	—	—
Bank 5	—	—	—	—	—	2	—	—	1	—	—	—
Bank 6 MSS DDR	—	—	—	—	—	—	1	—	—	1	—	—

Note:

1. The guidelines are provided on how to effectively decouple only the PolarFire SoC device. If the power source is placed on a different PCB or delivered through interconnects (flex cables or connectors), ensure an effective power delivery to the PolarFire SoC device. Follow the recommended operational conditions as per PolarFire SoC Datasheet.

Table 1-6. Power-Supply Decoupling Capacitors[1]—MPFS250TS/MPFS160TS/MPFS095TS - FCVG784 (0.8 mm)

Pin Name	Ceramic										Tantalum
	1 nF	2.2 nF	3.3 nF	4.7 nF	10 nF	47 nF	0.1 µF	1 µF	10 µF	47 µF	330 µF
VDD	—	—	—	—	—	3	3	3	—	1	2
VDD18	—	—	—	1	1	—	1	—	—	2	—
VDDA	—	2	—	—	2	—	1	—	—	2	—
VDDA25	1	—	—	—	—	—	1	—	—	1	—

Table 1-6. Power-Supply Decoupling Capacitors[1]—MPFS250TS/MPFS160TS/MPFS095TS - FCVG784 (0.8 mm) (continued)

Pin Name	Ceramic										Tantalum
	1 nF	2.2 nF	3.3 nF	4.7 nF	10 nF	47 nF	0.1 µF	1 µF	10 µF	47 µF	330 µF
VDD25	1	—	—	—	2	—	2	—	—	1	—
VDDAUX (GPIO)	—	—	—	1	1	—	1	—	—	1	—
GPIO Bank	1	—	—	1	—	—	1	—	—	1	—
HSIO Bank	1	—	—	1	—	—	1	—	—	1	—
VDD_XCVR_CLK	—	—	—	—	—	—	2	—	1	—	—
SERDES_VREF	—	—	—	—	—	—	2	—	—	—	—
Bank 3 JTAG	—	—	—	—	—	—	2	—	1	—	—
Bank 2	—	—	—	—	—	—	2	—	1	—	—
Bank 4	—	—	—	—	—	—	2	—	1	—	—
Bank 5	—	—	—	—	—	—	2	—	1	—	—
Bank 6 MSS DDR	1	—	1	1	1	—	1	—	—	1	—

Note:

1. The guidelines are provided on how to effectively decouple only the PolarFire SoC device. If the power source is placed on a different PCB or delivered through interconnects (flex cables or connectors), ensure an effective power delivery to the PolarFire SoC device. Follow the recommended operational conditions as per PolarFire SoC Datasheet.

Table 1-7. Power-Supply Decoupling Capacitors[1]—MPFS095TS/MPFS025TS - FCSG325 (0.5 mm)

Pin Name	Ceramic										Tantalum
	1 nF	4.7 nF	22 nF	10 nF	47 nF	0.1 µF	1 µF	4.7 µF	10 µF	47 µF	330 µF
VDD	—	4	—	1	—	1	—	—	1	1	1
VDD18	—	—	—	—	—	2	—	—	—	2	—
VDDA	2	—	—	—	—	2	—	—	1	—	—
VDDA25	1	—	—	—	—	1	—	—	—	1	—
VDD25	—	—	—	—	—	5	—	—	1	—	—
VDDAUXGPIO	—	—	—	—	—	2	—	—	—	1	—
GPIO Bank	—	—	—	—	—	2	—	—	—	1	—
HSIO Bank	—	—	—	—	—	2	—	—	—	1	—
VDD_XCVR_CLK	—	—	—	—	—	2	—	—	1	—	—
SERDES_VREF	—	—	—	—	—	2	—	—	—	—	—
JTAG Bank 3 (VDDI3)	—	—	—	—	—	2	—	—	1	—	—
Bank 2	—	—	—	—	—	2	—	—	1	—	—
Bank 4	—	—	—	—	—	2	—	—	1	—	—
Bank 5	—	—	—	—	—	2	—	—	1	—	—
Bank 6 MSS	—	—	—	—	—	—	1	—	—	1	—

Note:

1. The guidelines are provided on how to effectively decouple only the PolarFire SoC device. If the power source is placed on a different PCB or delivered through interconnects (flex cables or connectors), ensure an effective power delivery to the PolarFire SoC device. Follow the recommended operational conditions as per PolarFire SoC Datasheet.

Alternative decoupling capacitors may only be used if their physical sizes meet or exceed the performance of the specified network. Any substitution mandates rigorous analysis of the resulting power distribution network's impedance versus frequency to eliminate resonant spikes. See Figure

1-1 for power supply design guidelines. Failure to perform this analysis may cause system related voltage ripple and performance issues and instability.

For more information about the internal package capacitance for power supplies associated with PolarFire SoC packages, see PolarFire SoC FPGA Packaging and Pin Descriptions User Guide.

The following table lists the required decoupling capacitors for PolarFire SoC packages.

Table 1-8. Recommended Decoupling Capacitors For PolarFire SoC Devices

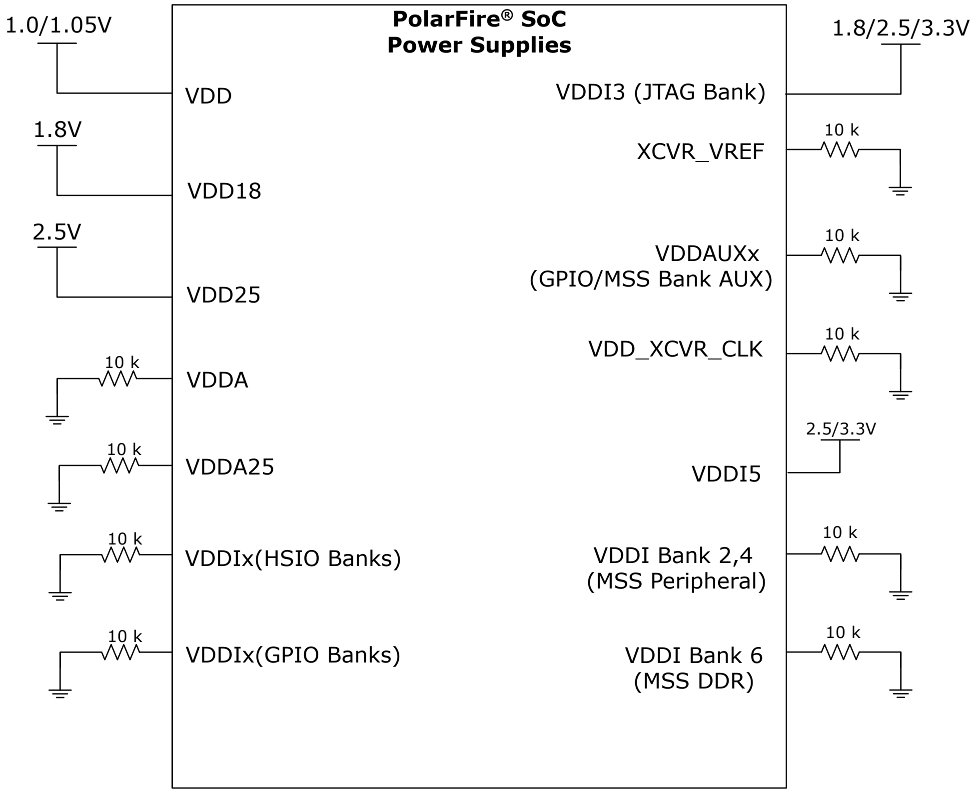
De-Cap Value	Part Number	Package	Description
1 nF	CL05B102KO5NNNC	0402	For 1 mm package
22 nF	GRM155R71C223KA01D	0402	For 1 mm package
10 nF	GRM155R71C103KA01D	0402	For 1 mm package
0.1 µF	GRM155R71C104KA88D	0402	For 1 mm package
10 nF	GRM15XR11C103KA86	0402	For 1 mm package
4.7 nF	GRM155R11H472KA01	0402	For 1 mm package
10 µF	GRM21BR71A106KE51	0805	Bulk Caps (for 0.5, 0.8, and 1 mm)
47 µF	GRM31CR61A476KE15	1206	Bulk Caps (for 0.5, 0.8, and 1 mm)
330 µF	T495D337K010ATE150	2917	Bulk Caps (for 0.5, 0.8, and 1 mm)
1 nF	GRM033R71C102KA01	0201	For 0.8 and 0.5 mm package
2.2 nF	GRM033R71C222KA88D	0201	For 0.8 mm package
10 nF	GRM033R71A103KA01	0201	For 0.8 and 0.5 mm package
0.1 µF	GRM033C71C104KE14	0201	For 0.8 and 0.5 mm package
1 µF	GRM155R70J105KA12J	—	For 0.5 mm, 0.8 mm, and 1 mm package
47 nF	GRM155R71C473KA01J	—	For 0.5 mm, 0.8 mm, and 1 mm package

Important: Equivalent capacitor values can be used from a different vendor. For more information about the Packaging Decoupling Capacitors, see PolarFire SoC FPGA Packaging and Pin Descriptions User Guide.

1.1.2. Unused Power Supply (Ask a Question)

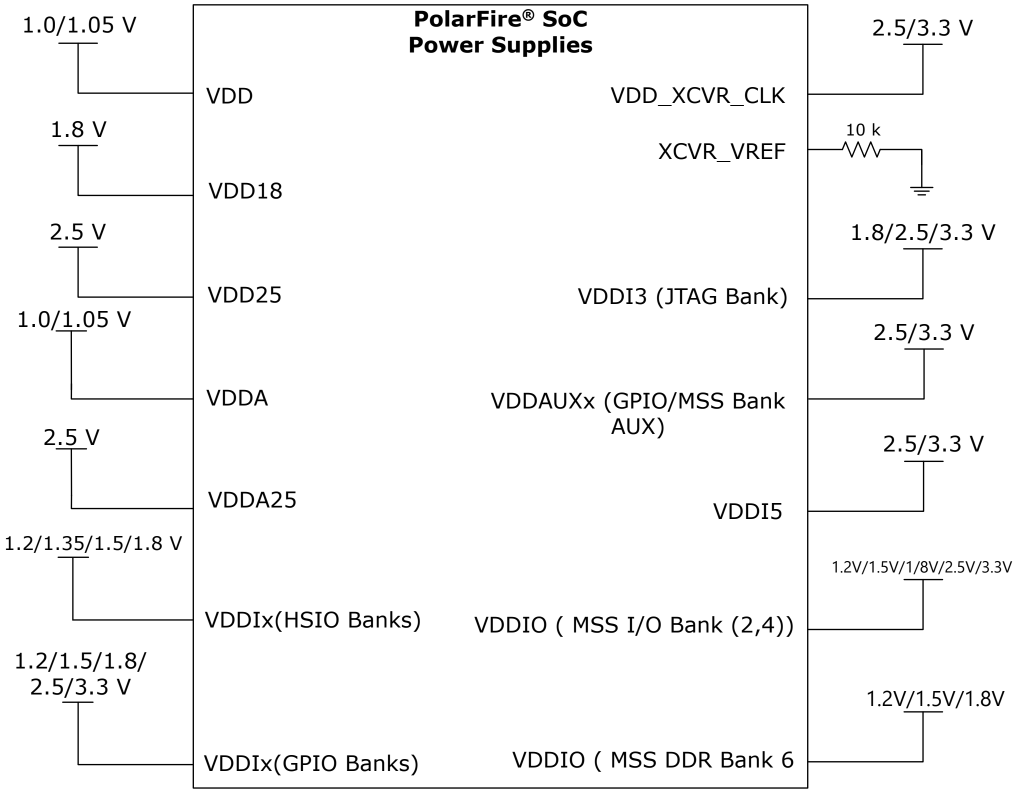
The following figure shows how power supplies can be configured when not in use and when you need to reduce leakage and power for the system.

Figure 1-2. Option 1 for Unused Connections



The following figure shows the power configuration of unused supplies. This option can be used when there is an intent to power-up the various supplies at a later time in the system, and the I/Os are not being used.

Figure 1-3. Option 2 for Unused Connections



Important: To simplify the board-level routing, multiple 10 kΩ resistors can be used as required. The power supplies can also be grouped into a single 10 kΩ resistor and tied-off to VSS.

1.1.3. Pin Assignment Tables (Ask a Question)

PolarFire SoC Packaging Pin Assignment Table (PPAT) contains information about the recommended DDR pinouts, PCI EXPRESS capability for XCVR-0, DDR Lane information for I/O CDR, generic IOD interface pin placement, and unused condition for package pins.

1.2. I/O Glitch (Ask a Question)

A glitch might occur during power-up or power-down for GPIO or HSIO outputs in PolarFire SoC devices. Glitch can occur before or after the device reaches a functional state. These glitches are not observed on LVDS outputs or Transceiver I/Os. No reliability issues are caused by either of the glitch types. Following are the types of glitches that can occur.

- Parasitic glitches might occur for GPIOs or HSIOs before the device reaches functional state with a maximum glitch of 1V with a 0.4 ms width. This type of glitch can typically be ignored. It is recommended to use a 100K pull-down resistor on critical signals[1] of the GPIO or HSIO pins if this type of glitch cannot be ignored. No glitches are observed once mitigation recommendations are placed. This may occur for both erased/blank and programmed units.
- Another type of glitch might occur on GPIOs and HSIOs during power-on sequencing or boot-up. This is due to a weak pull-up resistor being enabled by default on an input, output or

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[1] Critical outputs such as reset or clock of the HSIO or GPIOs going into another device.

bidirectional I/O. To mitigate this glitch, use the Libero SoC I/O Editor or PDC constraint to program a weak pull-down on the output buffer on the specified I/O. This might occur for both erased/blank and programmed units.

- The last type of glitch might occur after the device reaches functional state and might occur for both erased/blank and programmed units. This type of glitch is related to the power-up and power-down sequence of VDDI and VDDAUX supplies. This occurs only on GPIOs where the VDDI is 1.5V or 1.8V only with a maximum glitch of 1V with a 0.8 ms width during power-up and a maximum glitch of 1.8V with a 1 ms width during power down. For HSIOs where the VDDI is 1.5V or 1.8V only a maximum glitch of 600 mV and 1.5 ms width might occur at power-up and a maximum glitch of 220 mV and 200 µs width might occur at power-down.

To mitigate the post functional state glitch, follow the recommendations in the following tables.

Table 1-9. Power Sequencing[1] (For GPIO/MSSIO)

Use Cases for GPIO/MSSIO		Power-up Sequencing Requirement for Mitigating Glitches[2]	Power-down Sequencing Requirements for Mitigating Glitches[2]
VDDI	VDDAUX	—	—
1.2V	2.5V	No glitch occurs	No glitch occurs
1.5V	2.5V	Power up VDDAUX before VDDI of that bank	Power down VDDI before VDDAUX of that bank
1.8V	2.5V	Power up VDDAUX before VDDI of that bank	Power down VDDI before VDDAUX of that bank
2.5V	2.5V	Power VDDAUX and VDDI from the same regulator	No glitch occurs
3.3V	3.3V	Power VDDAUX and VDDI from the same regulator	No glitch occurs

(1) No glitches are observed once mitigation recommendations are placed.
(2) This power sequence does not mitigate any parasitic glitches. As mentioned, add a 100K pull-down resistor to critical signals of GPIO or HSIO pins for mitigation of parasitic glitches.

Note: The MSSIO power sequencing requirements are identical to those of GPIO. Therefore, the GPIO power-up and power-down sequencing requirements listed in this section also apply to MSSIO banks.

Table 1-10. Power Sequencing[1] (For HSIO)

Use Cases for HSIO		Power-up Sequencing Requirement for Mitigating Glitches[2]	Power-down Sequencing Requirements for Mitigating Glitches[2]
VDDI	VDD18	—	—
1.2V	1.8V	No glitch occurs	No glitch occurs
1.5V	1.8V	Power up VDD18 before VDDI of that bank	Power down VDDI before VDD18, VDD, VDD25 of that bank
1.8V	1.8V	Power up VDD18 before VDDI of that bank	Power down VDDI before VDD18, VDD, VDD25 of that bank

(1) No glitches are observed once mitigation recommendations are placed.
(2) This power sequence does not mitigate any parasitic glitches. As mentioned, add a 100K pull-down resistor to critical signals of GPIO or HSIO pins for mitigation of parasitic glitches.

Important: A glitch can occur on GPIO pins during JTAG programming if power is disrupted. The glitch can be mitigated by powering down VDDI before VDDAUX, VDD, and VDDI3.

1.3. User I/O (Ask a Question)

PolarFire SoC FPGAs have two types of I/O buffers: HSIO and GPIO. HSIO buffers are optimized for single-ended buffers with supplies from 1.2V to 1.8V. GPIO buffers support single-ended and true differential interfaces with supplies from 1.2V to 3.3V. PolarFire SoC FPGAs support the following types of I/O Banks:

- GPIO Banks—These Banks support I/O buffers for single-ended and true differential signals from 1.2V to 3.3V.
- HSIO Banks—These Banks support optimized I/O buffers for single-ended and true differential signals from 1.2V to 1.8V.
- MSS I/Os—These banks can support I/O buffer for single-ended signals from 1.2V to 3.3V.
- MSS DDR I/Os—These banks can support I/O buffer for single-ended and differential per the Pin table signals at 1.2V, 1.5V to 1.8V.
- MSS SGMII I/Os—These banks can support I/O buffer for single-ended and differential per the Pin table signals at 2.5V or 3.3V.

Notes:

- When the HSIO bank is configured as an LVDS receiver, the concerned I/Os must be connected externally by a 100Ω resistor.
- For supporting cold sparing application and guidance on pin assignment, see Cold Sparing.

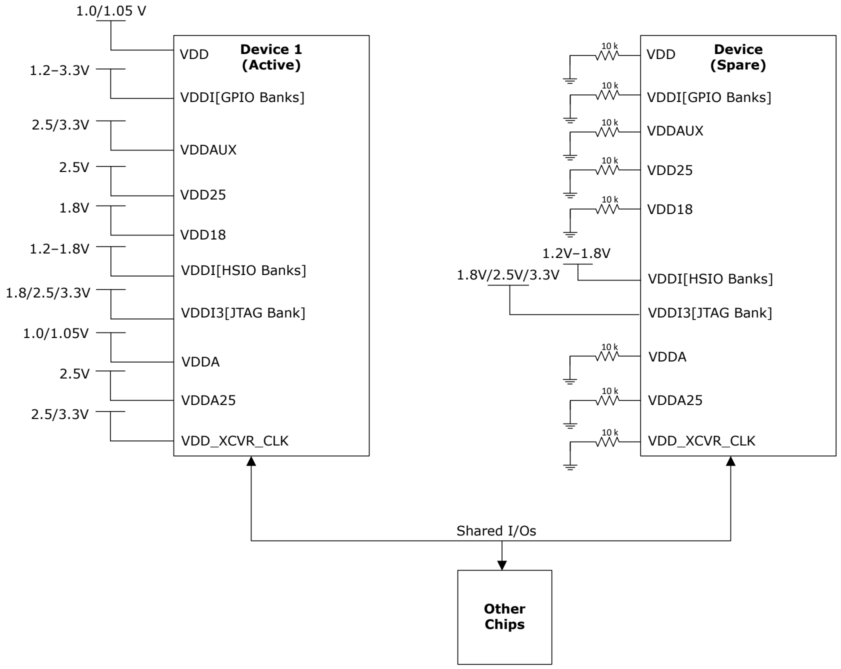
For more information about key features of I/O buffers and supported standards, see PolarFire SoC FPGA Packaging and Pin Descriptions User Guide and PolarFire Family I/O User Guide.

1.3.1. Cold Sparing (Ask a Question)

PolarFire SoC devices support cold sparing for GPIO and HSIO. Cold sparing is implemented by connecting the devices as shown in the following figure. The system board has two PolarFire SoC devices in parallel, and the devices share I/Os. The spare device has its HSIO VDDI banks powered up to prevent I/O leakage through the ESD diodes. As a result, low power and a protected state for the spare device is established. The spare device can be changed to an active device by powering-up all the supplies. The active device can be changed to a spare device by powering down all the supplies, except HSIO VDDI banks.

A typical cold sparing application integrates two parallel devices with shared I/O connections, as shown in the following figure.

Figure 1-4. Cold Sparing



For supporting cold sparing applications on GPIO I/Os:

- All GPIO banks support single-ended and differential signaling.

  Naming Convention:
  - GPIOXXPBY: I/O pair XX, bank Y, P node
  - GPIOXXNBY: I/O pair XX, bank Y, N node
- Both nodes of any GPIO pair (for example, GPIO242PB1 and GPIO242NB1) can be used for single-ended signals.

The following points summarize the cold sparing recommendations:

- For a GPIO pair (for example, GPIO242[P/N]B1):
  - Use both as outputs or both as inputs
  - Avoid mixed directions (one input and one output)
- If mixed directions are required:
  - Add 15 kΩ pull-down to VSS on the output node only.
    - GPIO242PB1 (output) + GPIO242NB1 (input): Pull-down on GPIO242PB1
    - GPIO242PB1 (input) + GPIO242NB1 (output): Pull-down on GPIO242NB1
- When adding 15 kΩ pull-down, ensure that no additional external or internal pull-up resistor has been added to the signal. The user must ensure that with the pull-down resistor the signal integrity of the signal has been maintained.
- No pull-down needed if both are inputs or both are outputs.

Note: Transceiver and JTAG pins do not support the cold sparing feature.

1.3.2. Hot Socketing (GPIO Only) (Ask a Question)

Hot socketing (also known as hot swapping or hot plug-in) prevents damage to the PolarFire SoC FPGA if, at any time, voltage is detected at I/O while the device is powered OFF. It also helps prevent disruptions that may occur in the rest of the system if the I/O of a device are connected without a valid power supply.

Only GPIOs support hot socketing. In hot socketing, GPIOs are in high-impedance (hi-Z) state.

The GPIO maintains the following high-impedance state until the power supplies are at a valid state.

- VDDAUx is greater than or equal to 1.6V
- VDDIx is greater than or equal to 0.8V
- VDD and VDD25 are both high and the PolarFire SoC FPGA controller has asserted the global I/O ring signal (IO_EN)

Note: TMS, TDI, TRSTB, DEVRST_N, and FF_EXIT_N do not support hot socketing.

1.3.2.1. Over-Voltage Tolerance for GPIO (Ask a Question)

If GPIO is configured with the following settings, GPIO supports over-voltage tolerance, ensuring that the I/O signal at the pad is at a higher potential than the VDDIx power supply.

Table 1-11. Over-Voltage Tolerance

Standard	OE	Clamp Diode	VREF (Input)	Weak Pull-Up/ Pull-Down	Termination	Hot-plug
PCI	x	ON	ON	ON	ON	Disabled
GPIO	1	ON	ON	ON	ON	Disabled
	0	OFF	OFF	OFF	OFF	Enabled

For recommended operating conditions about over-voltage tolerance, see PolarFire SoC Datasheet.

1.4. MSS I/Os (Ask a Question)

PolarFire SoC FPGAs support the following type of MSS I/O buffers.

- MSS DDR I/Os
- MSS SGMII I/Os
- MSS-Specific I/O

1.4.1. MSS DDR I/Os (Ask a Question)

The MSS DDR I/Os are a dedicated set of pins for x32 width DDR interface with ECC support. The dedicated set of pins are as follows:

- MSS_DDR_DQ[0:35]
- MSS_DDR_DQSP[0:4], MSS_DDR_DQSN[0:4]
- MSS_DDR_DM[0:4]
- MSS_DDR_A[0:16]
- MSS_DDR_CK_0, MSS_DDR_CK_N0
- MSS_DDR_CK_1, MSS_DDR_CK_N1
- MSS_DDR_RAM_RST_N
- MSS_DDR_VREF_IN
- MSS_DDR_BA0, MSS_DDR_BA1
- MSS_DDR_BG0, MSS_DDR_BG1
- MSS_DDR_CS0, MSS_DDR_CS1
- MSS_DDR_CKE0, MSS_DDR_CKE1
- MSS_DDR_ODT0, MSS_DDR_ODT1

- MSS_DDR_ACT_N
- MSS_DDR_WE_N
- MSS_DDR_ALERT_N
- MSS_DDR_PARITY
  The interface supports the following types of DDR memories:
- DDR4 – Single and Dual Rank
- DDR3 – Single and Dual Rank
- LPDDR4
- LPDDR3

For more details about pin mapping and DDR user models, see PolarFire SoC Packaging Pin Assignment Table (PPAT) and PolarFire Family Memory Controller User Guide.

1.4.2. MSS SGMII I/Os (Ask a Question)

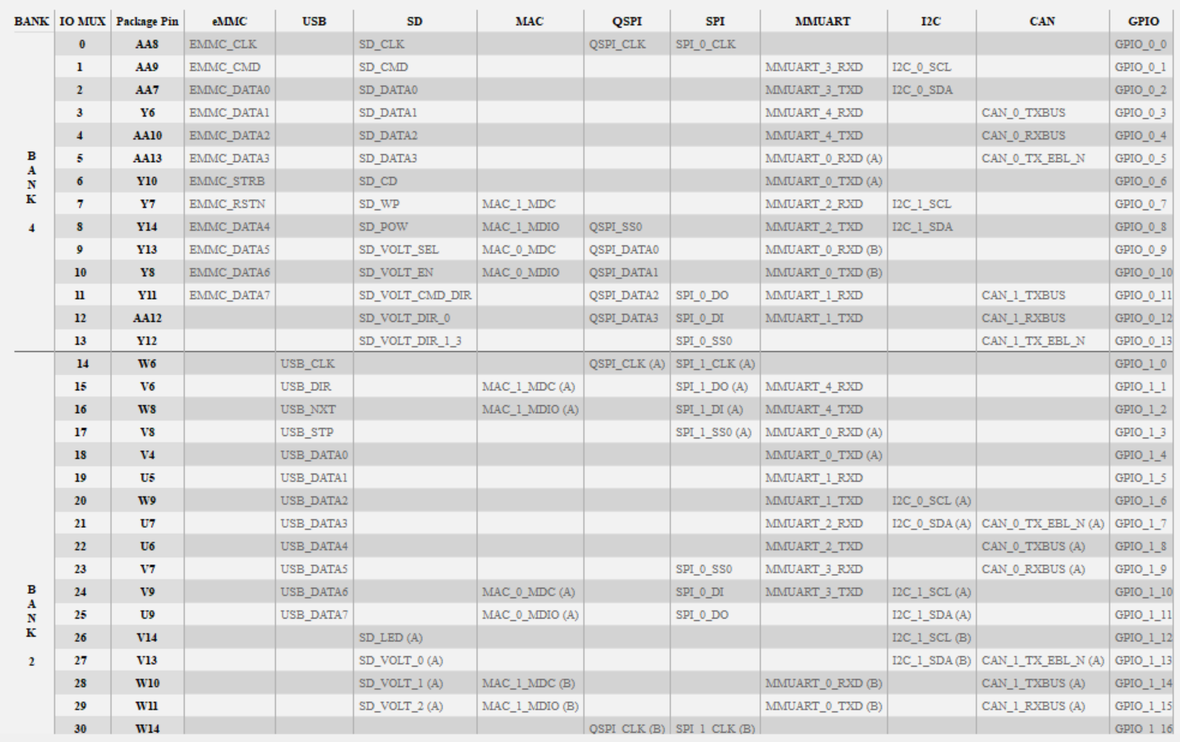
The MSS SGMII I/Os are a dedicated set of pins. Two sets of pins are for transceiver and one set for sourcing the reference clock. The MSS SGMII pins are listed as follows:

- MSS_SGMII_TXP0, MSS_SGMII_TXN0
- MSS_SGMII_RXP0, MSS_SGMII_RXN0
- MSS_SGMII_TXP1, MSS_SGMII_TXN1
- MSS_SGMII_RXP1, MSS_SGMII_RXN1
- MSS_REFCLK_IN_P, MSS_REFCLK_IN_N

1.4.3. MSS-Specific I/O (Ask a Question)

There are 38 MSS I/Os that can be configured using Libero® SoC to interface with various peripherals (see Figure 1-5). For the MSS I/Os pinout information, see PolarFire SoC Packaging Pin Assignment Table. The PPAT lists the MSS I/Os and the peripherals they support. MSS I/Os are configured using Libero SoC > PFSOC_MSS SgCore IP Configurator.

Figure 1-5. Peripherals



BANK	IO MUX	Package Pin	eMMC	USB	SD	MAC	QSPI	SPI	MMUART	I2C	CAN	GPIO
BANK 4	0	AA8	EMMC_CLK		SD_CLK		QSPI_CLK	SPI_0_CLK				GPIO_0_0
	1	AA9	EMMC_CMD		SD_CMD				MMUART_3_RXD	I2C_0_SCL		GPIO_0_1
	2	AA7	EMMC_DATA0		SD_DATA0				MMUART_3_TXD	I2C_0_SDA		GPIO_0_2
	3	Y6	EMMC_DATA1		SD_DATA1				MMUART_4_RXD		CAN_0_TXBUS	GPIO_0_3
	4	AA10	EMMC_DATA2		SD_DATA2				MMUART_4_TXD		CAN_0_RXBUS	GPIO_0_4
	5	AA13	EMMC_DATA3		SD_DATA3				MMUART_0_RXD (A)		CAN_0_TX_EBL_N	GPIO_0_5
	6	Y10	EMMC_STRB		SD_CD				MMUART_0_TXD (A)			GPIO_0_6
	7	Y7	EMMC_RSTN		SD_WP	MAC_1_MDC			MMUART_2_RXD	I2C_1_SCL		GPIO_0_7
	8	Y14	EMMC_DATA4		SD_POW	MAC_1_MDIO	QSPI_SS0		MMUART_2_TXD	I2C_1_SDA		GPIO_0_8
	9	Y13	EMMC_DATA5		SD_VOLT_SEL	MAC_0_MDC	QSPI_DATA0		MMUART_0_RXD (B)			GPIO_0_9
	10	Y8	EMMC_DATA6		SD_VOLT_EN	MAC_0_MDIO	QSPI_DATA1		MMUART_0_TXD (B)			GPIO_0_10
	11	Y11	EMMC_DATA7		SD_VOLT_CMD_DIR		QSPI_DATA2	SPI_0_DO	MMUART_1_RXD		CAN_1_TXBUS	GPIO_0_11
	12	AA12			SD_VOLT_DIR_0		QSPI_DATA3	SPI_0_DI	MMUART_1_TXD		CAN_1_RXBUS	GPIO_0_12
	13	Y12			SD_VOLT_DIR_1_3			SPI_0_SS0			CAN_1_TX_EBL_N	GPIO_0_13
BANK 2	14	W6		USB_CLK			QSPI_CLK (A)	SPI_1_CLK (A)				GPIO_1_0
	15	V6		USB_DIR		MAC_1_MDC (A)		SPI_1_DO (A)	MMUART_4_RXD			GPIO_1_1
	16	W8		USB_NXT		MAC_1_MDIO (A)		SPI_1_DI (A)	MMUART_4_TXD			GPIO_1_2
	17	V8		USB_STP				SPI_1_SS0 (A)	MMUART_0_RXD (A)			GPIO_1_3
	18	V4		USB_DATA0					MMUART_0_TXD (A)			GPIO_1_4
	19	U5		USB_DATA1					MMUART_1_RXD			GPIO_1_5
	20	W9		USB_DATA2					MMUART_1_TXD	I2C_0_SCL (A)		GPIO_1_6
	21	U7		USB_DATA3					MMUART_2_RXD	I2C_0_SDA (A)	CAN_0_TX_EBL_N (A)	GPIO_1_7
	22	U6		USB_DATA4					MMUART_2_TXD		CAN_0_TXBUS (A)	GPIO_1_8
	23	V7		USB_DATA5				SPI_0_SS0	MMUART_3_RXD		CAN_0_RXBUS (A)	GPIO_1_9
	24	V9		USB_DATA6		MAC_0_MDC (A)		SPI_0_DI	MMUART_3_TXD	I2C_1_SCL (A)		GPIO_1_10
	25	U9		USB_DATA7		MAC_0_MDIO (A)		SPI_0_DO		I2C_1_SDA (A)		GPIO_1_11
	26	V14			SD_LED (A)					I2C_1_SCL (B)		GPIO_1_12
	27	V13			SD_VOLT_0 (A)					I2C_1_SDA (B)	CAN_1_TX_EBL_N (A)	GPIO_1_13
	28	W10			SD_VOLT_1 (A)	MAC_1_MDC (B)			MMUART_0_RXD (B)		CAN_1_TXBUS (A)	GPIO_1_14
	29	W11			SD_VOLT_2 (A)	MAC_1_MDIO (B)			MMUART_0_TXD (B)		CAN_1_RXBUS (A)	GPIO_1_15
	30	W14					QSPI_CLK (B)	SPI_1_CLK (B)				GPIO_1_16

1.5. Clocks (Ask a Question)

PolarFire SoC devices offer two on-chip RC oscillators (2 MHz and 160 MHz) to generate free-running clocks. The clocks do not have any I/O pads and do not require external components to operate.

The following table lists the number of RC oscillators available in PolarFire SoC devices.

Table 1-12. RC Oscillator Count

Resource	Supported Range (MHz)	MPFS250
On-chip oscillator	2	1
	160	1

you must understand the regional clock implications when targeting designs that might be migrated to different device sizes. It is important that you go through the pin planning before finalizing it on the board while targeting a die. For more information about clocking in PolarFire devices, see PolarFire Family Clocking Resources User Guide.

For more information about the preferred clock inputs connectivity to PLLs, DLLs, and global clock network, see the Packaging Pin Assignment Table (PPAT) on the PolarFire SoC Documentation web page.

1.6. Reset (Ask a Question)

For designing a robust system, users may use the dedicated DEVRST_N pin or a general purpose reset signal using any GPIO/HSIO as a global system level reset.

For the following cases, the users must use the DEVRST_N as a warm reset for the device:

- A user design modifies auto-initialized fabric RAMs or PCIe configuration during operation.

- A user design is using PCIe, transceivers or user crypto.
  For all other use cases, it is recommended to use a general purpose reset signal using any GPIO/ HSIO IO because they take much shorter time for design to come out of reset.

  If the dedicated DEVRST_N is not used for warm resets, the DEVRST_N pin must be configured using one of the following methods:
- Drive the signal with a POR chip or an external device and keep the DEVRST_N asserted till the system/clocks are stable and the chip is properly powered up.
- Connect DEVRST_N to VDDI3 through a 1 kΩ resistor per pin without sharing with any other pins.
  - In this case, the user needs to ensure that all clocks are stable going to the device before the user design is released from power-on reset. The details of the minimum time taken for the fabric design to be activated after power-on is specified in the Power-Up To Functional section of PolarFire SoC Datasheet.

1.7. DDR Interface Requirements (Ask a Question)

PolarFire SoC devices support DDR3, LPDDR4, LPDDR3, and DDR4. For complete DDR support details, see the PolarFire SoC Datasheet.

DDR interface reliability demands impeccable signal layout and power plane design. You must strictly follow PolarFire SoC Decoupling Capacitors, including precise power coupling capacitor selection. For board layout and routing requirements, see the PolarFire Family Memory Controller User Guide. Non-compliance will result in interface failure.

1.8. Device Programming (Ask a Question)

The PolarFire SoC device can be programmed using one of the two dedicated interfaces: JTAG or SPI. These two interfaces support the following programming modes:

- JTAG programming
- SPI master mode programming
- SPI slave mode programming

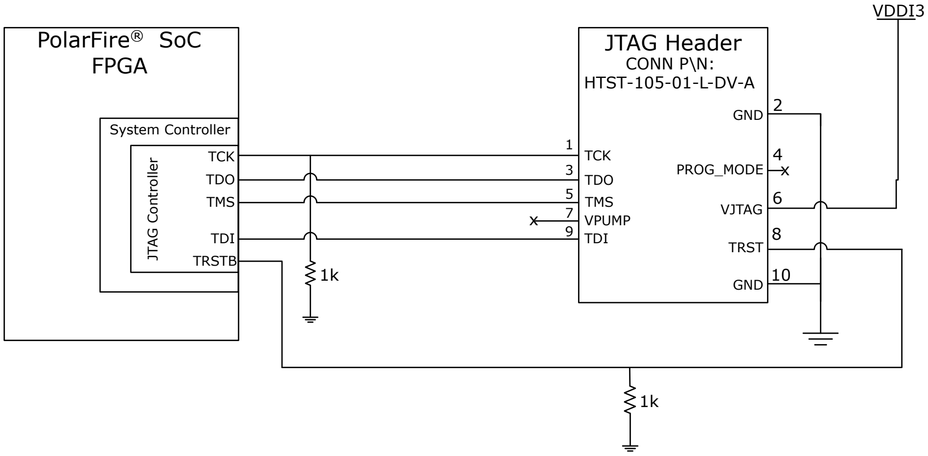
The PolarFire SoC FPGA supports programming modes through an internal system controller using SPI master mode or an external master using JTAG or SPI interfaces. For detailed information on hardware connections for each programming mode, see PolarFire Family Programming User Guide.

1.8.1. JTAG Programming (Ask a Question)

The JTAG interface is used for the device programming and testing, or for debugging the firmware. When the device reset (DEVRST_N) is asserted, JTAG I/Os are not accessible. JTAG I/Os are powered by Bank 3 VDDI.

The following figure shows the board-level connectivity for JTAG programming mode in PolarFire SoC devices.

Figure 1-6. JTAG Programming



The following table lists the JTAG pin names and descriptions.

Table 1-13. JTAG Pins

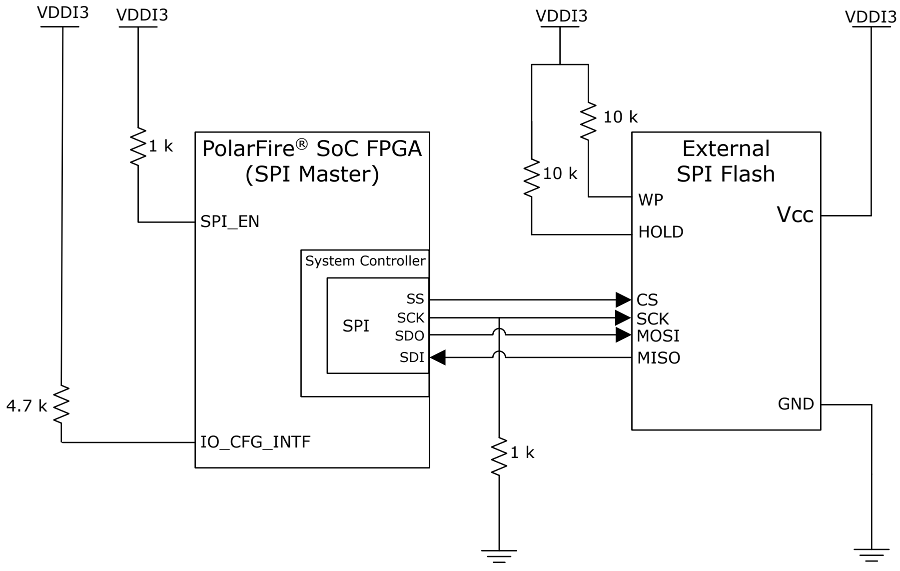
Pin Names	Direction	Unused Condition	Description
TMS	Input	DNC	JTAG test mode select.
TRSTB	Input	Must be connected to VDDI3 through a 1 kΩ resistor.	JTAG test reset. Must be held low during device operation. If JTAG is not used, an external pull-down resistor can be included to ensure that the TAP is held in reset mode.
TDI	Input	DNC	JTAG test data in
TCK	Input	Must be connected to VSS through a 10 kΩ resistor	JTAG test clock
TDO	Output	DNC	JTAG test data out

1.8.2. SPI Master Mode Programming (Ask a Question)

The embedded system controller contains a dedicated SPI block for programming, which can operate in master or slave mode. In master mode, the PolarFire SoC device interfaces are used to download programming data through the external SPI flash. In slave mode, the SPI block communicates with a remote device that initiates download of programming data to the device.

The following figure shows the board-level connectivity for SPI master mode programming in PolarFire SoC devices.

Figure 1-7. SPI Master Mode Programming



The following table lists the SPI master mode programming pins.

Table 1-14. SPI Master Mode Programming Pins

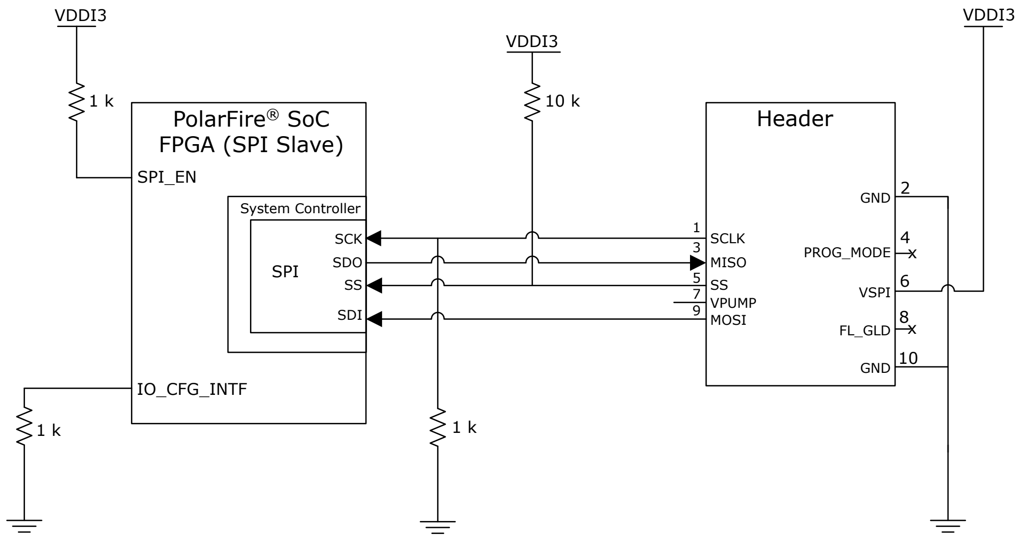
SPI Pin Name	Direction	Unused Condition	Description
SCK	Bidirectional	Connect to VSS through a 10 kΩ resistor	SPI clock.[1]
SS	Bidirectional	Connect to VSS through a 10 kΩ resistor	SPI slave select.[1]
SDI	Input	Connect to VDDI3 through a 10 kΩ resistor	SDI input.[1]
SDO	Output	DNC	SDO output.[1]
SPI_EN	Input	Connect to VSS through a 10 kΩ resistor	SPI enable. 0: SPI output tri-stated 1: Enabled Pulled up or down through a resistor or driven dynamically from an external source to enable or tri-state the SPI I/O.
IO_CFG_INTF	Input	Connect to VSS through a 10 kΩ resistor	SPI I/O configuration. 0: SPI slave interface 1: SPI master interface Pulled up or down through a resistor or driven dynamically from an external source to indicate whether the shared SPI is a master or slave.

(1) The SCK, SS, SDI, and SDO pins are shared between the system controller and the FPGA fabric. When the system controller's SPI is enabled and configured as a master, the system controller hands over the control of the SPI to the fabric (after device power-up).

1.8.3. SPI Slave Mode Programming (Ask a Question)

The following figure shows the board-level connectivity for SPI slave mode programming in PolarFire SoC devices.

Figure 1-8. SPI Slave Mode Programming



1.9. Special Pins (Ask a Question)

For information about special pins, see PolarFire SoC FPGA Packaging and Pin Descriptions User Guide.

1.10. Transceiver (Ask a Question)

Transceiver blocks are located on the east corner of the PolarFire SoC device. PolarFire SoC devices support PCIe interface, which supports only Transceiver quad 0.

For more information about implementing PCIe interfaces, see PolarFire Family PCI Express User Guide. For more information about implementing other transceiver based interfaces and power supplies, see PolarFire Family Transceiver User Guide.

The PolarFire SoC MPFS250T-FCG1152 device includes:

- Four Transceiver Quads (4 Lanes per Quad) - XCVR_[3:0].
- The embedded PCIe controller subsystem (PCIESS) is available only within Quad_0 or XCVR_0 Lane.

For more information about supported I/O standards, see PolarFire Family I/O User Guide.

1.10.1. Reference Clock (Ask a Question)

A transceiver reference clock is delivered to each transmit PLL for transmit functions and to each receiver lane for receive clock data recovery (CDR).

1.10.1.1. Transceiver Reference Clock Requirements (Ask a Question)

The following are requirements for the transceiver reference clock:

- When differential clock input is provided to the reference clock:
  - ODT must be enabled for transceiver reference clock pins.
  - Must be within the range of 20 MHz to 400 MHz.
- Must be within the tolerance range of I/O standards. The reference input buffer is provided and is expected to support these input standards directly without external components on the board. The reference I/O standards such as LVCMOS25, SSTL18, LVDS25, and HCSL25 are supported. For more information, see the “Reference Clock Input Buffer Standards” table in PolarFire Family Transceiver User Guide.

See the *PCI Express Base specification Rev 2.1* for detailed PHY specifications. Also, see the *PCIe Add-in Card Electro-Mechanical (CEM) specifications*.

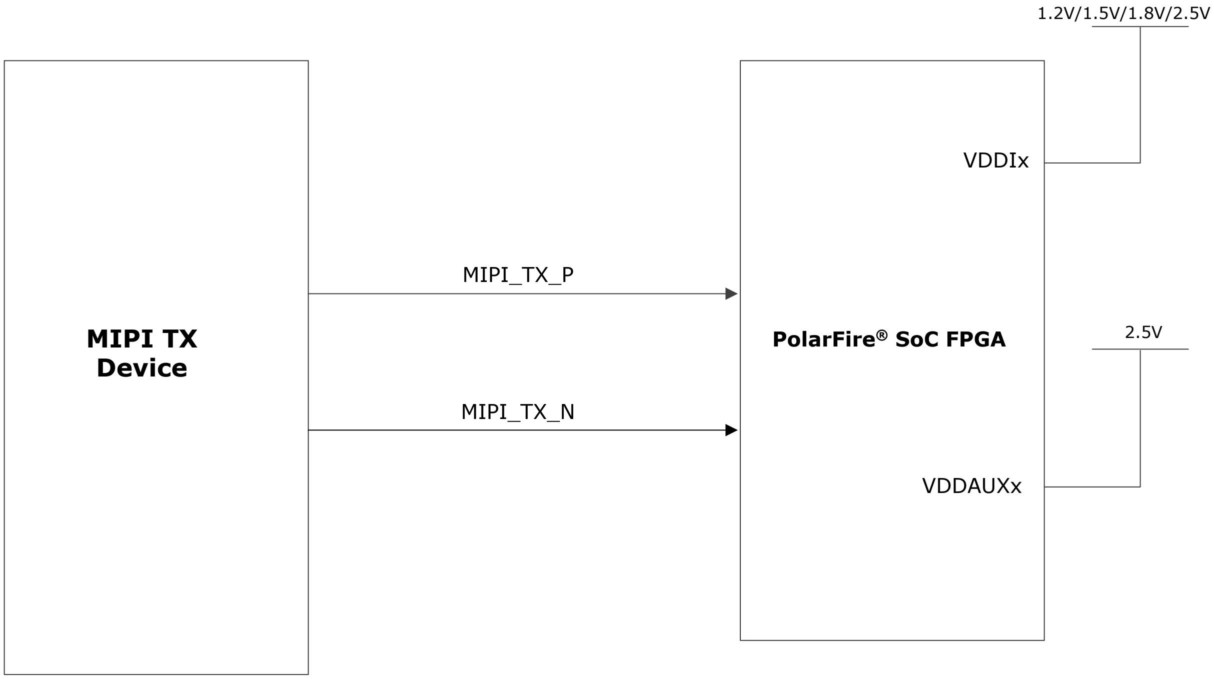
1.11. MIPI Hardware Design Guidelines (Ask a Question)

The following sections discuss the guidelines for MIPI RX and TX interface with PolarFire SoC device.

1.11.1. MIPI RX (Ask a Question)

The MIPI RX is supported only in GPIO Bank. The corresponding Bank voltage (VDDI), and VDDAUX voltage must be connected as shown in the following figure.

Figure 1-9. MIPI RX Connection



MIPI RX signal connections are as follows:

- Four data and clock must be within one DDR_Lane.
- Connect the data signals to adjacent DDR_Lanes, if more than four data signals are available.
- The MIPI RX clock must be connected to a CLKIN pin.

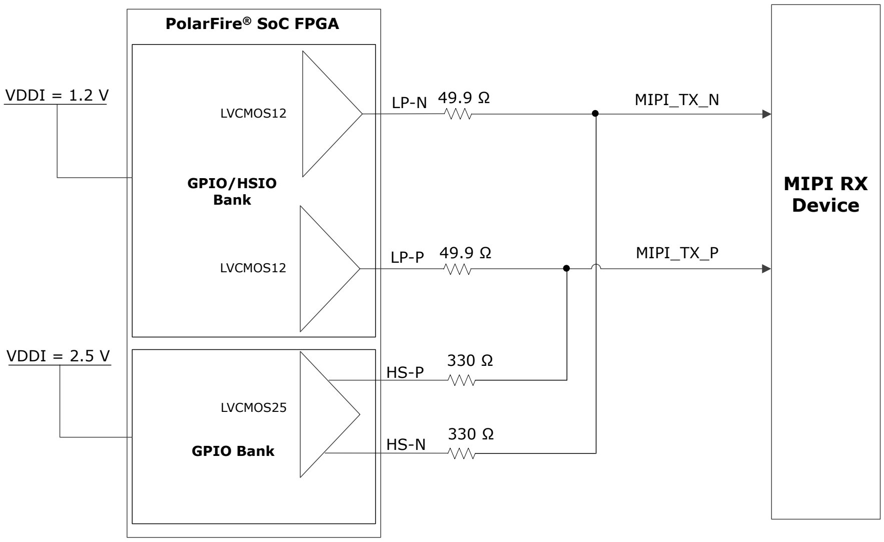
For more information about DDR_Lane, see PolarFire SoC Packaging Pin Assignment Table.

1.11.2. MIPI TX (Ask a Question)

The MIPI Low Power (LP) signals should be connected to a 1.2V GPIO/HSIO Bank supply. High-speed signals should be connected to a 2.5V GPIO Bank supply. Select the HS and LP pins in adjacent pins to minimize the LP stub. The HS data and clock signals should be in one DDR_Lane. For more information about DDR_Lane information, see PolarFire SoC Packaging Pin Assignment Table.

The MIPI TX standard can be implemented by using the resistor divider network for Low Power (LP) and High Speed (HS) signals, as shown in the following figure. The resistor values mentioned in the following provide a throughput upto of 1 Gpbs.

Figure 1-10. MIPI TX Connections



Important: Run the PDC verification in the Libero SoC tool before moving to layout. To know about MIPI RX electrical characteristics, see PolarFire SoC Datasheet.

For information about the MIPI layout guidelines, see MIPI.

1.12. AC and DC Coupling (Ask a Question)

Each transmit channel of a PCIe lane must be AC-coupled to allow link detection. Capacitors used for AC coupling must be external to the device and large enough to avoid excessive low-frequency drops when the data signal contains a long string of consecutive identical bits. For non-PCIe applications, Microchip recommends that a PolarFire SoC device receives inputs that are AC-coupled to prevent common-mode mismatches between devices. Suitable values (for example, 0.1 µF) for AC-coupling capacitors must be used to maximize link signal quality and must conform to PolarFire SoC Datasheet electrical specifications.

For lower data rates as per the datasheet, DC coupling is supported by PolarFire SoC Transceiver Tx and Rx interfaces through a configuration option. If a PolarFire SoC transmitter is used to drive a PolarFire SoC receiver in DC-coupled mode, select the lowest common mode settings for the transmitter.

1.13. Brownout Detection (Ask a Question)

The PolarFire SoC FPGA functionality is guaranteed only if VDD is above the recommended level specified in the Datasheet. Brownout occurs when VDD drops below the minimum recommended operating voltage. When this occurs, the device operation may not be reliable. The design might continue to malfunction even after the supply is brought back to the recommended values because parts of the device might have lost functionality during brownout.

Important: For brownout detection on any PolarFire supply (including VDD, VDD18, and VDD25), use external brownout detection circuits.

2. Board Design Checklist (Ask a Question)

This chapter provides a set of hardware board design checks for designing hardware using Microchip PolarFire SoC FPGAs. The checklists provided in this chapter are a high-level summary checklist to assist the design engineers in the design process.

2.1. Prerequisites (Ask a Question)

Ensure to go through the following before reading this chapter:

- Introduction
- Appendix: General Layout Design Practices

This checklist is intended as a guideline only. The PolarFire SoC family consists of SoC FPGAs ranging from densities of 100K to 400K Logic Elements (LEs).

2.2. Design Checklist (Ask a Question)

The following table lists the various checks that design engineers must take care while designing a system.

Table 2-1. Design Checklist

Guideline	Yes/No	Remarks
Prerequisites		
– See PolarFire SoC Datasheet. – See PolarFire SoC FPGA Packaging and Pin Descriptions User Guide.	—	—
Refer to the board-level schematics of PolarFire SoC Evaluation Kit	—	—
Device Selection		
Check for available device variants for PolarFire SoC FPGA – Select a device based on I/O pin count, transceivers, package, phase-locked loops (PLLs), and speed grade	—	—
Check device errata in PolarFire SoC FPGA Errata	—	—
Design Checklist		
Power Analysis Download the PolarFire Power Estimator and check for the power budget. For more information, see PolarFire and PolarFire SoC FPGA Power Estimator User Guide.	—	—
Power Supply Checklist See Power Supplies for used power rails. See Unused Power Supply and Figure 1-3 for unused rails.	—	—
Decoupling Capacitors Strictly implement the PolarFire SoC Decoupling Capacitors as specified in PolarFire SoC Decoupling Capacitors. Device performance and adherence to datasheet specifications depend entirely on these requirements being met without exception. Any deviation from the specified capacitors requires Power Integrity (PI) analysis.	—	—
Clocks		
For more information about dynamic phase shift ports, see Table 4-4 of PolarFire Family Clocking Resources User Guide. The XCVR reference clock ranges from 20 MHz to 400 MHz.	—	—

Table 2-1. Design Checklist (continued)

Guideline	Yes/No	Remarks
The global clock network can be driven by any of the following: – Preferred clock inputs (CLKIN_z_w) – On-chip oscillators – CCC (PLL/DLL) – XCVR interface clocks High-Speed I/O Clocks High-speed I/O clock networks can be driven by I/O or CCCs. The high-speed I/O clocks can feed reference clock inputs of adjacent CCCs through hardwired connections. **CCC** The CCC can be configured to have a PLL or DLL clock output, driving a high-speed I/O clock network.	—	—
Global buffer (GB) can be driven through the dedicated global I/O, CCC or fabric (regular I/O) routing. The global network is composed of GBs to distribute low-skew clock signals or high-fanout nets. Dedicated global I/O drive the GBs directly and are the primary source for connecting external clock inputs (to minimize the delay) to the internal global clock network. For more information about global clock network, see PolarFire Family Clocking Resources User Guide.	—	—
Reset		
For more information about DEVRST_N and user reset, see Reset.	—	—
DDR Interface		
For more information about DDR routing and topology, see PolarFire Family Memory Controller User Guide.	—	—
Programming and Debugging Scheme For programming and debugging information, see Device Programming.	—	—
XCVR		
For more information about XCVR, see PolarFire Family Transceiver User Guide.	—	—
For I/O gearing interfaces, place the clocks and data based on the defined requirements by selecting the correct I/O. For more information about the placement of User I/O, see PolarFire Family I/O User Guide.	—	—
There is one IO_CFG_INTF pin available, which can be used as input.	—	—
See the bank location diagrams in the PolarFire SoC FPGA Packaging and Pin Descriptions User Guide to assess the preliminary placement of major components on PCB.	—	—

2.3. Layout Checklist (Ask a Question)

The following table lists the layout checklist.

Table 2-2. Layout Checklist

Guideline	Yes/No
Power	
Are the 0402 or lesser size capacitors used for all decoupling capacitors?	—
Is the required copper shape provided to core voltage?	—
Are the required copper shape and sufficient vias provided to voltages?	—
Are VREF planes for the DDRx reference supply isolated from the noisy planes?	—
Is the VTT plane width sufficient?	—
DDR Memories	
Is the length-match recommended by vendor followed for DDR memories? Are the traces with the correct controlled impedance required for DDR memories?	—
XCVR	
Are the length-match recommendations for XCVR followed?	—
Are DC blocking capacitors required for PCIe interface?	—
Is tight-controlled impedance maintained along the XCVR traces?	—
Are differential vias well designed to match XCVR trace impedance?	—
Are DC blocking capacitor pads designed to match XCVR trace impedance?	—
Dielectric Material	
Is proper PCB material selected for critical layers?	—

3. Appendix: General Layout Design Practices (Ask a Question)

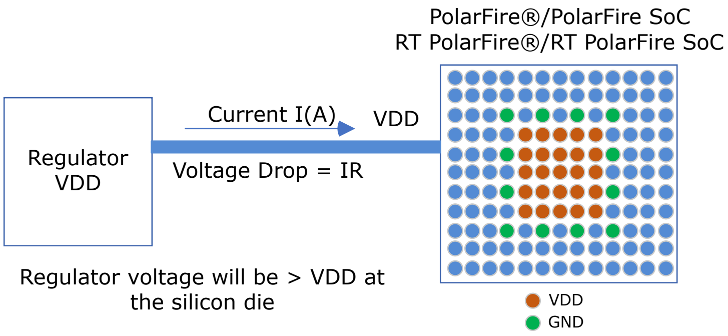
This chapter provides guidelines for the hardware board layout that incorporates PolarFire SoC devices. The guidelines mentioned in this document act as a supplement to the standard board-level layout practices.

This chapter is intended for readers who are familiar with the PolarFire SoC FPGA chip, experience in digital board layout, and know about line theory and signal integrity.

3.1. Powering Core VDD (Ask a Question)

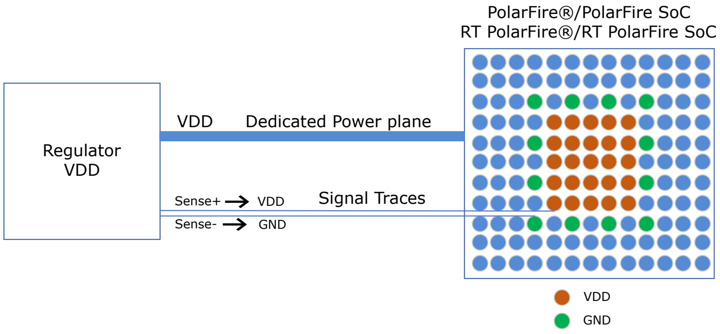
The PolarFire product family requires the VDD to meet a tight tolerant specification for min/max, per the datasheet. To ensure this is designed correctly, users can use standard regulators placed very close to the device, with good layout practices, so the IR drop of the VDD power rail is very minimal. If the regulator is kept further away and a higher IR drop is suspected (especially with high current consumption), it is a good practice to use a regulator which supports closed loop compensation with sense line detectors to power the VDD. This allows the regulator to compensate for the IR drop being seen by silicon, if the current consumption is high.

Figure 3-1. Powering VDD with Standard Regulator



If the regulator is kept further away, the sense lines from the silicon can be fed back to the regulator to compensate for the IR drop by the regulator. This is done by regulators which support closed loop compensation and remote sensing. In this design, the sense lines need to be routed as signal traces back to the regulator. They can be routed as loosely coupled differential transmission lines.

Figure 3-2. Powering VDD with Regulator Supporting Closed Loop Compensation with Remote Sensing



Note: Always follow the sense line recommendations from the VRM vendors.

3.2. MIPI (Ask a Question)

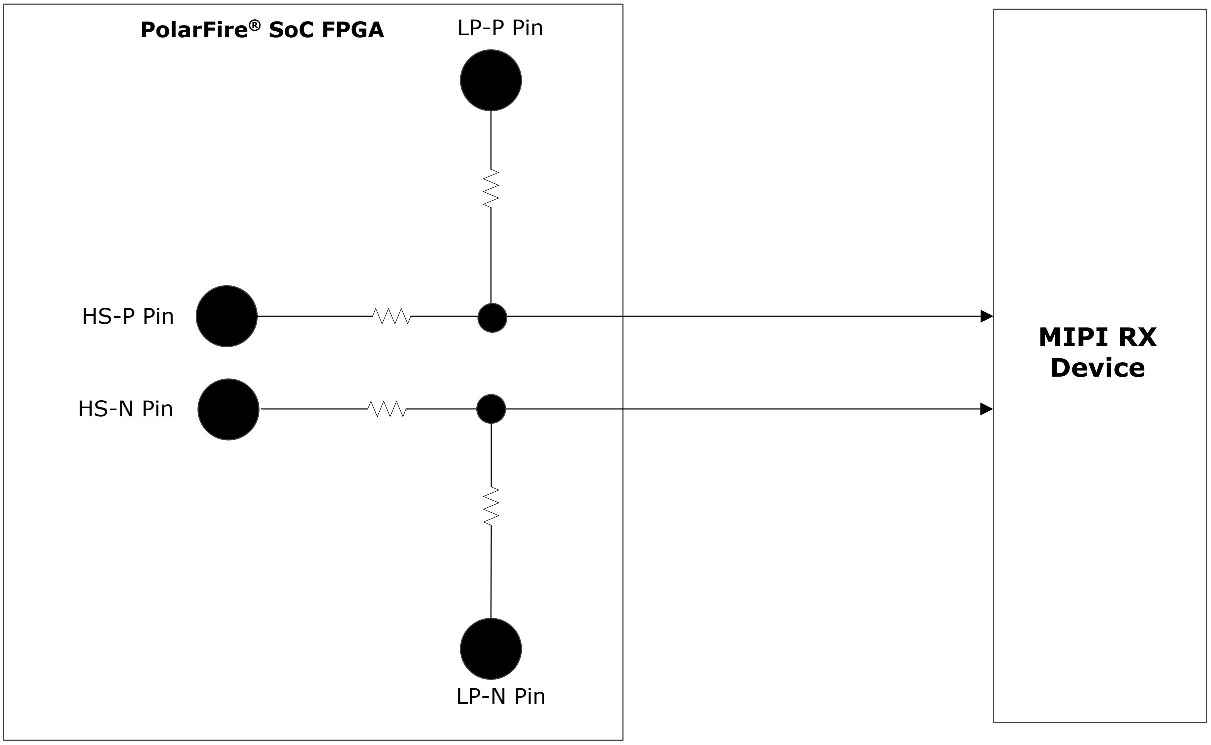
MIPI RX Layout Guidelines:

The data and clock must be matched within 20 mils in PCB.

MIPI TX Layout Guidelines:

As shown in Figure 3-3, the LP and HS resistors must be close to the PolarFire SoC device pin. The HS signals should be routed to LP resistors to minimize the LP signals PCB stub length. The LP signals stub should be less than 500 mils. The data lane and clock should be length matched within 20 mils. Eight inches are the maximum length supported.

Figure 3-3. MIPI TX Layout



3.3. Transceiver (Ask a Question)

Transceivers are high-speed serial connectivity with built-in, multi-gigabit, and multi-protocol transceivers from 250 Mbps to 12.7 Gbps. For these transceiver-based interfaces, the system designer must be familiar with the industry specifications, transceivers technology, or RF/microwave PCB design. However, the PCB design can be evaluated by a knowledgeable high-speed digital PCB designer.

3.3.1. Layout Considerations (Ask a Question)

This section describes differential traces and skew matching, which must be taken care while designing the PCB layout.

3.3.1.1. Differential Traces (Ask a Question)

A well-designed differential trace must have the following qualities:

- No mismatch in impedance
- Insertion loss and return loss
- Skew within the differential traces

The following points must be considered while routing the high-speed differential traces to meet the previous qualities.

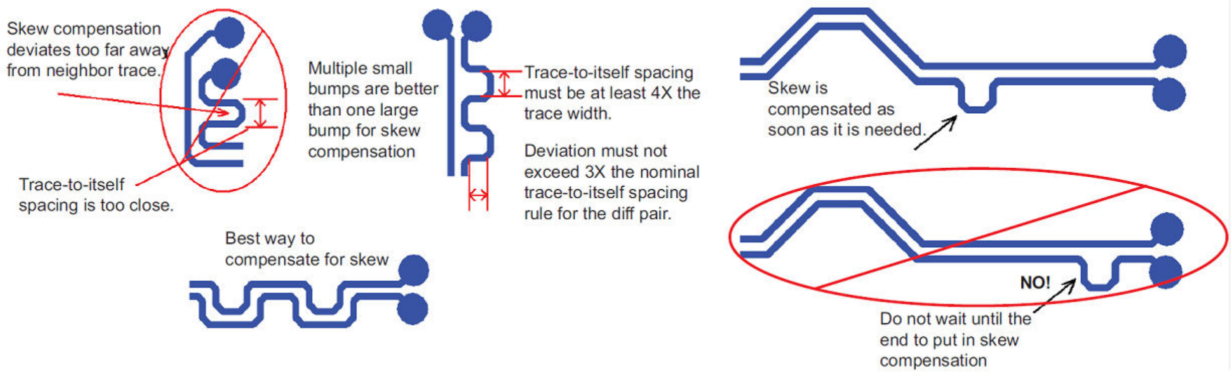
- The traces should be routed with tight length matching (skew) within differential traces. Asymmetry in length causes conversion of differential signals in Common mode signals.
- The differential pair should be routed such that the skew within differential pairs is less than 5 mils. The length match should be used by matching techniques.

3.3.1.2. Skew Matching (Ask a Question)

The length of differential lanes should be matched within the TX and RX group. This applies only to specific protocols such as XAUI.

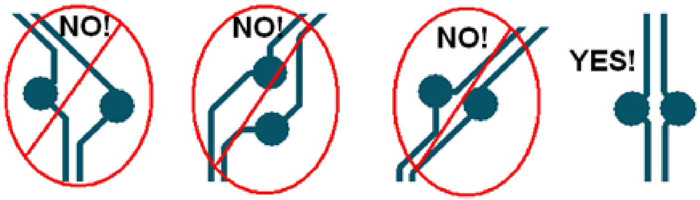
The following figure shows the skew matching.

Figure 3-4. Skew Matching



Differential pairs should be routed symmetrically in-to and out of structures, as shown in the following figure.

Figure 3-5. Example of Asymmetric and Symmetric Differential Pairs Structure



Skin effect dominates as the speed increases. To reduce the skin effect, the width of the trace must be increased (loosely coupled differential traces). Increase in trace width causes increase in dielectric losses. To minimize dielectric loss, use low dissipation factor (DF) PCB materials such as Nelco 4000-13EP SI. Cost is significantly higher than FR4 PCB material, but FR4 PCB material cannot provide increased eye-opening when longer trace interconnections are required. Ensure that a 85 - 100 Ω differential impedance is maintained. This is an important guideline to be followed if the data rate is 5 Gbps or higher.

Far end crosstalk is eliminated by using stripline routing. However, this type of routing in stripline causes more dielectric loss. In order to minimize dielectric loss, it is better to route as a microstrip if there is enough space between differential pairs (>4 times the width of the conductor). Simulations are recommended to see the best possible routing.

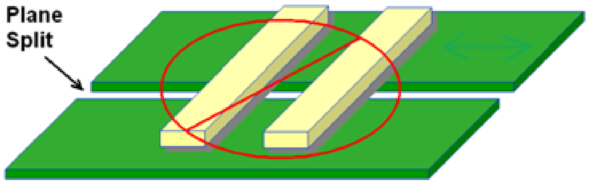
Instruct the fabrication vendor to use these PCB materials before manufacturing.

Transceiver traces must be kept away from the aggressive nets or clock traces. For example, on MPF300 devices, the transceiver and DDR traces should not be adjacent to each other. Trace stubs must be avoided.

It is recommended to use low roughness, that is, smooth copper. As the speed increases, insertion loss due to the copper roughness increases. The attenuation due to skin effect is increased proportional to the square root of frequency. Microchip recommends instructing the PCB fabrication house to use smooth copper, if the frequency exceeds 2 Gbps.

Split reference planes should be avoided. Ground planes must be used for reference for all transceiver lanes.

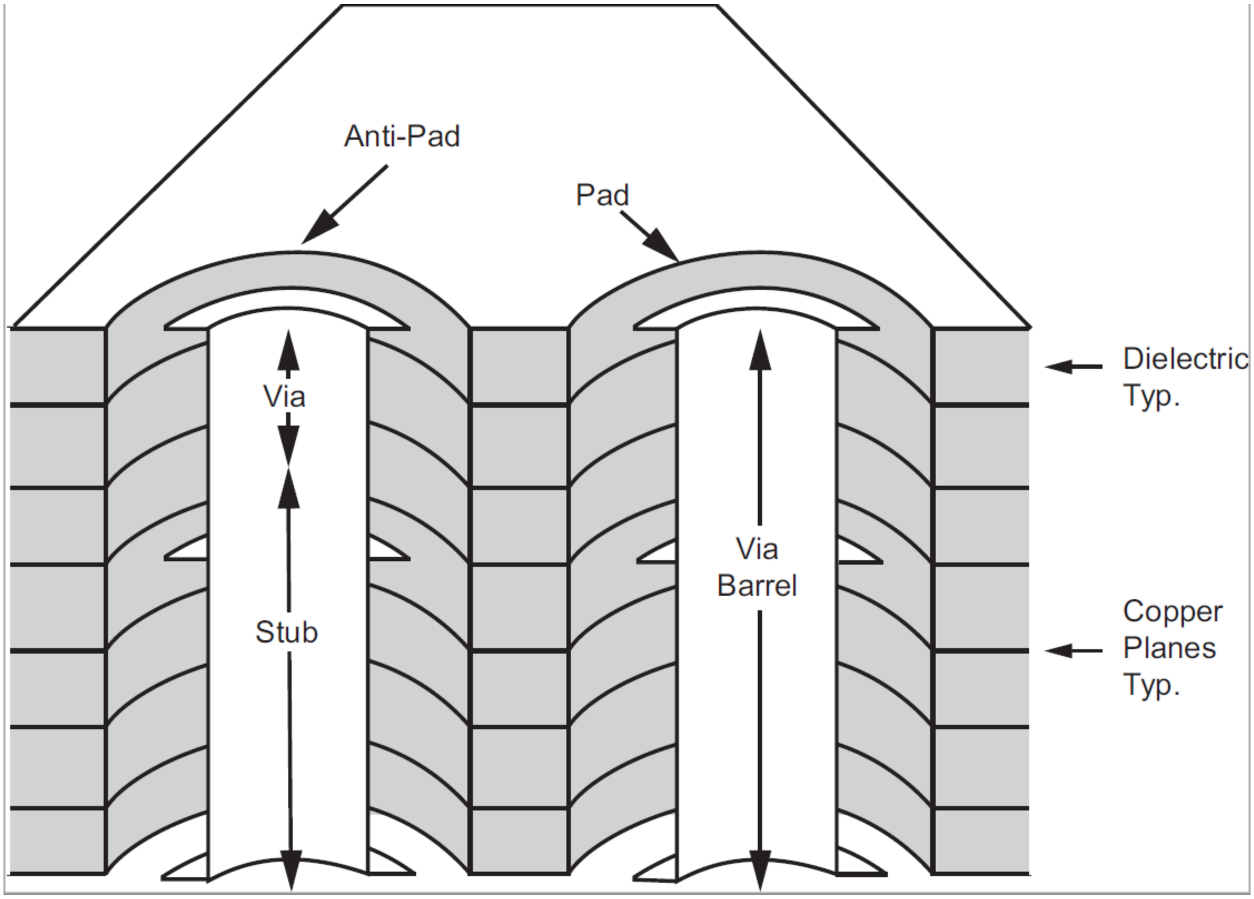
Figure 3-6. Ground Planes for Reference



3.3.1.3. Via (Ask a Question)

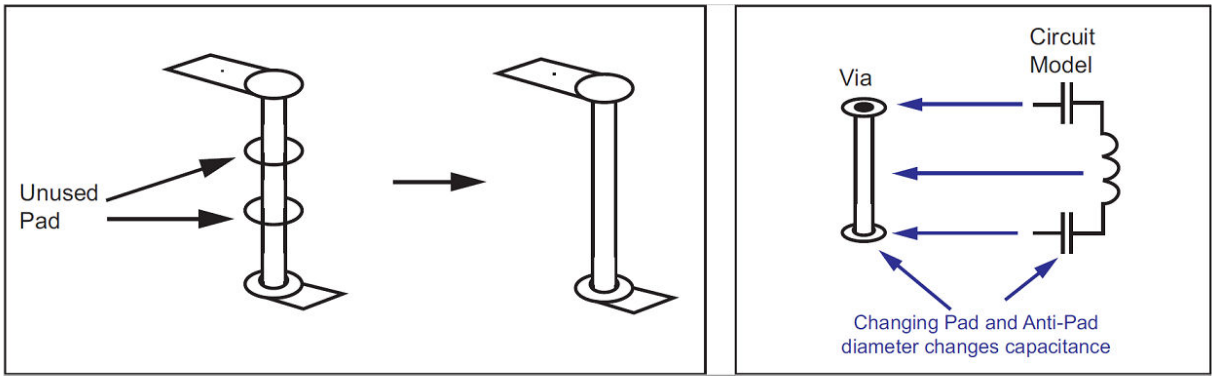
The target impedance of vias is designed by adjusting the pad clearance (anti-pad size). Field solver should be used to optimize the via according to the stack-up.

Figure 3-7. Via Illustration



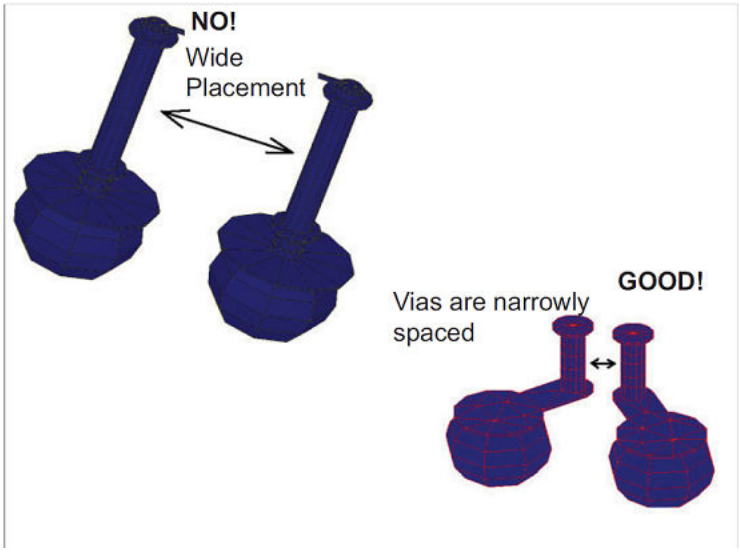
- Many vias on different traces should be avoided or minimized as much as possible.
- The length of via stubs should be minimized by back-drilling the vias, routing signals from the near-top to the near-bottom layer, or using blind or buried vias. Using blind-vias and back drilling are good methods to eliminate via stubs and reduce reflections.
- If feasible, non-functional pads should be removed. Non-functional pads on-via are the pads where no trace is connected. This reduces the via capacitance and stub effect of pads.

Figure 3-8. Non-Functional Pads of Via



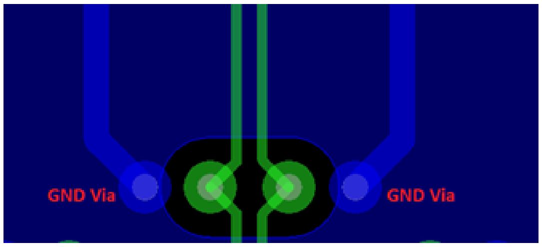
Using tight via-to-via pitches helps reducing the effect of crosstalk, as shown in the following figure.

Figure 3-9. Via-to-Via Pitch



Symmetrical ground vias (return vias) should be used to reduce discontinuity for Common mode signal components, as shown in the following figure. Common mode of part of the signal requires continuous return path for TX and RX to GND. Return vias help maintain the continuity.

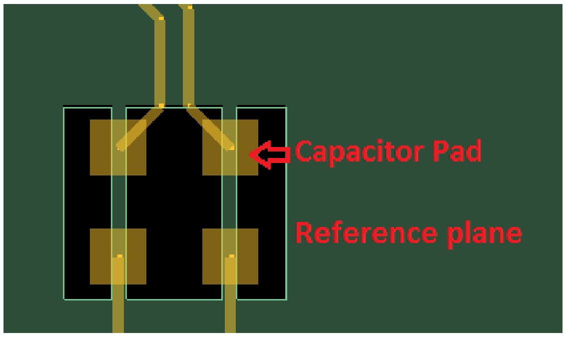
Figure 3-10. GND Via or Return Via



3.3.2. DC Blocking Capacitors (Ask a Question)

The plane underneath the pads of DC blocking capacitors should be removed, as shown in the following figure, to match the impedance of the pad to 50Ω.

Figure 3-11. Capacitor Pad Reference Plane



4. Revision History (Ask a Question)

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the current publication.

Revision	Date	Description
H	06/2026	The following is a summary of changes made in this revision: • Made the following updates in PolarFire SoC Decoupling Capacitors: – Added "MPFS025TS" to the table title of Table 1-4 as the same decoupling capacitors are required for MPFS025TS-FCVG484. – Removed "MPFS025TS" from Table 1-6 as the FCVG784 package does not support the MPFS025TS device. • Added a note to the I/O Glitch section.
G	03/2026	The following is a summary of changes made in this revision: • The following changes were made in the Power Supplies section: – Added a note for VDDIO (MSS DDR Bank 6) and XCVR_VREF under Figure 1-1. – Updated a note to update the supply requirement information for VDDA, VDD, and VDDI5 and to add a footnote for VDDI3 . – Updated a note to update the information on VDD, VDD18, and VDD25 monotonic ramp by clearly stating the monotonic ramp of these power supplies must be followed strictly. • The following changes were made in the PolarFire SoC Decoupling Capacitors section: – Updated the introductory paragraph to clearly state that the decoupling capacitors list must be followed strictly. – Updated the information on the guidelines to use alternative decoupling capacitor parts other than those listed in Table 1-8. • Added a note in the User I/O section to cross-reference the Cold Sparing section. • Made the following changes in the Cold Sparing section: – Added cold sparing recommendations on GPIOs. – Updated the supply connection of VDDI3 in Figure 1-4. • Updated the DDR Interface Requirements section. • Updated the Table 2-1 in the Design Checklist section for decoupling capacitors. • Updated the Table 2-2 in the Layout Checklist section for DDR memories. • Added the Powering Core VDD section.
F	08/2024	The following is a summary of changes made in this revision. • Following changes have been made in Table 1-8: – Updated the decoupling capacitor part number for 2.2 nF. – Added the decoupling capacitor part numbers for 1 µF and 47 nF. • Added a note under Table 1-1 to clarify the VDDI5 power-up sequence. • Removed instances of SPI_EN and IO_CFG_INTF pins from Figure 1-6 in JTAG Programming section as they are not used during JTAG programming. • Updated Brownout Detection for a note related to the brownout detection on any PolarFire supply.

Revision History (continued)

Revision	Date	Description
E	11/2023	The following is a summary of changes made in this revision. • Updated Figure 1-1 and Figure 1-3 by changing the power supply name from “VDDIO (MSS SGMII Bank 5)” to “VDDI5”. • Revised information regarding the VDDI5 power supply. See Table 1-1. • Changed the number of 47 μF decoupling capacitors to be used for VDDA25 in Table 1-5. • Updated Figure 1-2 by changing the power supply name from “VDDI Bank 5 (MSS SGMII)” to “VDDI5”. • Revised a note about GPIO glitch during JTAG programming. See I/O Glitch. • Substituted Figure 1-5 with a high-quality image.
D	10/2023	The following is a summary of changes made in this revision. • Updated Power Supplies as follows: – Added information about target impedance. – Updated Figure 1-1 by adding operating voltage 1.1V to VDDIO (MSS DDR Bank 6). – Added a note describing that the 1.1V operating voltage for VDDIO (MSS DDR Bank 6) is for the LPDDR4 support. Also, added a link to PolarFire Family Memory Controller User Guide. • Updated PolarFire SoC Decoupling Capacitors as follows: – Added power supply decoupling capacitor details for MPFS460TS - FCG1152 and MPFS095TS/MPFS025TS - FCS325 devices. – Updated the power supply decoupling capacitor details for MPFS250TS/ MPFS160TS/MPFS095TS - FCG1152, FCSG536, FCVG484, and FCVG784 devices. • Added a note about GPIO glitch during JTAG programming. See I/O Glitch. • Replaced “VDDSREF” with “VDD_XCVR_CLK” throughout all the decoupling capacitors tables in PolarFire SoC Decoupling Capacitors. • Added Table 1-5 and Table 1-6. • Updated the unused condition of VDDI Bank 5 (MSS SGMII) to 2.5/3.3V in Figure 1-2.
C	05/2022	The following is a summary of changes made in this revision. • In Power Supplies, added a note about power sequencing requirement for I/O calibration. • Updated I/O Glitch. • Updated Clocks to highlight regional clock implications while migrating designs to different device sizes. • Updated Figure 1-9. • Added a note about hot socketing exceptions in Hot Socketing (GPIO Only). • Added link to PPAT in Clocks for preferred clock inputs connectivity to PLLs, DLLs, and global clock network. • Enabled ‘Ask A Question’ hyperlink for each section in the document.
B	10/2021	The following is a summary of changes made in this revision. • Updated Table 1-9 for power-up and power-down sequencing requirements for mitigating I/O glitch. • Added recommended 1 nF, 2.2 nF, 10 nF, and 0.1 μF decoupling capacitors of the 0402 size for the 1 mm package. See Table 1-8. • Added more information in new footnotes for VDD and VDDA in Table 1-1. • Added footnotes for all decoupling capacitor tables in PolarFire SoC Decoupling Capacitors to specify the objective of decoupling capacitors.

Revision History (continued)

Revision	Date	Description
A	01/2021	The following is a summary of changes made in this revision. • Updated 1.2 I/O Glitch. • Updated 1.1.2 Unused Power Supply. • Migrated this document from Microsemi format to Microchip format. Document number is changed from 50200901 to DS60001681A
1.0	—	The first publication of this document.

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