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RT54SX T_r / T_f Experiment

July 08, 2002

BY

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DATE: **July 08, 2002**

DEVICE TYPE:	RT54SX16-CQ256E	RT54SX32-CQ208P
WAFER LOT CODES:	T6HP12	T6JP04
DATE CODE:	0019	0217
NUMBER OF UNITS:	2	2

Table 1 – RTSX Device Type Information

1. ISSUE

Actel understands that customers may have difficulty meeting the 50ns T_r and T_f specification of the RT54SX devices for certain applications (see Note 1, Electrical Specifications). As reported by customers in their application of RT54SX programmed parts the maximum fall transition time specification could exceed the limits of the Actel data book for these parts (See Note 2 and 3 for other discussions on this). This may occur during a bus tri-state operation where there is no active pull up or pull down of the bus voltage and only a passive resistor of large value (~100 KΩ) to ground to discharge the bus. In this type of application, the only concern will be when the customer design has implemented an input or bi-directional user I/O function connected to the bus. The tri-state buffer implementation (output drive only) in an RT54SX device disables the input buffer and will not be a concern. With a corresponding large bus capacitance (~2700pF) the resulting fall times for input pins from the tri-stated bus operation on these or any similar Actel parts would be on the order of 500µs, exceeding the specified 50ns maximum transition time. There may be concerns for functionality issues during the tri-state conditions as well as long-term reliability concerns. This report summarizes the findings of fall time experiments completed to determine any potential reliability issues with slow fall times.

2. EXPERIMENT

In order to study the potential reliability issues Actel programmed two each RT54SX16 and RT54SX32 units with the different I/O buffer configurations available. The specific device type is shown in Table 1. A mix of LVTTL and CMOS I/Os were configured in order to test the effects of slow fall times on each of the available I/Os (See Note 1). Included in this experiment were multipurpose I/Os TDI, TCK, TDO and PRB in order to determine if these selectable I/Os are sensitive to slow transitions. In addition, clock inputs CLKB and HCLK were programmed into the design since these networks will have large internal capacitive loads that could draw heavy currents during oscillatory switching conditions. These clocks were driven by external jumper connections from one of the standard I/O pins. All units were programmed for 3.3V I/O operation. Table 2 lists the pin configurations for the RT54SX16 and RT54SX32 units. The internal array (Vcca) was biased at 3.6 volts and Vccr was set to 5.5 volts. External RC networks consisting of a 100KΩ resistor in parallel with a 2700pF capacitor created slow fall time signals on the order of 500µs. An I/O output buffer is first enabled to charge the RC network to Vcci, and then tri-stated, allowing the RC network to control the subsequent fall time.

With reference to Figure 1 and Figure 2, a total of ten I/Os were incorporated into the experimental designs, two additional from the earlier SX-S experiment described in Note 3. The direction of each I/O is controlled via a low speed 500Hz clock signal. A multiplexer selects between either the low speed clock signal or an asserted active low reset signal. The reset signal allows all RC networks to be discharged during initialization. After initialization each alternate cycle of the external clock switches the I/O from input mode (tri-stated) to output mode. The I/Os are further configured in pairs, whereby the output of an input buffer is directed through an internal logic array inverter to the input of another I/O buffer. This design allows for monitoring the effect of a

slow fall times on internal logic module circuits and subsequent input buffers. On any given cycle of the clock, half of the I/Os are acting as input buffers. The charge will decay from the external capacitor and the signal will approach the input threshold transition region. The logic propagates through the I/O input buffer and through an inverter into the other half of the I/O buffers, which are now acting as output drivers charging the external capacitor for the next half of the clock cycle. When the clock input changes state the role of each I/O buffer reverses, I/Os previously set as drivers are now tri-stated and behave as input buffers.

Note 1: *http://www.actel.com/docs/datasheets/RTSXDS.pdf*

Note 2: *http://www.actel.com/appnotes/SchmittTrigger.pdf*

Note 3*:* *http://www.actel.com/products/aero/misc/rtsxs_trtf_report.pdf*

Table 2 Summary of RT54SX16 I/O Configurations

PORT NAME	MACRO CELL	PIN # RTSX16	PIN # RTSX32	I/O LEVEL	I/O TYPE
Io_test1	ADLIB:BIBUF	2	2	LVTTL	TDI- I/O
Io_test2	ADLIB:BIBUF	256	208	CMOS*	TCLK - I/O
Io_test3	ADLIB:BIBUF	18	18	LVTTL	I/O
Io_test4	ADLIB:BIBUF	150	150	CMOS*	I/O
Io_test5	ADLIB:BIBUF	33	33	LVTTL	I/O
Io_test6	ADLIB:BIBUF	134	134	CMOS*	I/O
Io_test7	ADLIB:BIBUF	44	44	LVTTL	I/O
Io_test8	ADLIB:BIBUF	126	103	CMOS*	TDO – I/O
Io_test9	ADLIB:BIBUF	72	67	LVTTL	
Io_test10	ADLIB:BIBUF	90	76	CMOS*	PRB - I/O
Ref_in	ADLIB:INBUF	55	55	- -	
Ref_out	ADLIB:OUTBUF	58	58	LVTTL	
Resetn	ADLIB:INBUF	154	154	- -	
Switch	ADLIB:INBUF	219	180	- -	
CLOCKB	ADLIB:CLKBUFR	220	180	- -	
HCLOCK	ADLIB:HCLKBUF	96	82	- -	

* Supports 5.0 Volt input signals with 3.3 Volt output drive

The four programmed units were then subjected to a 125°C dynamic burn-in with the RC networks in place. Burn-in time for the units was 164 hours.

Figure 1 - RT54SX32 Fall Time Experiment Burn-in Schematic

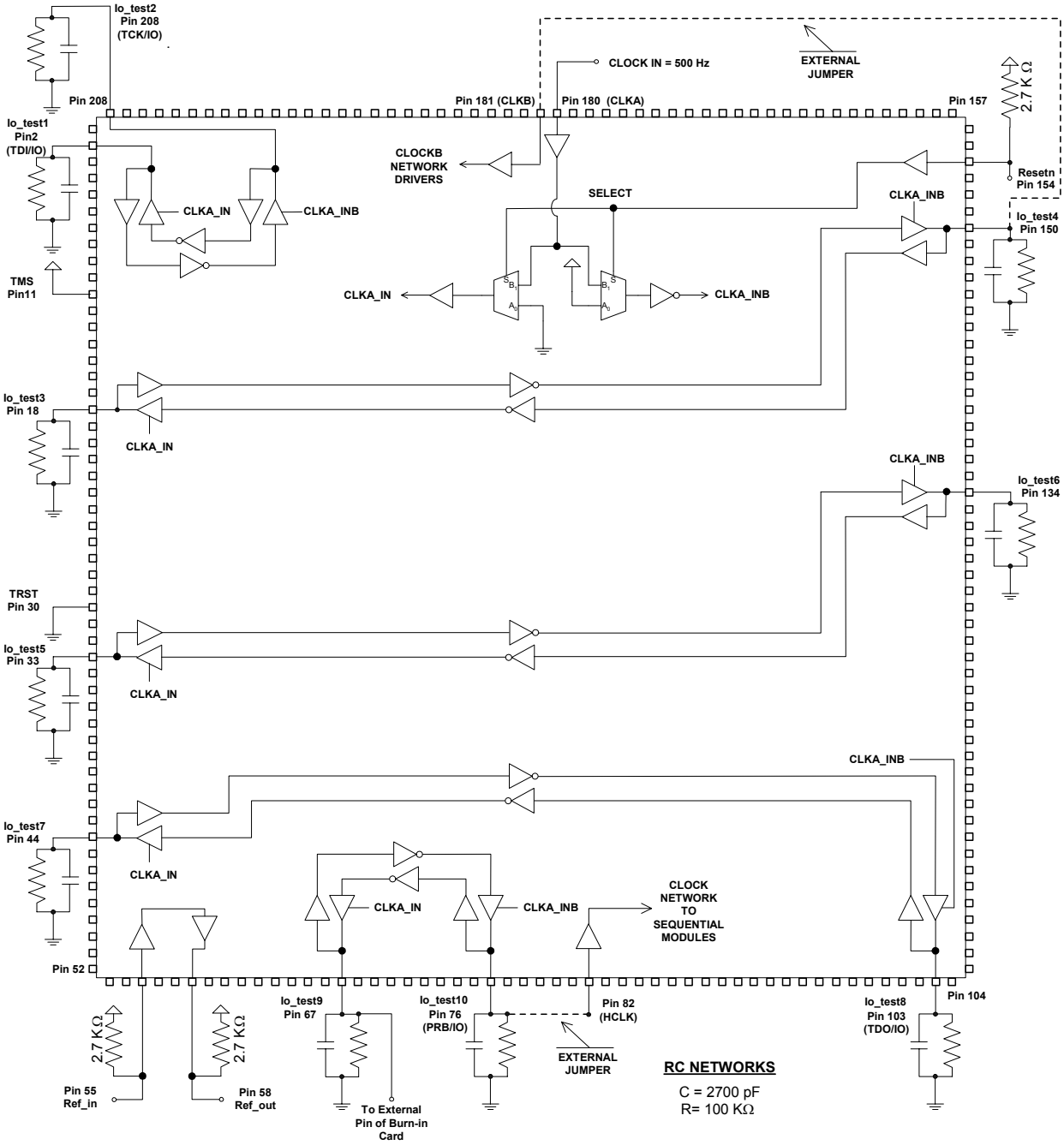
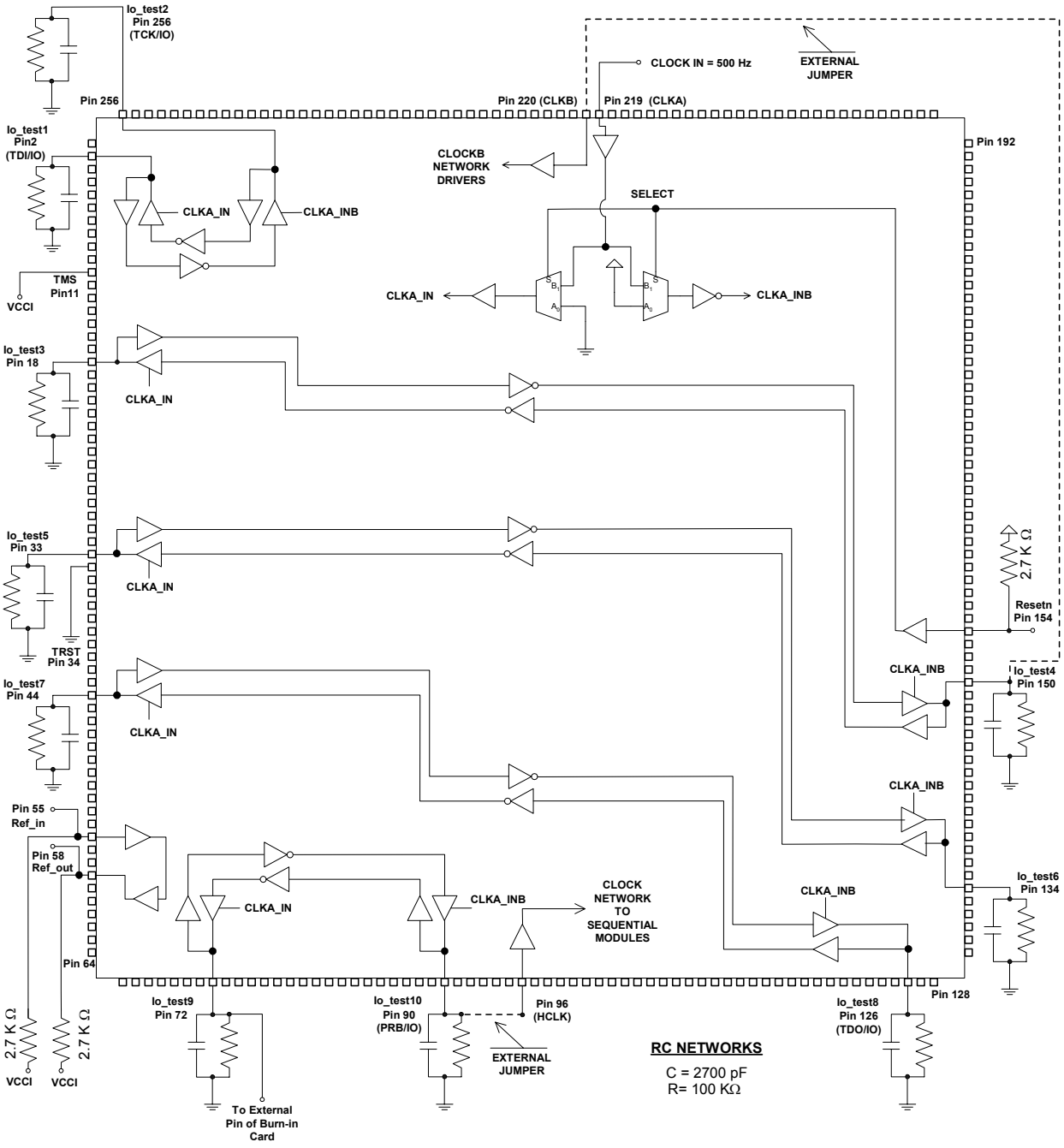


Figure 2 - RT54SX16 Fall Time Experiment Burn-in Schematic



3. Results

Prior to burn-in I/O signals were verified operational on all four units. In addition, logic thresholds on all inputs were measured with the intent to use the threshold as an indicator of stability in transistor device characteristics during burn-in. The Vcci currents were monitored both pre and post burn-in. Since driving the clock networks CLKB and HCLK adds additional dynamic switching, currents were monitored for clock disabled and clocks enabled. For a disabled clock, the resulting static currents for all units cases were less than 0.1 mA. With the 500 Hz clock enabled, currents increase to slightly under 30 mA for the RTSX16 units and just under 8 mA for the RTSX32 units. The differences in dynamic currents between the RTSX16 and RTSX32 units are attributed to the effects of external wiring layouts and test sockets. There was less than +/- 0.1 mA change in current overall from pre to post burn-in, most probably measurement differences. Input logic switching thresholds were monitored by manually increasing the input voltages to the I/O acting as an input buffer while monitoring its corresponding I/O that is set as an output buffer. Once the input buffer threshold is achieved, the output would start to oscillate, as expected. Threshold switching voltages for all I/Os were in the range of 1.42 to 1.50 volts. The post burn-in threshold switching voltages ranges remained in the same range, with differences of 50 mV observed. Since this measurement is very sensitive to wiring, most of delta differences are most likely measurement related. An interesting aspect of this measurement was the observation of a hysterisis effect. When the input voltage was rising, once oscillations commenced, they would continue for approximately 0.2 volts beyond the trigger point. However lowering the input voltage would cause the oscillations to continue below the initial trigger point by about 0.1 volts.

Each I/O toggles with relatively fast rise times and slow fall times created by the RC load, as can be seen in the captured scope waveforms in Figure 3 and

Figure 4 from the programmed devices post burn-in. In the first photo (Figure 3), note on the rising edge of the input clock (Green signal) an I/O is tri-stated (Purple signal) with the fall time determined by the RC time constant. This signal is routed to another I/O (not shown) via an internal inverter, which then switches to an active high at about half of Vcci on its input. Note in the expanded waveform (Figure 4), there are about 30 microseconds of oscillation on the rising edge of the waveform. This is a direct result of the slowly falling input signal remaining a long time in the I/O buffer transition region where both P-channel and N-channel devices are conducting. Slight changes in currents result in small changes in voltages, which sets up oscillatory conditions until the input signal falls below the point where both transistors are conducting heavily. It is this region of oscillation that could be of concern as this is the point of maximum conduction. From the waveform it is most likely that there would be **"logic upsets"** occurring during this transition time however as the burn-in results indicates, there were no circuit failures or large increases in standby or dynamic currents found.

Figure 3 Waveforms of input clock & I/Os under test

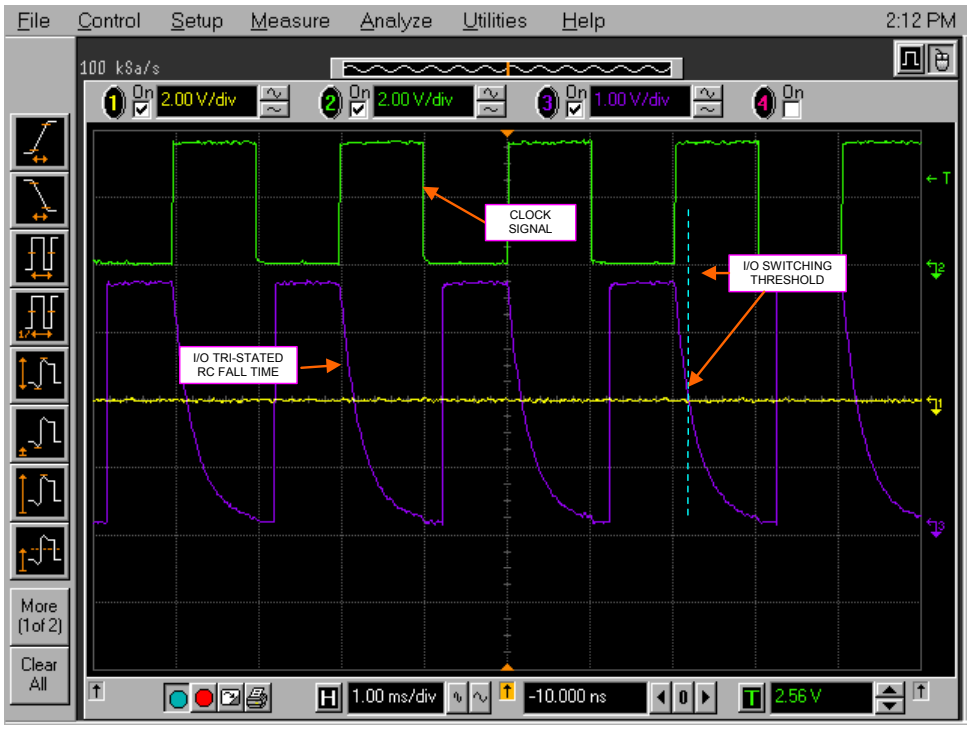
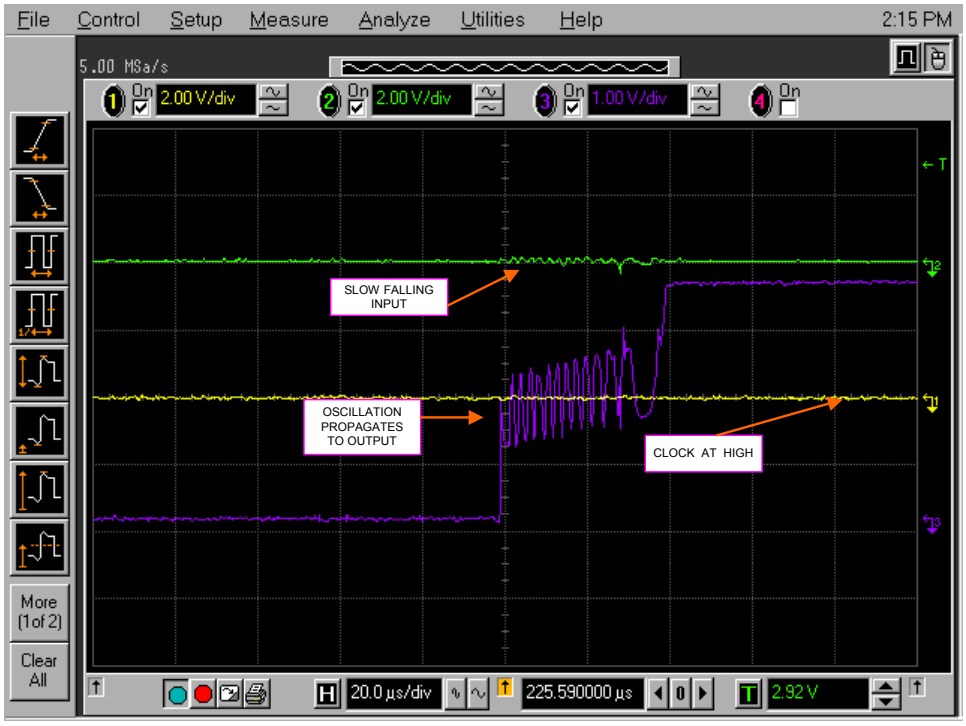


Figure 4 Expanded waveform of input clock & I/Os under test



4. ELECTRO-MIGRATION (EM) ANALYSIS:

A slow falling (or rising) input signal to an I/O buffer may lead to high currents in the input circuitry, therefore an examination was made to determine the possibility of electro-migration conditions. In examining the waveform photos of Figure 3 and Figure 4 there are time periods during the slow falling input signal (or a rising signal) in which the signal is oscillating and remains in the transition region for several microseconds. During this oscillatory time, current flowing in the input buffer drivers, as well as through subsequent logic circuitry, are at or near their peak values.

The previous RTSX-S report (See Note 3) detailed calculations of totem pole currents in the input buffer driver circuitry. For the RTSX product, totem pole currents are approximately one third of the newer RTSX-S product resulting from a combination of larger transistor gate length geometries as well as lower Vcci voltage maximums. In examination of the metal line widths for the RTSX I/O buffer, the metal line widths are near the same dimensions. Thus the RTSX buffer is considered robust for electro-migration concerns as is the RTSX-S I/O buffer design.

5. CONCLUSION:

Based on the data and results collected from the transition time experiments after high temperature dynamic burn-in following conclusions can be made:

a. Oscillations will occur on input buffers and subsequent internal logic modules when fall times are well beyond those allowed in Actel specifications.

b. Logic levels will most likely be disturbed, as signals will oscillate around the transition region of the particular input buffer and logic modules.

c. Average current levels are relatively low per I/O subjected to the lengthy fall times with approximately 200 μA per I/O measured for the RTSX16 units and 1.2 mA per I/O for RTSX32 units.

d. No I/O or logic module in the burn-in test failed functionality.

e. Post Burn-in current levels remained the same as pre Burn-in.

f. Input logic thresholds remained stable from pre burn-in to post burn-in with shifts less than 50 mV observed.

g. Special purpose pins like TDI, TCK, TDO, and PRB revealed similar behavior as regular I/Os due to the input buffer structure being similar.

h. Clock pins with slow fall time input transitions increased current consumption however no degradation in clock driver operation was observed.

i. EM concern was analyzed and for worse case operating conditions, a 20-year reliability is assured for the input buffer circuitry as well as the output driver circuitry.

*In conclusion, Actel "**guarantees Reliability"** of the RTSX part for a 20 year period for the slow transition time issue on the I/O circuitry, but does **"Not guarantee functionality"** of the part if subjected to the above conditions. Actel will not change the datasheet, and recommends Designer's stay within the 50ns T_r / T_f specification.*

Please feel free to contact us if any clarifications or additional information is required.