RTAX-S/SL/DSP Power-On Reset and Brown-Out Device Behavior FAQs

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Power-Up and Global Clear (GCLR)/Global Preset (GPSET)

1. What are the power-up process steps?

The power-up process steps are as follows,

i) If VCCDA or VCCA starts ramping up during power-up, the internal power-on-reset (POR) is asserted.

ii) When VCCDA and VCCA supplies cross their power-up-to-functional voltage (that is, voltage threshold) levels, the internal POR is de-asserted, refer to Figure 1 and Table 1. The internal blocks are enabled or activated one by one sequentially.

iii) When VCCI is powered up to its operational level, the I/Os are functional.

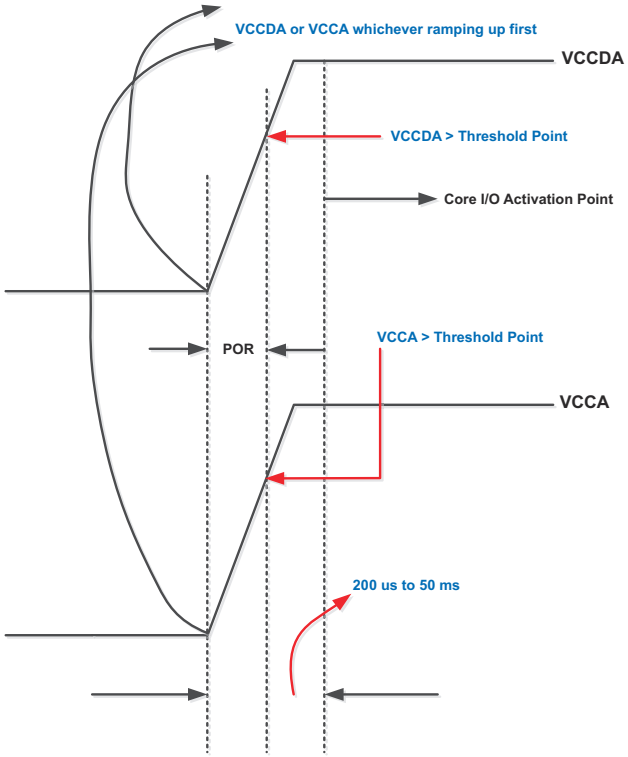

Figure 1: **POR Versus Core and I/Os Activation Points**

Note: Not to scale and just for demonstration.

2. When do the core logic and I/Os become functional?

The core logic and the I/Os are functional after 200 us to about 50 ms (depending on the supply ramp rate) from the point when both supplies cross their power-up-to-functional (voltage threshold) levels, refer to Table 1. Once the I/Os are active, the I/Os function as designed; if any external user reset or preset happens, it takes over at that point.

Table 1: **RTAX-S/SL/DSP Power-Up-To-Functional Time and Voltage**

Supply Ramped		Ramp = 10 us	Ramp = 100 us	Ramp = 1 ms	Ramp = 10 ms	Ramp = 100 ms
VCCDA	Time	223.6 us	323.6 us	1.31 ms	8.54 ms	58.2 ms
	Voltage [V]	3.30	3.30	3.30	2.35	1.50
VCCA	Time	160 us	218 us	640 us	6.36 ms	60.9 ms
	Voltage [V]	1.50	1.50	1.08	1.05	0.99
VCCI	Time	3.27 us	28.18 us	290 us	2.95 ms	30.18 ms
	Voltage [V]	0.77	0.71	0.80	0.79	0.84

Note: Ramp is the time it takes the supply to get to its functional level.

3. Do the RTAX-S/SL/DSP devices have an embedded POR circuit?

Yes, the RTAX-S/SL/DSP devices have an embedded POR circuit and two internal global power-on signals (global clear (GCLR) and global preset (GPSET)). During power-up, either supply VCCDA or VCCA signals rising above the Power-up-To-Functional voltage threshold will assert the internal POR. When both supplies cross their voltage threshold, the internal POR is de-asserted.

4. What are the GCLR and GPSET signals and what are they used for?

The global clear (GCLR) and global preset (GPSET) signals drive, at power-up, the clear and preset inputs of each fabric R-cell as well as each I/O register on a chip-wide basis. Refer to the R-Cell section of the *RTAX-S/SL datasheet* for more information. These signals are used to predefine the state of flip-flops and I/O registers after power up.

5. How are the GCLR and GPSET signals enabled or disabled?

The GCLR and GPSET signals are enabled or disabled by selecting the **Use the global set fuse** check box in the Libero® IDE Designer software when generating the programming file.

- **Use the global set fuse** check box is cleared by default. It means GCLR = 0 (Enabled) and GPSET = 1 (Disabled) during device power-up.
- If the **Use the global set fuse** check box is selected, it means GCLR = 1(Disabled) and GPSET = 0 (Enabled) during device power-up.

Both pins are pulled HIGH when the RTAX-S/SL/DSP devices are in user mode.

6. Are the GCLR and GPSET signals accessible to users?

No, the GCLR and GPSET signals are not accessible to users.

7. What is the difference between the GCLR/GPSET and CLR/PSET signals?

The clear (CLR) and preset (PSET) are two separate, independent, active low, asynchronous, clear, and preset user signals, as shown in Figure 2. The GCLR and GPSET signals, on the other hand, define the state of the flip-flops and I/O registers during power-up based on the user settings (refer to Question 5). Refer to the R-Cell section of the *RTAX-S/SL datasheet* for more information.

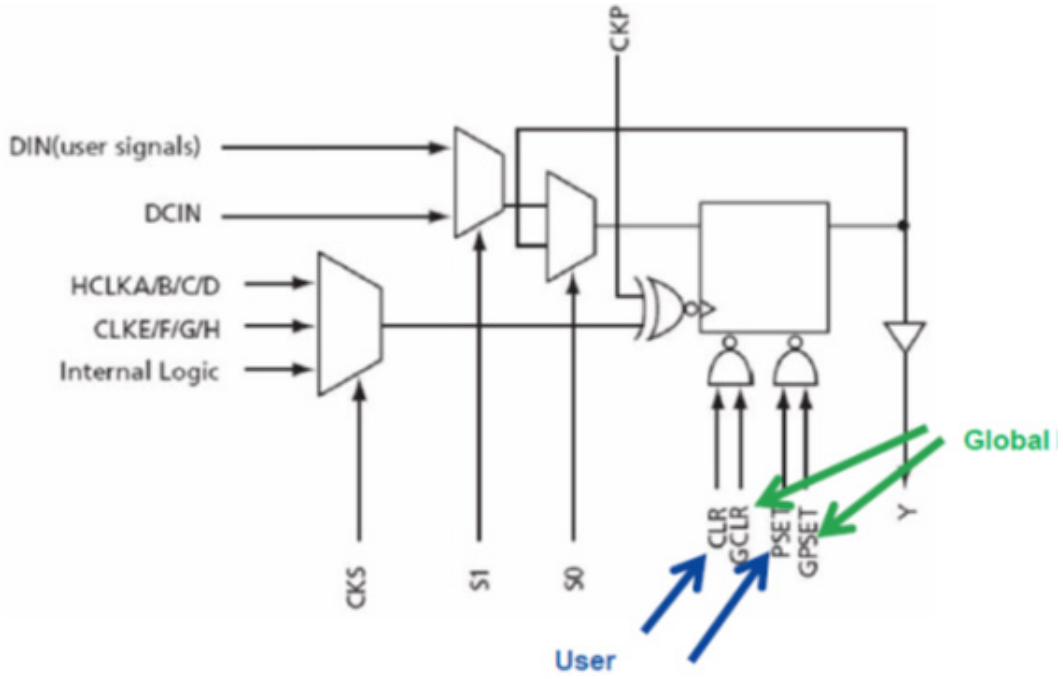

Figure 2: **Global Versus User Clear and Preset Signals**

8. When do the user Clear/Preset (CLR/PSET) signals become active relative to the global clear/preset (GCLR/GPSET) signals?

The global GCLR or GPSET is asserted to all of the core and I/O flip-flops during power-up and it is active until both VCCA and VCCDA reach their operational thresholds, refer to Figure 1 and Table 1. When VCCA and VCCDA reach their operational thresholds, the global signals are de-asserted, the user CLR/PSET signals take over.

Both, the input and output buffers, remain disabled (inputs to the core are “zero” and outputs are “tri-stated”). Once the VCCI is at its minimum operational threshold, the input buffers are enabled where the output buffers remain tri-stated. The time I/Os take to fully power up after the global signal is de-asserted depends on the ramp rate of the VCCI power supply, refer to Table 1.

Outputs are enabled after a long enough time to ensure that all the unwanted glitches are filtered out and that the time is managed by the POR circuit. The entire process typically takes 200 us in the best case and 50 ms in the worst case.

Brown-Out

1. What are the brown-out voltage levels?

As a reference, the brown-out voltage levels are summarized in Table 2. Table 2 shows the voltage levels where functionality ceases for each power supply (Data are collected at room temperature). The device functionality could be affected depending on the power supply that goes below the brown-out voltage level.

Table 2: **RTAX-S/SL/DSP Brown-out Voltage Levels**

Power Supply	Brown-Out Point [V]
VCCDA	1.46
VCCA	0.91
VCCI	0.84

2. What happens when a brown-out is detected? Is the internal POR asserted during power-down or brown-out?

- If the power supplies drop beyond the limits specified in Table 2, a non-deterministic behavior might happen.
- If the brown-out happens only to VCCI, then the internal core logic state is not disturbed.
- Brown-out in RTAX will NOT cause internal chip reset (no POR) and does not start the power-up sequencing of internal blocks on its own.

Note: Axcelerator has a different POR circuitry. If the power supply goes down below the limits, POR will be triggered, and internal blocks will be enabled sequentially one after another

3. How to recover from brown-out?

In order to bring back the functionality, all the power supplies must be backed up to the functional level, and the user must reset the device.

4. Are the flip-flops and/or SRAM states preserved during brown-out?

If VCCA power supply does not go below the limit as listed in Table 2, the flip-flops and/or the SRAM states are preserved during brown-out. If brown-out happens only to VCCI or VCCDA, the internal core logic state is not affected.

5. What is the state of R-cells if only the I/O ring voltage dips to a brown-out level?

The R-cells retain their configuration as brown-out does not trigger reset.

6. What is the state of outputs during brown-out/power-up/power-down?

- If there is a brown-out, the RTAX-S chip does not reset itself.
- If the power supplies continue to drop below the brown-out levels, the I/O behavior and internal logic state are non-deterministic (that is, unknown state), refer to Table 2.
- During power-up, the I/Os are tri-stated. When all the power supplies go above the functional level, the I/Os function as designed, refer to Table 1.

7. How are the internal pulls/clamps affected during power-up/brown-out/power-down?

The internal pulls/clamps are only activated when VCCI and VCCA/VCCDA are fully powered up.

8. Are there any recommendations for designing radiation-tolerant power supplies for RTAX-S/SL/DSP FPGA?

Refer to the *Designing Radiation-Tolerant Power-Supplies for the RTAX-S/SL/DSP FPGA Application Note*

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