The New "Power-Smart" Power Paradigm

White Paper

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Abstract

The next few years will bring great changes in the way our society views the high-tech community. We're in the early stages of a transition that will result in recognition of the electronics industry as a major contributor to the resolution of the world's global warming problems. To date, companies are talking about power reduction initiatives, but more can be done. From the design of "power-smart" chips and systems to the development of industry-wide power efficiency guidelines, the new power paradigm calls for the electronics industry to take responsibility for reducing energy consumption, improving power efficiency and ultimately, reducing greenhouse gasses.

“Power” in a Changing World

In the 1990s, "power" was discussed in relation to supplying power to a system or providing volts and amps to a PC card. And, for most people, "low power" was about a few power-conscious products that looked good on paper, but often saw little success.

Power in semiconductor devices takes two basic forms: static and dynamic. Static power is consumed when the part is not doing any useful work, while dynamic power is consumed when the device is actively working. Until recently, dynamic power was the dominant source of power consumption. Once helping to manage the dynamic power problem, device supply voltages (V_{CC}) had scaled downward with process shrinks and subsequent lower system voltages, but the days of continued scaling are gone. Additionally, the physics associated with integrated circuits (ICs) on smaller process geometries have dramatically increased power related to leakage. And, with leakage worsening, static power has begun to dominate the power consumption equation as the biggest concern (Figure 1).

Figure 1 illustrates the increasing contribution of static power at shrinking process nodes.

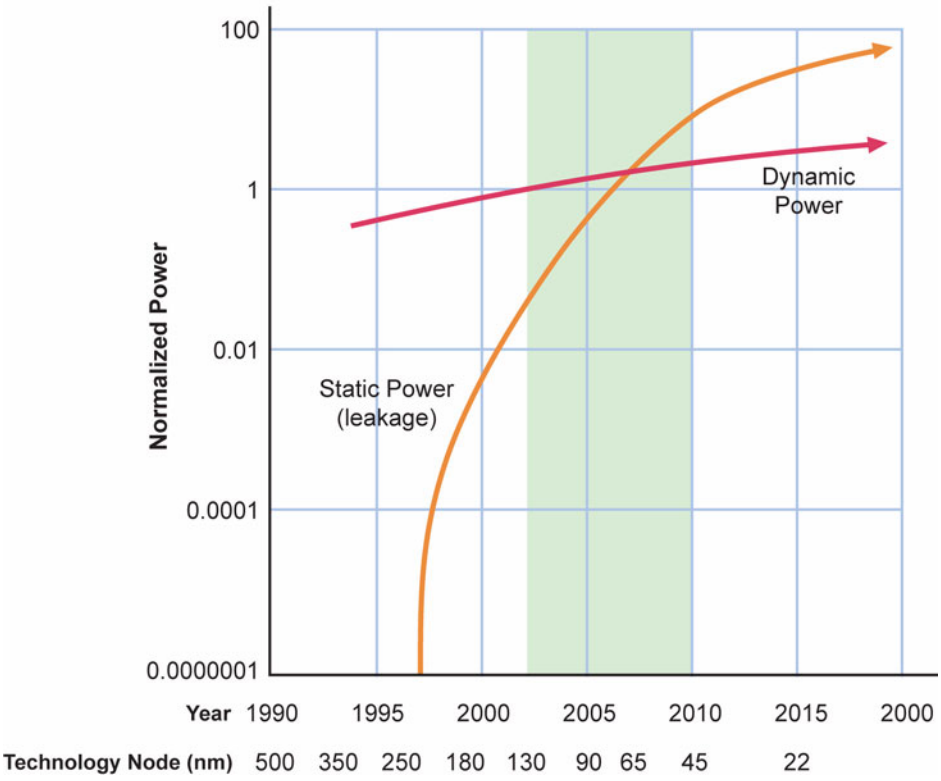

Figure 1: **Static Power Significant at 90 nm**

Another dramatic change from the 1990s is the proliferation of electronics in our society. Yesterday, we used pen and paper to interact, inform, and communicate. Today, we use electronic devices, such as the Apple iPhone® and Palm Treo™ smart phones. As the trend toward portable electronics continues, the world is less willing to buy equipment, like desktop PCs, that has to be plugged into a wall socket. Wasting nearly half of the power delivered to them and increasing the cost of power, today's desktop PCs are a perfect example of the need for low-power offerings.

Unfortunately, the generation of the electricity required to power electronic systems contributes to a surprisingly high proportion of the greenhouse gasses associated with global warming, a real and serious issue. According to a United Nations report issued in May 2007, the average global temperature will rise by as much as 11°F by the turn of the century, even with an aggressive program aimed at minimizing this rise.

As a result, companies are talking about reducing energy usage across the power continuum—from chips to systems—with the goal of helping to protect the environment. Though environmentally friendly steps have been taken, such as lead-free initiatives and RoHS compliance, the electronics industry has not adequately addressed the power issue. And, whereas the presence of small quantities of lead in electronics devices does indeed present a problem, its scope is minimal compared to the disastrous effects that could come if we fail to control global warming.

For example, it is interesting to note that no Environmental Protection Agency (EPA) Energy Star® guidelines exist for semiconductors to date. Though these semiconductor products directly contribute to the power efficiency and management of Energy Star-rated products, the industry has not yet rallied around an approach to benchmarking power efficiency for "low-power" ICs. Well-conceived requirements for semiconductors would enable boards, systems, and end products to minimize energy consumption, improve power efficiency, and reduce greenhouse gasses.

Certainly, a part of the solution to the problem lies in the hands of the electronics industry. With today's power-smart technologies, more can be done. Taking responsibility is mandatory—no longer a choice. The new "power" means a coordinated attack on power consumption—from chips to systems.

Power-Smart Chips

Designers of portable, battery-powered equipment are faced with a daunting challenge—insatiable consumer demand for smaller, cheaper, feature-rich portable devices with longer battery lives, lower cost, and short time to market. The longer the battery life, the lower the cost of ownership for consumers. If the battery life of a smart phone is good for six hours, and if lithium ion batteries typically support 300–500 recharge cycles before a "costly" battery replacement is required, would not these devices be even more attractive if the battery life was extended beyond six hours to weeks or months?

Designers have traditionally relied on application-specific integrated circuits (ASICs) to support the low-power consumption that portable designers require. But ASICs come with their own baggage, namely expensive mask sets and longer time to market. Alternatively, programmable logic solutions, particularly those based on SRAM technology, have provided the shortened time to market but with inherently high static power consumption. In fact, some of today's "low-power" field-programmable gate arrays (FPGAs) and complex programmable logic devices (CPLDs) draw upwards of 30 mA, which is often an order of magnitude or two higher than typical battery-operated applications can tolerate.

SRAM-based devices also experience power surges at startup that can cause battery drain or possible system-initialization failures. Compounding the issue further, each process node shrink means additional static power consumption for transistor-heavy, SRAM-based FPGAs. This is due to worsening problems like quantum tunneling and sub-threshold leakage, which create real challenges for devices targeted to portable applications. The power problem becomes further confused when considering new SRAM-based solutions that utilize flash technology to program the chip's SRAM architecture. Though marketed as flash-

based devices, these solutions must add additional circuitry to the already power-hungry SRAM FPGA fabric.

Fortunately, "true flash" programmable logic technologies exist. Because nonvolatile, flash-based FPGAs do not use millions of power-hungry SRAM configuration bit cells, they have significantly lower static power than SRAM-based solutions, making them ideal for low-power applications. In fact, some available flash-based FPGAs have been designed expressly for low-power applications. With static power as low as 5 µW, these FPGAs deliver more complexity and features with four times lower static power and as much as five times longer battery life in portable applications than CPLDs.

Compared with today's "low-power" best-of-breed, SRAM-based FPGAs, Actel's flash-based IGLOO™ FPGAs deliver between 100 and 1,000 times improvement in power reduction. The two to three orders of magnitude lower static power consumption can translate into weeks and months of standby battery life. For designers of battery-operated portable applications, other advantages of flash-based devices include flexible power saving modes with rapid recovery to operation, low dynamic power consumption, and clock management.

Power-smart chips can offer more than low-power consumption. They also can be used to intelligently control and reduce total power consumption in the overall system. For example, the mixed-signal Actel Fusion™ Programmable System Chip (PSC) offers the integration of FPGA logic with other elements used in system management, such as flash, analog, microprocessors, and clock management. This integration enables designers to remove parts from the board, reduce total power consumption and bill-of-materials (BOM) costs, and enable sophisticated power management of the system.

Power-Smart Systems

Generally, when designing a system, a power goal is set. Often, however, if the designer "approximately" meets this specification, little additional effort is expended to improve the design, leaving watts on the table. Because electronic systems are sold by the hundreds of millions, a few watts of inefficiency in each system eventually translates into staggering amounts of resources being consumed unnecessarily, which ultimately has a detrimental impact on the environmental. Unfortunately, there is usually no easy way to track power down to the individual components or voltage rails, making the job of removing all unnecessary power from devices a difficult task. There is also rarely a way to measure voltages, currents, and temperatures when the system is in operation, which complicates the ability to recognize when things are going badly.

The proliferation of new standards, such as Advanced Telecommunications Computer Architecture (ATCA), MicroTCA, and Intelligent Platform Management Interface (IPMI), prove that the world needs and wants system and enterprise-level power management. These applications require the ability to measure voltages, currents, and temperature in real time and recognize problems; the ability to log and communicate this data; and the ability to take corrective action when appropriate. After all, knowing that a power supply is providing more current than it should or that the board temperature is higher than it should be is not helpful unless steps can be taken to correct it.

System management has historically required multi-chip solutions. With as many as 10–15 extra chips, these designs cost money, consume valuable board space, and burn additional power, which means that the "solution" to the problem is not a solution at all. Multi-chip solutions also require substantial engineering resources, which are often a scarce commodity. And yet, despite these significant costs, the industry has put little effort forth into being smarter about managing and controlling system power.

Recognizing that "one-size-fits-all" is one of the world's greatest lies, it seems clear that a field-programmable solution is called for. A flash-based, single-chip, field-programmable device implementation is the best approach for creating a simple and inexpensive system management solution. Already available off the shelf, these live-at-power-up solutions reduce component count and enable system power

management. Because they are field-programmable, these flexible devices also allow the easy adaptation to the unique needs and changing demands of the project, the system, the board, and the engineer. Further reducing engineering resource requirements, Actel's nonvolatile, mixed-signal Fusion PSCs are complete solutions and include both software and hardware.

Additionally, by integrating necessary housekeeping functions, such as boot up and power supply sequencing, with the power management functionality, system costs are improved. Building power-smart systems costs less upfront and saves significant operating costs. Since each watt that is saved reduces system operating costs by one to two dollars per year, the deployment of cost-effective power management solutions at the enterprise level can save staggering amounts of energy, huge amounts of money, and, more importantly, reap significant benefits on our environment.

A Power-Smart Example

Today, electric motors are used in nearly everything—from elevators to home appliances. In 2005, the US consumed 4,055 billion kWh of electrical power. More than 50 percent of this power was used in electric motors, translating into a staggering 2000 billion kWh. Unfortunately, many of the motors currently in use are inefficient and waste a substantial amount of the power they consume.

With technology improvements in semiconductor processes and integration, mixed-signal FPGAs are emerging as an important alternative for motor control implementation. These highly integrated, flexible platforms offer the bulk of the resources needed for motor control on a single, low-cost device. Using FPGAs in lieu of fixed logic gives designers the flexibility to implement the most efficient design for their application, and the ability to use the same device across a range of motor applications.

The efficiency of small AC motors can be as low as 50 percent. While motor efficiency improves to more than 90 percent as motor size increases, there is still opportunity to improve efficiency and reduce energy consumption. By adding intelligent load matching or variable speed control, the power efficiency of electric motors across the full range can be increased. With a reprogrammable, mixed-signal FPGA and a soft optimized microprocessor, such as the ARM7™ or the ARM® Cortex-M1 processor, this can be accomplished for a range of motor types at a cost attractive for most applications. In fact, coupled with best practices, this combination can result in motor efficiencies approaching 95 percent and, when implemented broadly, could result in annual reduction in U.S. energy consumption of as much as 300 billion kWh, saving billions of dollars and reducing greenhouse gasses by more than 180 million metric tons.

The combination of a reprogrammable, mixed-signal solution and an ARM Cortex-M1 soft microprocessor can improve motor efficiencies, reduce energy consumption, save billions of dollars, and minimize greenhouse gas emissions (Figure 2 on page 6).

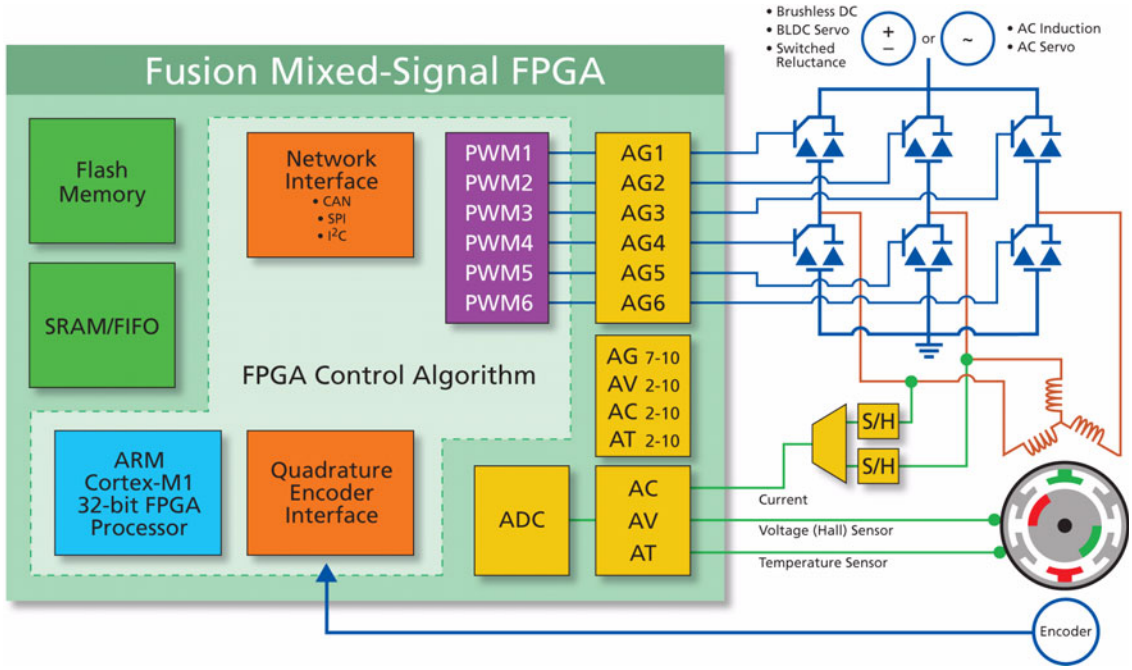

Figure 2: **Power Savings from AC Motor Control Using Mixed-Signal FPGAs**

Conclusion

Over the last two decades, the concept of power has greatly changed. Simultaneously, different types of electronic systems have proliferated. Tragically, the generation of the electricity required to power these electronic systems contributes to a surprisingly high fraction of the greenhouse gasses associated with global warming.

Though companies are talking about reducing energy usage to help protect the environment, more can be done. Whether the design of power-smart chips and systems or the development of industry-wide power efficiency guidelines, the new power paradigm calls for the electronics industry to take responsibility for reducing energy consumption, improving power efficiency and ultimately, reducing greenhouse gasses.

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