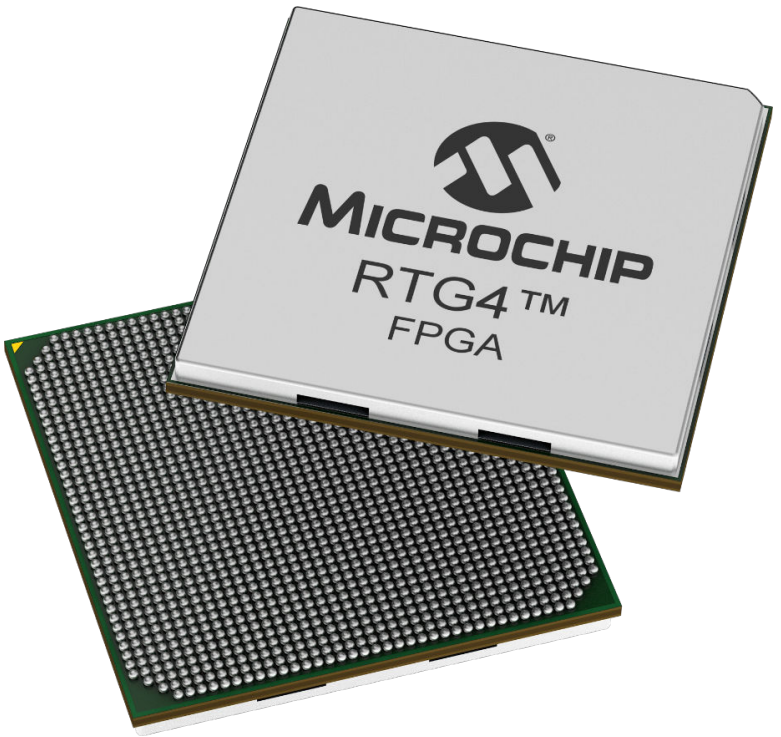
Plastic Package Information for RTG4™ Sub-QML FPGAs

Introduction (Ask a Question)

Microchip's RTG4™ Sub-QML FPGA has been qualified to JEDEC standards in a flip-chip (FC/FCG) 1657 ball grid array plastic package, with 1.0 mm ball pitch. It is pin compatible with our QML Class V-qualified RTG4 FPGAs in ceramic packages CG/LG1657. This document summaries RTG4 plastic package information and recommended Printed Circuit Board (PCB) design rules.

Figure 1. RTG4™ Sub-QML FPGA in Plastic FC/FCG 1657 Package



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1. Thermal Characteristics (Ask a Question)

The temperature variable in the Microchip SoC Products Group Libero® SoC software refers to the junction temperature, not the ambient, case, or board temperatures. This is an important distinction because dynamic and static power consumption will cause the chip's junction temperature to be higher than the ambient, case, or board temperatures.

The following equations show the relationship between thermal resistance, temperature gradient, and power.

$\Theta_{JB} = (T_J - T_B)/P$

$\Theta_{JC} = (T_J - T_C)/P$

where:

Θ_{JB} = Junction-to-board thermal resistance

Θ_{JC} = Junction-to-case thermal resistance

T_J = Junction temperature

T_A = Ambient temperature

T_B = Board temperature (measured 1.0 mm away from the package edge)

T_C = Case temperature

P = Total power dissipated by the device

The following table lists the details of package thermal resistance.

Table 1-1. Package Thermal Resistance

RTG4™ Product	Θ_{JA}	Θ_{JB}	Θ_{JC}	Units
FCG/FC1657[1, 2, 3]	7.52	1.31	0.075	°C/W

Notes: Theta-JC and Theta-JB values are simulated with conduction heat transfer only.

1. Theta-JA values are simulated for still air.
2. Theta-JB for FCG/FC1657 refers to the thermal resistance between the junction to the board as defined in the JESD51 standards.
3. Theta-JC refers to the thermal resistance between the junction and the top surface (package lid).

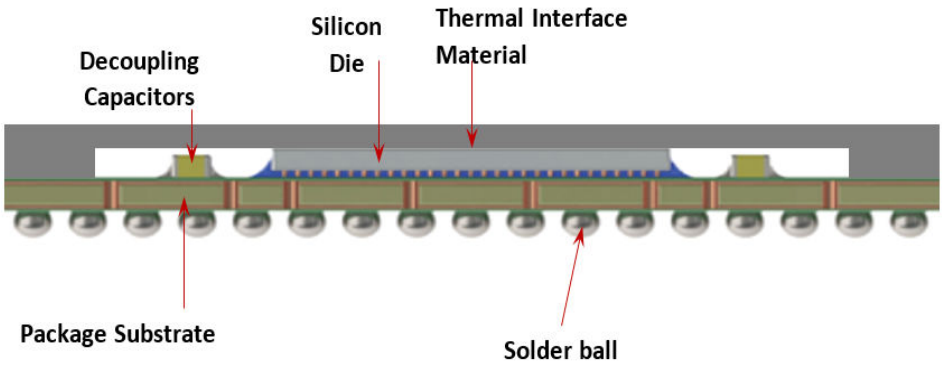
2. Package Specifications (Ask a Question)

The following sections describe the package information and specifications of the RTG4 Sub-QML FPGA.

2.1. Package Information and Materials (Ask a Question)

The following figure shows package information of the RTG4 sub-QML FPGA.

Figure 2-1. Package Information



The following table lists the package information and materials of the RTG4 FC/FCG 1657 package.

Table 2-1. FC1657/FCG1657 Package Information

Package Information and Materials	FC1657	FCG1657
Package type	Flip-chip Ball Grid Array (BGA)	
Package size[1]	42.5 mm x 42.5 mm	
Package pitch	1 mm	
Packaged device weight	16.05 gm	
Decoupling capacitors[2]	Presidio precious metal electrode (PME) 0508	
Solder ball composition	Eutectic SnPb (Sn: 63%/Pb: 37%)	SAC305 (Sn: 96.5%/Ag: 3%/Cu: 0.5%)
Solder bump composition	Pb-free (Sn: 98.2%/Ag: 1.8%)	
Substrate	Organic substrate with ultra-low alpha	
Lid[3]	AlSiC	

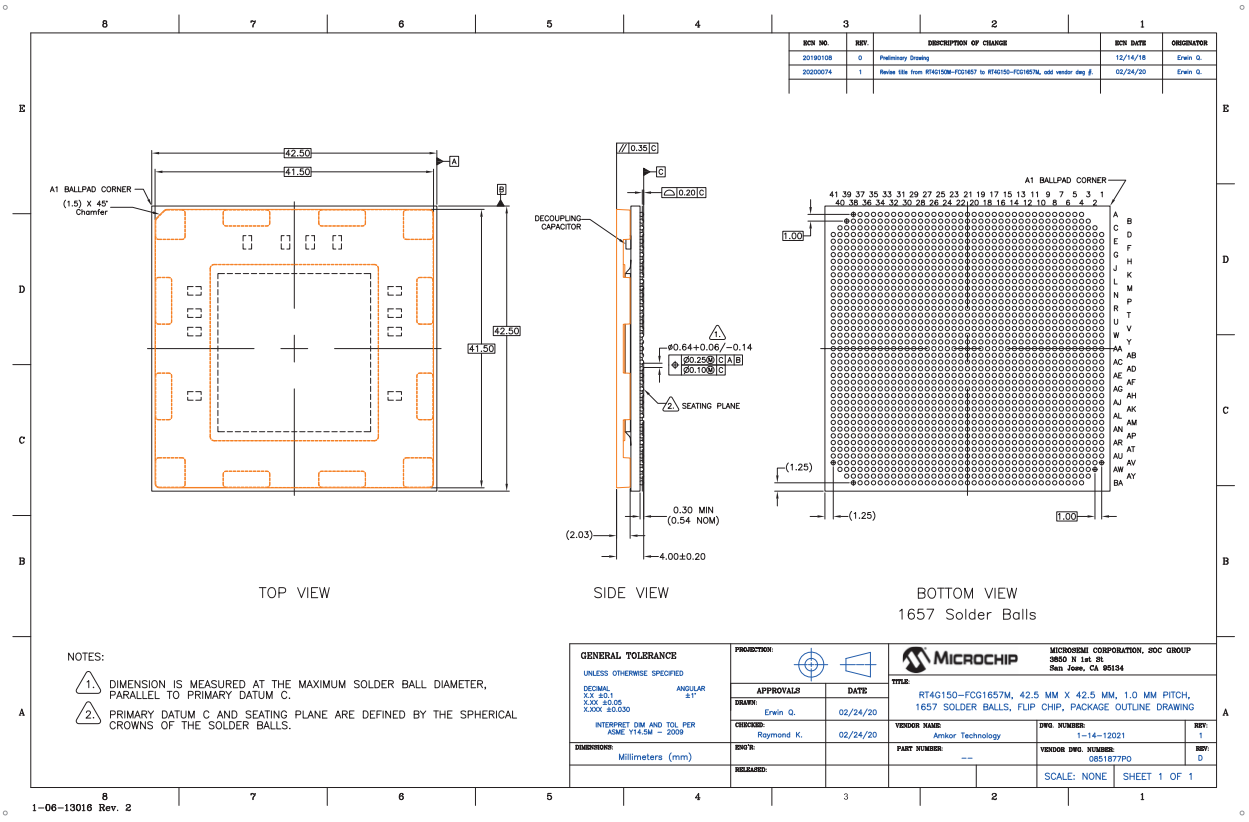
Notes:

1. FC1657 and FCG1657 packages have the same footprint and IO pin assignment as the CG/CB/LG1657 package.
2. The same internal decoupling capacitors are used in RTG4's CG/CB/LG1657 and CQ352 packages.
3. The lids in the FC1657 and FCG1657 packages are not grounded.

2.2. Package Mechanical Drawing (Ask a Question)

The following figure shows the package outline drawing of FC/FCG 1657.

Figure 2-2. Package Outline Drawing



2.3. Packaging Pin Assignment (Ask a Question)

For details, see the FC1657 and FCG1657 Package Pin Assignment Table.

2.4. Pin Descriptions (Ask a Question)

For details, see the DS0130: RTG4 FPGA Pin Descriptions Datasheet.

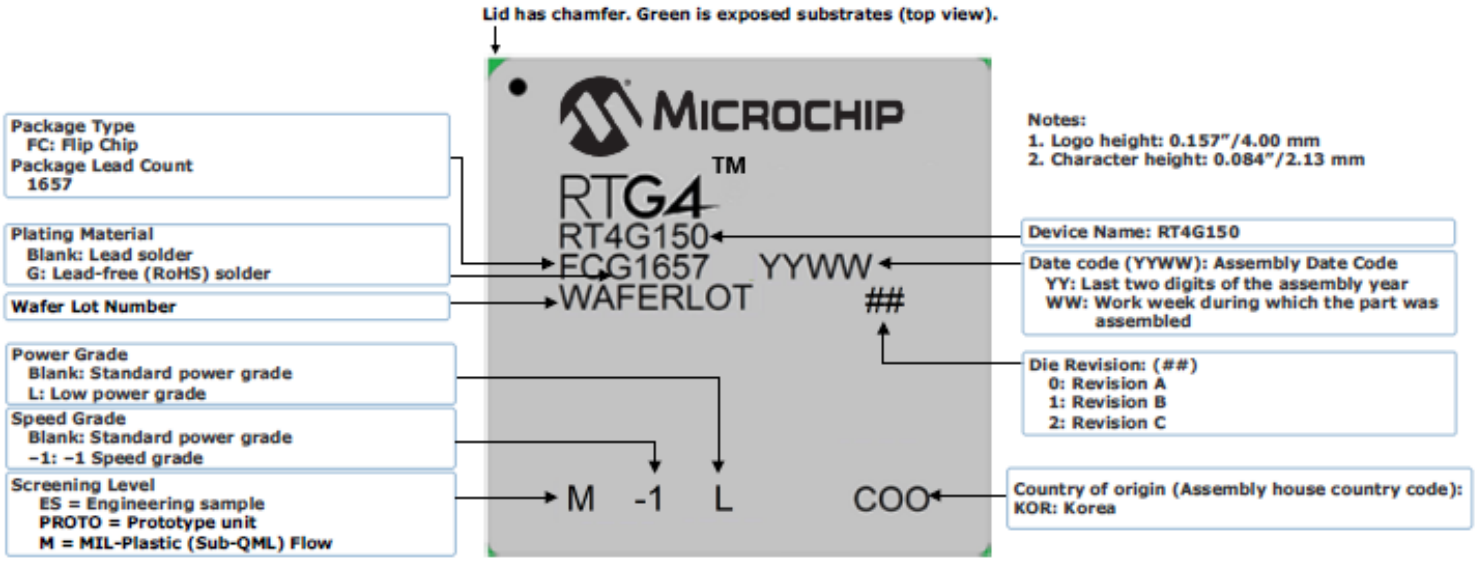
2.5. Daisy Chain Packages (Ask a Question)

For details, see the FCG1657 Daisy Chain Package User Guide.

2.6. Package Marking Specifications (Ask a Question)

Microchip marks the part number on the top of every RTG4 device along with other device specifications, as shown in the following figure.

Figure 2-3. RTG4 Plastic Device Marking Specifications



2.7. Packing and Shipping (Ask a Question)

The RTG4 Sub-QML FPGA in plastic packaging is packed in trays to provide protection from mechanical damage. The maximum number of devices per tray is 12.

2.8. Recommended PCB Design Rules for BGA Packages (Ask a Question)

The land pad information on the package side is required prior to the start of the board layout, so that the board pads can be designed to match the component-side land geometry. The typical values of these land pads are shown in the following figure and listed in Table 2-2. For BGA packages, Non-Solder Mask Defined (NSMD) pads on the board are suggested to allow a clearance between the land metal (diameter) and the solder mask opening (diameter), as shown in the following figure. The space between the NSMD pad and the solder mask, the actual signal trace widths, and through dimensions depend on the capability of the PCB vendor. The cost of the PCB is higher when the line width and spaces are smaller.

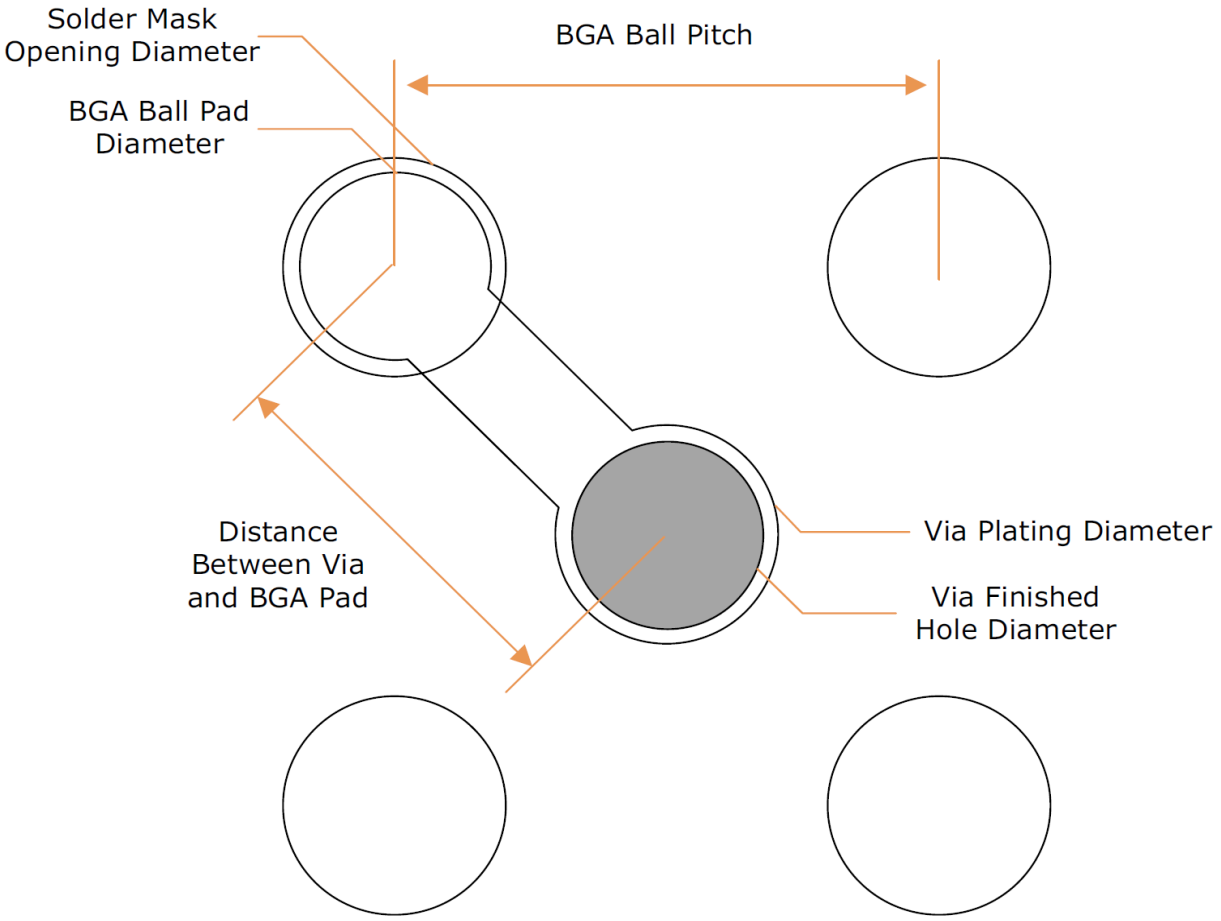


Table 2-2. Recommended PCB Designs Rules

Design Rule for Packages	FC1657/FCG1657 (in mm)
BGA ball pad diameter	0.51
Solder mask opening diameter	0.54
BGA ball pitch	1.0
Line width between via and solder land	0.15
Distance between via and solder Land	0.7
Via finished hole diameter	0.33
Via plating diameter	0.48

3. Moisture Sensitive Level (Ask a Question)

RTG4 Sub-QML FPGAs in FC/FCG1657 packages have Moisture Sensitive Level (MSL) 4.

4. Soldering Reflow Guidelines (Ask a Question)

This section describes the standard reflow profile for standard and lead-free packages.

Note: The reflow is for reference only. Users must optimize their own board level parameters to get proper reflow outcome. Per package qualification maximum number of reflow that can be done on Microchip FPGA packages is 3.

Table 4-1. SnPb Eutectic Process—Classification Temperature (T_C)

Package Thickness	Volume mm^3 < 350	Volume mm^3 ≥ 350
<2.5 mm	235 + 0/–5 °C	225 + 0/–5 °C
2.5 mm	225 + 0/–5 °C	225 + 0/–5 °C

Table 4-2. Pb-Free Process—Classification Temperature (T_C)

Package Thickness (in mm)	Volume mm^3 < 350	Volume mm^3 350–2000	Volume mm^3 > 2000
<1.6	260 + 0 °C[1]	260 + 0 °C[1]	260 + 0 °C[1]
1.6–2.5	260 + 0 °C[1]	250 + 0 °C[1]	245 + 0 °C[1]
≥2.5	250 + 0 °C[1]	245 + 0 °C[1]	245 + 0 °C[1]

Notes:

1. Tolerance: The device manufacturer/supplier must assure process compatibility up to and including the stated classification temperature at the rated MSL level (that is, peak reflow temperature + 0 °C. For example, 260 °C + 0 °C).
2. At the discretion of the device manufacturer, but not the board assembler/user, the maximum peak package body temperature (T_p) can exceed the values specified in Table 4-2 and Table 4-3. The use of a higher T_p does not change the T_C.
3. Package volume excludes external terminals (balls, bumps, lands, and leads) and/or non-integral heat sinks.
4. The maximum component temperature reached during reflow depends on package thickness and volume. The use of convection reflow processes reduces the thermal gradients between packages. However, thermal gradients due to differences in thermal mass of SMD packages might still exist.
5. Moisture sensitivity levels of components used in a Pb-free assembly process must be evaluated using the Pb-free classification temperatures and profiles defined in Table 4-2 and Table 4-3, if Pb-free.
6. SMD packages classified to a given moisture sensitivity level by using Procedures or Criteria defined within any previous version of J-STD-020, JESD22-A112 (rescinded), IPC-SM-786 (rescinded) need not be reclassified to the current revision, unless a change in classification level or a higher peak classification temperature is required.

Table 4-3. Classification Reflow Profile

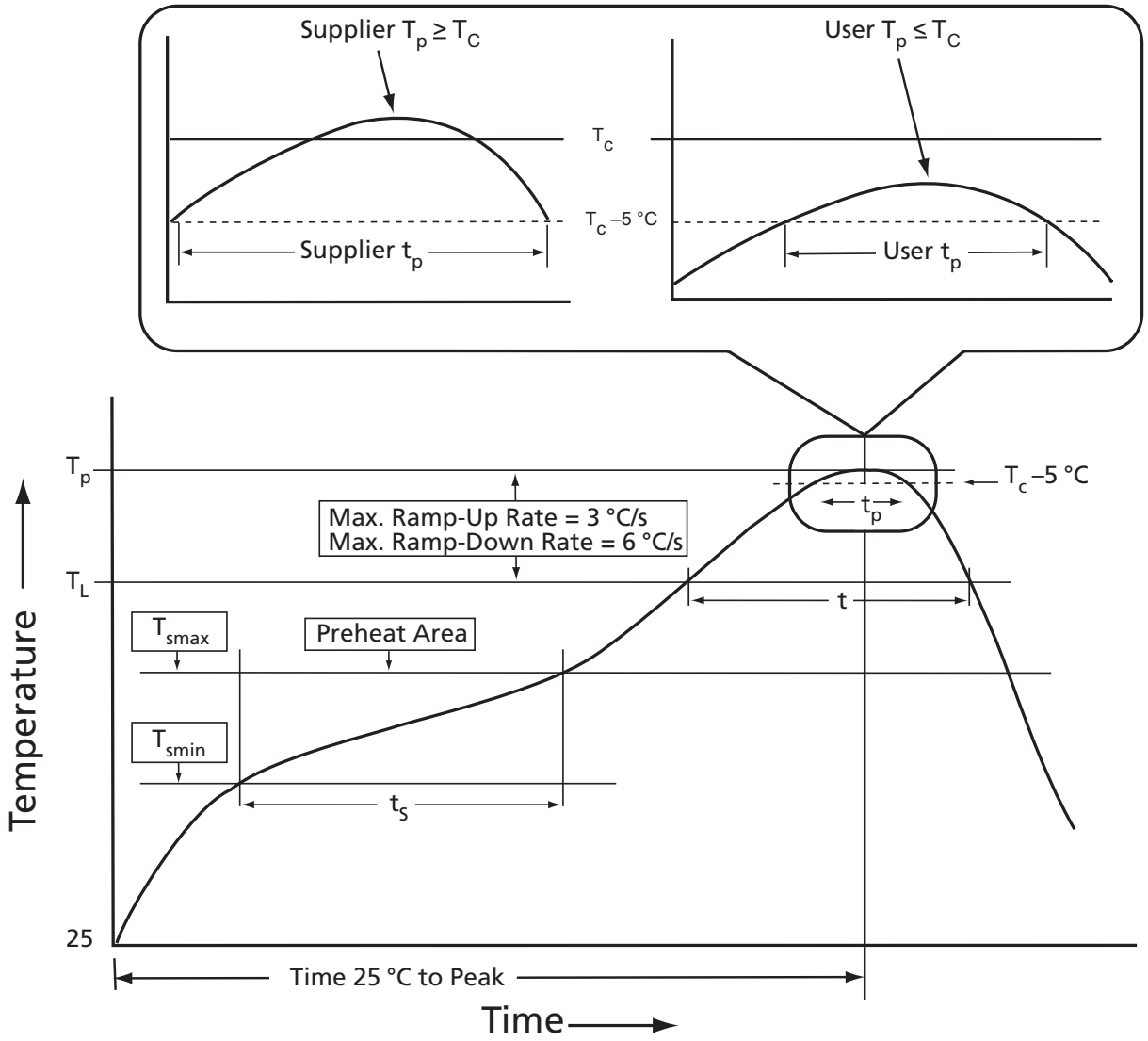
Profile Feature	SnPb Eutectic Assembly	Pb-Free Assembly
Preheat and Soak Temperature minimum (T_{smin}) Temperature maximum (T_{smax}) Time (T_{smin} to T_{smax}) (t_s)	100 °C 150 °C 60s–120s	150 °C 200 °C 60s–120s
Average ramp-up rate (T_{smax} to T_p)	3 °C/second maximum	3 °C/second maximum
Liquidous temperature (T_L) Time at liquidous (t_L)	183 °C 60s–150s	217 °C 60s–150s
Peak package body temperature (T_p)[1]	See classification temperature in Table 4-1.	See classification temperature in Table 4-2.
Time (t_p)[2] within 5 °C of the specified classification temperature (T_C)	202s	302s
Average ramp-down rate (T_p to T_{smax})	6 °C/s maximum	6 °C/s maximum
Time 25 °C to peak temperature	6 minutes maximum	8 minutes maximum

Notes:

1. Tolerance for peak profile temperature (T_p) is defined as a supplier minimum and a user maximum.
2. Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.
3. All temperatures refer to the center of the package, measured on the package body surface that is facing up during the assembly reflow (for example, live-bug). If parts are reflowed in other than the normal live-bug assembly reflow orientation (that is, dead-bug), then the T_p must be within ±2 °C of the live-bug T_p and still meet the T_O requirements. Otherwise, the profile is adjusted to achieve the latter. To accurately measure actual peak package body temperatures, see the JEP140 for recommended thermocouple use.
4. Reflow profiles in this document are for classification/preconditioning and are not meant to specify board assembly profiles. Actual board assembly profiles must be developed based on specific process needs and board designs, and must not exceed the parameters that are listed in Table 4-3.
   For example, if T_O is 260 °C and time t_p is 30 seconds, then:
   - For a supplier: The peak temperature must be at least 260 °C. The time above 255 °C must be at least 30 seconds.
   - Fora user: The peak temperature must not exceed 260 °C. The time above 255 °C must not exceed 30 seconds.
5. All components in the test load must meet the classification profile requirements.
6. SMD packages classified to a given moisture sensitivity level by using Procedures or Criteria defined within any previous version of J-STD-020, JESD22-A112 (rescinded), IPC-SM-786 (rescinded) need not be reclassified to the current revision, unless a change in classification level or a higher peak classification temperature is desired.

The following figure shows the reflow profile.

Figure 4-1. Reflow Profile



5. Revision History (Ask a Question)

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

Revision	Date	Description
B	12/2023	The following is a summary of changes in revision B of this document: • Added a note stating that the lids in the FC1657 and FCG1657 packages are not grounded, in Table 2-1.
A	12/2021	Initial Revision.

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