Automotive Grade 2 IGLOO 2 FPGAs Product Brief

Introduction (Ask a Question)

Microchip's IGLOO® 2 Field Programmable Gate Array (FPGA) integrates fourth generation, Flash-based FPGA fabric and high-performance communications interfaces on a single chip. The IGLOO® 2 family is the industry's lowest-power, most reliable and highest-security programmable logic solution. This next generation IGLOO® 2 architecture offers up to 3.6X gate count, implemented with 4-input Look-Up Table (LUT) fabric with carry chains, giving 2X performance and includes multiple embedded memory options and mathblocks for Digital Signal Processing (DSP). High-speed serial interfaces include PCI Express® (PCIe®), while Double Data Rate 2 (DDR2) or Double Data Rate 3 (DDR3) memory controllers provide high-speed memory interfaces.

Microchip's automotive grade IGLOO® 2 FPGA offers automotive designers the advantages of best-in-class security, high-reliability and low-power flash FPGAs. Automotive grade IGLOO® 2 is offered in grade 2 (-40°C to 125°C TJ) temperature range and is recommended for under-the-hood, in-cabin or on-body applications. IGLOO® 2 provides a broad product roadmap ,with multiple I/Os and fabric density options, to allow users to select a device that fits their requirements.

Features (Ask a Question)

IGLOO® 2 FPGAs have the following features:

- High-performance FPGA
  - Extended temperature AEC-Q100 qualified devices
    - Grade T2: –40°C to 125°C TJ
  - Efficient 4-input LUTs with carry chains for high performance and low power
  - Up to 109 blocks of dual-port 18 Kb SRAM (Large SRAM), with 400 MHz synchronous performance (512 x 36, 512 x 32, 1 Kb x 18, 1 Kb x 16, 2 Kb x 9, 2 Kb x 8,4 Kb x 4, 8 Kb x 2 or 16 Kb x 1)
  - Up to 112 blocks of three-port 1 Kb SRAM, with two Read ports and one Write port (micro SRAM)
  - High-performance DSP
    - Up to 84 fast mathblocks with 18 x 18 signed multiplication, 17 x 17 unsigned multiplication and 44-bit accumulator
- High-speed Serial Interfaces
  - Up to four SerDes lanes, each supporting:
    - Native SerDes interface, facilitating implementation of Serial RapidIO in fabric, or an SGMII interface to a soft ethernet MAC
    - PCI Express® (PCIe®) Endpoint Controller
      - x1, x2 and x4 Lane PCI Express® core
      - Up to 2 KB maximum payload size
      - 64-/32-bit AXI/AHB Host and Client interfaces to the application layer
- High-speed Memory Interfaces
  - High-speed DDRx memory controllers:
    - High-Performance Memory System (HPMS) DDR (MDDR) controllers
    - Supports LPDDR/DDR2/DDR3

        - Maximum 333 MHz clock rate
        - SECDED Enable/Disable feature
        - Supports various DRAM Bus Width Modes, x8, x9, x16 and x18
        - Supports command reordering to optimize memory efficiency
        - Supports data reordering, returning critical word first for each command
    - SDRAM support through a soft SDRAM memory Controller
- High-performance Memory Subsystem
    - 64-KB embedded SRAM (eSRAM)
    - Up to 512-KB embedded Non-Volatile Memory (eNVM)
    - One SPI/COMM_BLK
    - DDR Bridge (two-port data R/W buffering bridge to DDR memory) with 64-bit AXI interface
    - Non-blocking, multi-layer AHB Bus matrix, allowing multi-master scheme, supporting five hosts and seven clients
    - Two AHB/APB interfaces to FPGA fabric (host/client capable)
    - Two DMA controllers to offload data transactions
        - Eight-channel Peripheral DMA (PDMA) for data transfer between HPMS peripherals and memory
    - High-Performance DMA (HPDMA) for data transfer between eSRAM and DDR memories
- Clocking Resources
    - Clock sources
        - High-precision 32-kHz to 20-MHz Main Crystal Oscillator
        - 1-MHz embedded RC Oscillator
        - 50-MHz embedded RC Oscillator
    - Up to 6 Clock Conditioning Circuits (CCCs), with up to six integrated analog PLLs
        - Output clock with six output phases and 45° phase difference (multiply/divide and delay capabilities)
    - Frequency:
        - Input: 1 MHz to 200 MHz
        - Output: 20 MHz to 400 MHz
- Operating Voltage and I/Os
    - 1.2V core voltage
    - Multi-Standard User I/Os (MSIO/MSIOD)
        - LVTTL/LVCMOS 3.3V (MSIO only)
        - LVCMOS 1.2V, 1.5V, 1.8V, 2.5V
        - DDR (SSTL2_1, SSTL2_2)
        - LVDS, MLVDS, Mini-LVDS, RSDS differential standards
        - PCI
        - LVPECL (receiver only)
    - DDR I/Os (DDRIO)
        - DDR, DDR2, DDR3, LPDDR, SSTL2, SSTL18, HSTL
        - LVCMOS 1.2V, 1.5V, 1.8V, 2.5V
- Security
    - Design security:

        - Intellectual Property (IP) protection through unique security features and Use Models New to the PLD industry
        - Encrypted user key and bitstream loading, enabling programming in less-trusted locations
        - Supply-chain assurance device certificate
        - Enhanced anti-tamper features
        - Zeroization
    - Data security:
        - Non-deterministic Random Bit Generator (NRBG)
        - User cryptographic services (AES-256, SHA-256, Elliptical Curve Cryptographic (ECC) engine)
        - User Physically Unclonable Function (PUF) key enrollment and regeneration
        - CRI pass-through DPA patent portfolio license
        - Hardware Firewalls Protecting Microcontroller Subsystem (HPMS) memories
- Reliability
    - Single Event Upset (SEU) immune
        - Zero FIT FPGA configuration cells
    - Single Error Correct Double Error Detect (SECDED) protection on the following:
        - Embedded memory (eSRAMs)
        - PCIe buffer
        - DDR memory controllers with optional SECDED modes
    - Buffers implemented with SEU-Resistant latches on the following:
        - DDR bridges (HPMS, MDDR)
        - SPI FIFO
    - NVM integrity check at power-up and on-demand
    - No external configuration memory required—instant-on, retains configuration when powered off
- Low Power
    - Low static and dynamic power
        - Flash*Freeze mode for fabric
    - Power as low as 13 mW/Gbps, per lane, for SerDes devices
    - Up to 25% lower total power than competing devices

Acronyms (Ask a Question)

The following table lists the acronyms used in the product brief.

Table 1. Acronyms

Acronyms	Descriptions
AES	Advanced Encryption Standard
AHB	Advanced High-Performance Bus
APB	Advanced Peripheral Bus
AXI	Advanced extensible Interface
COMM_BLK	Communication Block
DDR	Double Data Rate
DPA	Differentia lPower Analysis
ECC	Elliptical Curve Cryptography

Table 1. Acronyms (continued)

Acronyms	Descriptions
EDAC	Error Detection And Correction
FIC	Fabric Interface Controller
HPMS	High-Performance Memory Subsystem
IAP	In-Application Programming
MACC	Multiply-Accumulate
MDDR	DDR2/3 Controller in HPMS
SECDED	Single Error Correct Double Error Detect
SEU	Single Event Upset
SHA	Secure Hashing Algorithm

Table of Contents

1. IGLOO® 2 FPGA Overview (Ask a Question)

The following sections discuss key features and the block diagram of IGLOO® 2 FPGAs.

1.1. Block Diagram (Ask a Question)

The following figure shows the various blocks available in IGLOO® 2 FPGAs.

Figure 1-1. IGLOO® 2 FPGA Block Diagram

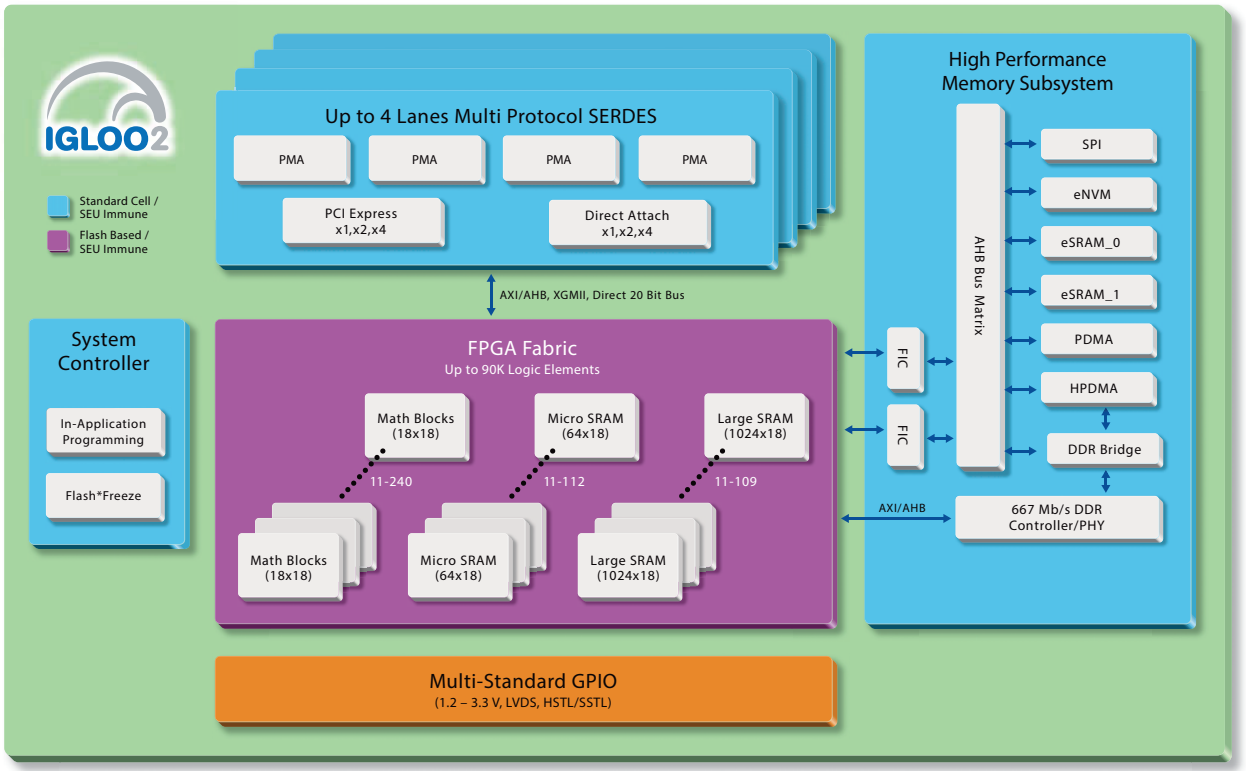


Table 1-1. IGLOO® 2 FPGA Product Family[1]

Peripheral	Features	M2GL005S	M2GL010TS	M2GL025TS	M2GL060TS	M2GL090TS
Logic/DSP	Maximum logic elements (4LUT + DFF)[2]	6,060	12,084	27,696	56,520	86,184
	Math Blocks (18 × 18)	11	22	34	72	84
	PLLs and CCCs	2		6		
	SPI/HPDMA/PDMA	1 each				
	Fabric Interface Controllers (FICs)	1			1	
	Data security	AES256, SHA256, RNG			AES256, SHA256, RNG, ECC, PUF	
Memory	eNVM (KB)	128	256			512
	LSRAM 18K blocks	10	21	31	69	109
	uSRAM 1K blocks	11	22	34	72	112
	eSRAM (KB)	64				
	Total RAM (Kb)	703	912	1104	1826	2586
High Speed	DDR controllers (count × width)	1 × 18			1 × 18	
	SerDes lanes (T)	0	4			
	PCIe® end points	0	1		2	

Table 1-1. IGLOO® 2 FPGA Product Family[1] (continued)

Peripheral	Features	M2GL005S	M2GL010TS	M2GL025TS	M2GL060TS	M2GL090TS
UserI/Os	MSIO (3.3V)	119	123	157	271	309
	MSIOD (2.5V)	28	40	40	40	40
	DDRIO (2.5V)	66	70	70	76	76
	Total user I/O	209	233	267	387	425

Notes:

1. Feature availability is package dependent.
2. Total logic may vary based on utilization of DSP and memories in your design. For more information, see UG0445: SmartFusion 2 SoC FPGA and IGLOO 2 FPGA Fabric User Guide.

1.2. I/Os Per Package (Ask a Question)

The following table lists the various package options.

Table 1-2. I/Os per Package and Package Options

Device	Package and Dimension Information							
	VFG256[1] (14 mm × 14 mm, 0.8 mm pitch)		VFG400[1] (17 mm × 17 mm, 0.8 mm pitch)		FGG484[1] (23 mm × 23 mm, 1.0 mm pitch)		FGG676[1] (27 mm × 27 mm, 1.0 mm pitch)	
	I/O	Lanes	I/O	Lanes	I/O	Lanes	I/O	Lanes
M2GL005S	161	—	**171**	—	**209**	—	—	—
M2GL010TS	**138**	**2**	**195**	**4**	**233**	**4**	—	—
M2GL025TS	**138**	**2**	**207**	**4**	**267**	**4**	—	—
M2GL060TS	—	—	**207**	**4**	**267**	**4**	**387**	**4**
M2GL090TS	—	—	—	**4**	**267**	**4**	**425**	**4**

Notes:

1. All automotive packages are RoHS-compliant and are available in lead-free options only.
2. The blue color indicates that device packages have vertical migration capability.

Table 1-3. Features per Device-Package Combination

Package[4]	Devices	MDDR	Crystal Oscillators	3.125 Gbps SerDes Lanes	PCIe Endpoints	MSIO (3.3V max) [2]	MSIOD (2.5V max) [3]	DDRIO (2.5V max)	Total User I/O
VFG256	M2GL005S	—	1	—	—	119	12	30	161
	M2GL010TS	×18[1]	1	2	1	66	8	64	138
	M2GL025TS	×18[1]	1	2	1	66	8	64	138
VFG400	M2GL005S	×18[1]	1	—	—	79	28	64	171
	M2GL010TS	×18[1]	1	4	1	99	32	64	195
	M2GL025TS	×18[1]	1	4	1	111	32	64	207
	M2GL060TS	×18[1]	1	4	2	111	32	64	207
FGG484	M2GL005S	×18[1]	1	—	—	115	28	66	209
	M2GL010TS	×18[1]	1	4	1	123	40	70	233
	M2GL025TS	×18[1]	1	4	1	157	40	70	267
	M2GL060TS	×18[1]	1	4	2	157	40	70	267
	M2GL090TS	×18[1]	1	4	2	157	40	70	267
FGG676	M2GL060TS	×18[1]	1	4	2	271	40	76	387
	M2GL090TS	×18[1]	1	4	2	309	40	76	425

Notes:

1. DDR supports ×18, ×16, ×9 and ×8 modes.
2. Number of differential MSIO is as follows:
   a. Even: Number of MSIOs/2
   b. Odd: (Number of MSIOs - 1)/2
3. Number of differential MSIOD is as follows:
   a. Even: Number of MSIODs/2
   b. Odd: (Number of MSIODs - 1)/2
4. All automotive packages are RoHS-compliant and are available in lead-free options only.

Table 1-4. Available Programming Interfaces

Package[1]	Devices	JTAG	SPI_0	Flash_GOLDEN_N	System Controller SPI Port
VFG256	M2GL005S	Yes	Yes	Yes	Yes
	M2GL010TS	Yes	Yes	Yes	No
	M2GL025TS	Yes	Yes	Yes	No
VFG400	M2GL005S	Yes	Yes	Yes	Yes
	M2GL010TS	Yes	Yes	Yes	Yes
	M2GL025TS	Yes	Yes	Yes	Yes
	M2GL060TS	Yes	Yes	Yes	Yes
FGG484	M2GL005S	Yes	Yes	Yes	Yes
	M2GL010TS	Yes	Yes	Yes	Yes
	M2GL025TS	Yes	Yes	Yes	Yes
	M2GL060TS	Yes	Yes	Yes	Yes
	M2GL090TS	Yes	Yes	Yes	Yes
FGG676	M2GL060TS	Yes	Yes	Yes	Yes
	M2GL090TS	Yes	Yes	Yes	Yes

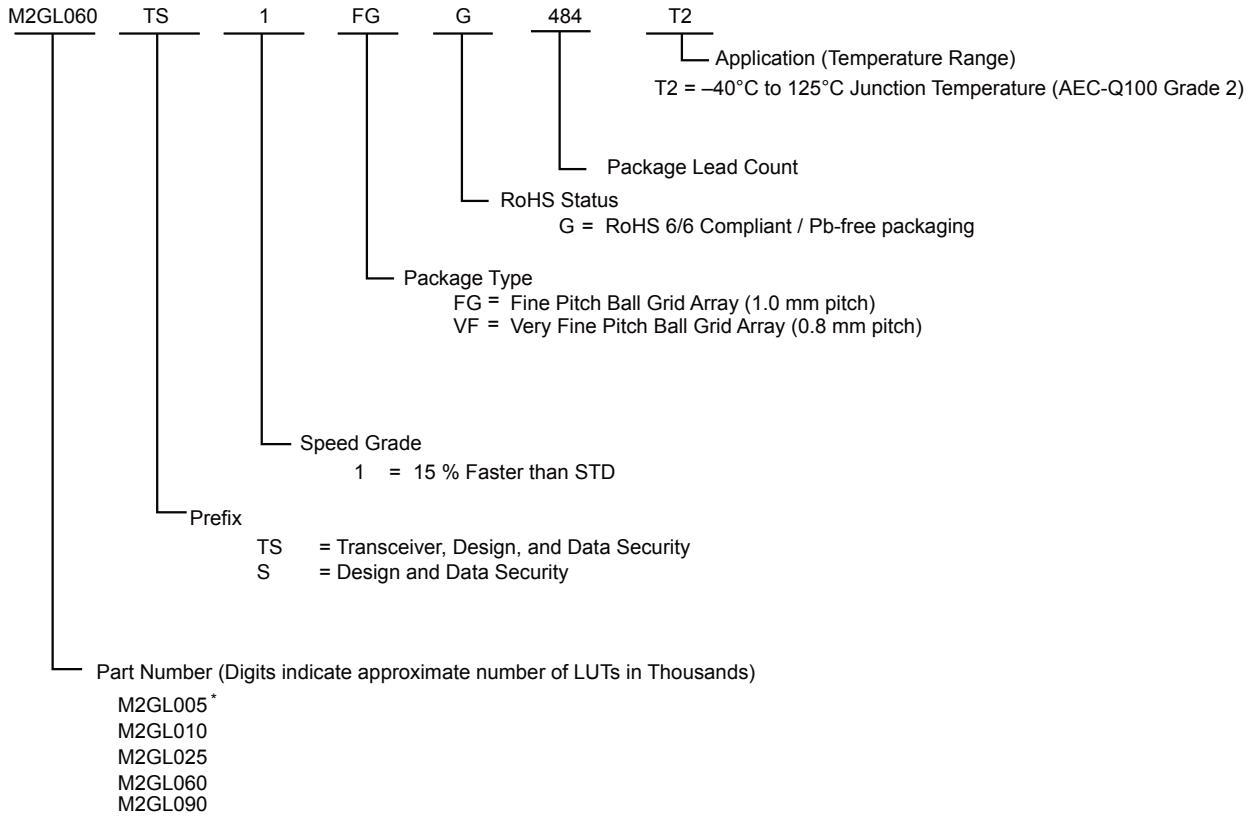
Note:

1. All automotive packages are RoHS-compliant and are available in lead-free options only.

1.3. Ordering Information (Ask a Question)

Each IGLOO® 2 device model has a unique part number, which is used for ordering the device. The part number consists of various elements, each providing additional information about the device. Using the M2GL060 device as an example, the following figure shows the significance of each element in the part number.

Figure 1-2. Elements in a Part Number



Note: M2GL005 devices are not available with transceivers.

1.4. IGLOO® 2 Device Status (Ask a Question)

For device status, see SmartFusion® 2 and IGLOO® 2 Automotive Grade 2 AC/DC Electrical Characteristics.

1.5. IGLOO® 2 Datasheet and Pin Descriptions (Ask a Question)

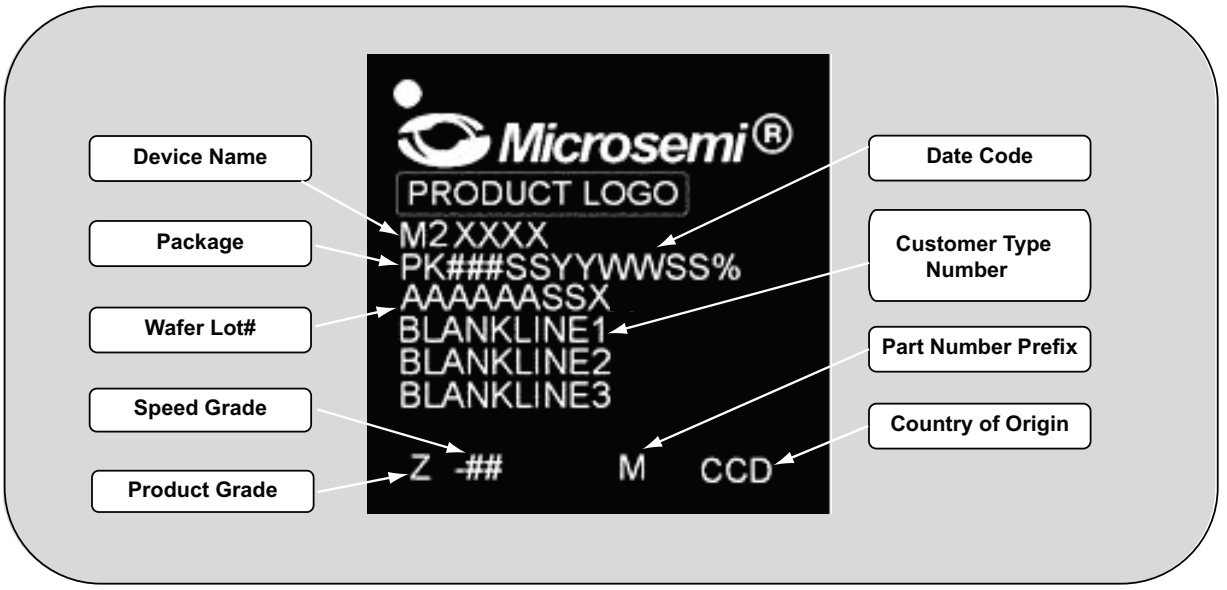
The following documents contain detailed specifications and pin descriptions for IGLOO® 2 FPGAs:

- SmartFusion® 2 and IGLOO® 2 Automotive Grade 2 AC/DC Electrical Characteristics
- IGLOO 2 Pin Descriptions

1.6. Marking Specification Details (Ask a Question)

Microchip normally topside marks the full ordering part number on each device. The following figure provides the details for each character code present on Microchip's IGLOO® 2 FPGA devices.

Figure 1-3. Marking Specifications



1.6.1. Description (Ask a Question)

- Device name (M2XXXX): M2GL for IGLOO® 2 devices
  - Example: M2GL060TS
- Package(PK###): Available package as below:
  - PK: Package code[1]:
    - FGG: Fine Pitch BGA, 1.00 mm pitch
    - VFG: Very Fine Pitch BGA, 0.8 mm pitch
    - ###: Number of Pins: Can be three or four digits (for example: 256)
- Wafer Lot (AAAAAASSX): Microchip wafer lot #
  - AAAAAA: Wafer lot number
  - X: One digit die revision code
  - SS: Two blank spaces
- Speed Grade (-##): Speed binning number
  - Blank: Standard speed grade
  - –1: –1 Speed grade
- Product grade (Z): Product grade; assigned as follows:
  - Blank/C: Commercial
  - ES: Engineering Samples
  - I: Industrial
  - M: Military Temperature
  - PP: Pre Production
  - T2: Automotive Temperature Grade 2
- Date Code (YYWWSS%): Assembly date code
  - YY: Last two digits for seal year

[1] All automotive packages are RoHS-compliant and available in lead-free options only.

  - WW: Work week the part was sealed
  - SS: Two blank spaces
    %: Can be digital number or character for new product
- Customer Type Number: As specified on lot traveler
  - GW: Gold Wire bond
- Part number Prefix: Part number prefix, assigned as below
  - Blank: Design security
  - S: Design and data security
  - TS: Transceiver, design and data security
- Country of Origin (CCD): Assembly house country code
  - China: CHN
  - HongKong: HKG
  - Japan: JPN
  - Korea,South: KOR
  - Philippines: PHL
  - Taiwan: TWN
  - Singapore: SGP
  - United States: USA
  - Malaysia: MYS

2. IGLOO® 2 FPGA Feature Description (Ask a Question)

Microchip's IGLOO® 2 FPGAs integrate fourth generation flash-based FPGA fabric and high-performance communications interfaces on a single chip. The IGLOO® 2 family is the industry's low power, highly-reliable and secure programmable logic solution. This next generation IGLOO® 2 architecture offers up to 3.6X gate count, implemented with 4-input Look-Up Table (LUT) fabric with carry chains, giving 2X performance and includes multiple embedded memory options and mathblocks for DSP. High-speed serial interfaces enable PCIe, while DDR2/DDR3 memory controllers provide high-speed memory interfaces.

The following sections provide detailed descriptions of the various features of IGLOO® 2 FPGAs.

2.1. Reliability (Ask a Question)

IGLOO® 2 flash-based fabric has zero FIT configuration rate due to its Single Event Upset (SEU) immunity, which is critical in reliability applications. The flash fabric also has the advantage of not requiring any external configuration memory, making the device instant-on; it retains configuration when powered off. To complement this unique FPGA capability, IGLOO® 2 devices add reliability to many other aspects of the device. Single Error Correct Double Error Detect (SECDED) protection is implemented on the embedded SRAM (eSRAM), and is optional on the DDR memory controllers. This means that if a one-bit error is detected, it will be corrected. Errors of more than one bit are detected only and not corrected. SECDED error signals are brought to the FPGA fabric to allow the user to monitor the status of these protected internal memories. Other areas of the architecture are implemented with latches, which are more resistant to SEUs. Therefore, no correction is needed in these locations: DDR bridges (HPMS, MDDR), SPI and PCIe® FIFOs.

2.2. Highest Security Devices (Ask a Question)

Building further on the intrinsic security benefits of flash nonvolatile memory technology, the IGLOO® 2 family incorporates all the legacy security features that made the original SmartFusion®, Fusion®, IGLOO® and ProASIC® 3 third-generation flash FPGAs and SoCs the gold standard for secure devices in the PLD industry. In addition, the fourth-generation flash-based SmartFusion® 2 and IGLOO® 2 FPGAs add many unique design and data security features and use models new to the PLD industry.

2.2.1. Design Security vs. Data Security (Ask a Question)

When classifying security attributes of Programmable Logic Devices (PLDs), a useful distinction is made between design security and data security.

2.2.2. Design Security (Ask a Question)

Design security protects the intent of the owner of the design, such as keeping the design and associated bitstream keys confidential, prevents design changes (for example, insertion of Trojan Horses), and controls the number of copies made throughout the device life cycle. Design security may also be known as Intellectual Property (IP) protection. It is one aspect of Anti-Tamper (AT) protection. Design security applies to the device from initial production, includes any updates such as in-the-field upgrades, and can include decommissioning of the device at the end of its life, if desired. Good design security is a prerequisite for good data security.

The following table lists the design security features supported in various IGLOO® 2 devices. Blank cells indicate that the feature is not supported

Table 2-1. Design Security Features

Features	M2GL005S, M2GL010TS, M2GL025TS	M2GL060TS, M2GL090TS
FlashLock™ passcode security (256-bit)	Yes	Yes
Flexible security settings using FlashLock™ bits	Yes	Yes

Table 2-1. Design Security Features (continued)

Features	M2GL005S, M2GL010TS, M2GL025TS	M2GL060TS, M2GL090TS
Encrypted/authenticated design key loading	Yes	Yes
Symmetric key design security (256-bit)	Yes	Yes
Design key verification protocol	Yes	Yes
Encrypted/authenticated configuration loading	Yes	Yes
Certificate-of-Conformance (C-of-C)	Yes	Yes
Back-tracking prevention (also known as, Versioning)	Yes	Yes
Device certificate(s) (anti-counterfeiting)	Yes	Yes
Support for configuration variations	Yes	Yes
Fabric NVM and eNVM integrity tests	Yes	Yes
Information services (S/N, Cert., USERCODE and others)	Yes	Yes
Tamper detection	Yes	Yes
Tamper response (includes Zeroization)	Yes	Yes
ECC public key design security (384-bit)	—	Yes
Hardware intrinsic design key (SRAM-PUF)	—	Yes

2.2.3. Data Security (Ask a Question)

Data Security is protecting the information the FPGA is storing, processing or communicating in its role in the end application. If, for example, the configured design is implementing the key management and encryption portion of a secure military radio, data security could entail encrypting and authenticating the radio traffic, and protecting the associated application-level cryptographic keys. Data security is closely related to the terms Information Assurance (IA) and information security. All IGLOO® 2 devices incorporate enhanced design security, making them the most secure programmable logic devices ever made. Select IGLOO® 2 models also include an advanced set of on-chip data security features that make designing secure information assurance applications easier and better than ever before.

The following table lists the data security features supported in various IGLOO® 2 devices. Blank cells indicate that the feature is not supported.

Table 2-2. Data Security Features

Features	M2GL005S, M2GL010TS, M2GL025TS	M2GL060TS, M2GL090TS
CRI pass-through DPA patent license	Yes	Yes
Hardware firewalls protecting access to memories	Yes	Yes
Non-deterministic random bit generator service	Yes	Yes
AES-128/256 service (ECB, OFB, CTR, CBC modes)	Yes	Yes
SHA-256 service	Yes	Yes
HMAC-SHA-256 service	Yes	Yes
Key tree service	Yes	Yes
PUF emulation (Pseudo-PUF)	Yes	—
PUF emulation (SRAM-PUF)	—	Yes
ECC point-multiplication service	—	Yes
ECC point-addition service	—	Yes
User SRAM-PUF enrollment service	—	Yes
User SRAM-PUF activation code export service	—	Yes
SRAM-PUF intrinsic key generation and enrollment service	—	Yes
SRAM-PUF key import and enrollment service	—	Yes

Table 2-2. Data Security Features (continued)

Features	M2GL005S, M2GL010TS, M2GL025TS	M2GL060TS, M2GL090TS
SRAM-PUF key regeneration service	—	Yes

2.3. Low Power (Ask a Question)

Microchip's flash-based FPGA fabric results in extremely low-power design implementation, with static power as low as 7.5 mW (for 6,060 LE device). Flash*Freeze (F*F) technology provides an ultra-low, power-static mode (Flash*Freeze mode) for IGLOO® 2 devices, with power less than 6.12 mW for the largest device (86,184 LE device). F*F mode entry retains all the SRAM and register information and the exit from F*F mode achieves rapid recovery to Active mode.

2.4. High-Performance FPGA Fabric (Ask a Question)

Built on 65 nm process technology, the IGLOO® 2 FPGA fabric is composed of four building blocks:

- Logic module
- Large SRAM
- Micro SRAM
- Mathblock

The logic module is the basic logic element and has advanced features:

- A fully permutable 4-input Look-Up Table (LUT), optimized for lowest power
- A dedicated carry chain based on carry look-ahead technique
- A separate flip-flop which can be used independently from the LUT

The 4-input LUT can be configured either to implement any 4-input combinatorial function or to implement an arithmetic function where the LUT output is XORed with carry input to generate the sum output.

2.4.1. Dual-Port Large SRAM (LSRAM) (Ask a Question)

Large SRAM (RAM1Kx18) is intended for storing large memory for use with various operations. Each LSRAM block can store up to 18,432 bits. Each RAM1Kx18 block contains two independent data ports: Port A and Port B. The LSRAM is synchronous for both Read and Write operations. Operations are triggered on the rising edge of the clock. The data output ports of the LSRAM have pipeline registers which have control signals that are independent of the SRAM's control signals.

2.4.2. Three-Port Micro SRAM (uSRAM) (Ask a Question)

Micro SRAM (RAM64x18) is the second type of SRAM which is embedded in the fabric of IGLOO® 2 devices. RAM64x18 uSRAM is a 3-port SRAM; it has two read ports (Port A and Port B) and one write port (Port C). The two read ports are independent of each other and can perform Read operations in both synchronous and asynchronous modes. The write port is always synchronous. The uSRAM block is approximately 1 KB (1,152 bits) in size. These uSRAM blocks are primarily intended for building embedded FIFOs to be used by any embedded fabric hosts.

2.4.3. Mathblocks for DSP Applications (Ask a Question)

The fundamental building block in any digital signal processing algorithm is the multiply-accumulate function. The IGLOO® 2 device implements a custom 18 × 18 Multiply-Accumulate (18 × 18 MACC) block for efficient implementation of complex DSP algorithms such as Finite Impulse Response (FIR) filters, Infinite Impulse Response (IIR) filters and Fast Fourier Transform (FFT) for filtering and image processing applications.

Each mathblock has the following capabilities:

- Supports 18 × 18 signed multiplications natively (A[17:0] x B[17:0])

- Supports dot product; the multiplier computes:
  - (A[8:0] × B[17:9] + A[17:9] × B[8:0]) × 2^9
- Built-in addition, subtraction and accumulation units to combine multiplication results efficiently

In addition to the basic MACC function, DSP algorithms typically need small amounts of RAM for coefficients and larger RAMs for data storage.IGLOO® 2 micro RAMs are ideally suited to serve the needs of coefficient storage while the large RAMs are used for data storage.

2.5. High-Performance Memory Subsystem (Ask a Question)

HPMS embeds two separates 32 KB SRAM blocks that have optional SECDED capabilities (32 KB with SECDED enabled, 40 KB with SECDED disabled), up to two separate 256 KB eNVM (flash) blocks, and two separate DMA controllers for fast DMA user logic offloading. The HPMS provides multiple interfacing options to the FPGA fabric in order to facilitate tight integration between the HPMS and user logic in the fabric.

2.5.1. DDR Bridge (Ask a Question)

The DDR bridge is a data bridge between two AHB bus hosts and a single AXI bus client. The DDR bridge accumulates AHB writes into write combining buffers prior to bursting out to external DDR memory. The DDR bridge also includes read combining buffers, allowing AHB hosts to efficiently read data from the external DDR memory from a local buffer. The DDR bridge optimizes reads and writes from multiple hosts to a single external DDR memory. Data coherency rules between the hosts and the external DDR memory are implemented in hardware. The DDR bridge contains two write combining/read buffers. All buffers within the DDR bridge are implemented with SEU-tolerant latches and are not subject to the Single Event Upsets (SEUs) that SRAM exhibits. IGLOO® 2 devices implement two DDR bridges in the HPMS and MDDR subsystems.

2.5.2. AHB Bus Matrix (ABM) (Ask a Question)

The AHB Bus Matrix (ABM) is a non-blocking, AHB-Lite multi-layer switch, supporting 4 Host interfaces and 8 Client interfaces. The switch decodes access attempts by hosts to various clients, according to the memory map and security configurations. When multiple hosts are attempting to access a particular client simultaneously, an arbiter associated with that client decides which hosts gains access, according to a configurable set of arbitration rules. These rules can be configured by the user to provide different usage patterns to each client. For example, a number of consecutive access opportunities to the client can be allocated to one particular host, to increase the likelihood of same type accesses (all reads or all writes), which makes more efficient usage of the bandwidth to the client.

2.5.3. Fabric Interface Controller (FIC) (Ask a Question)

The FIC block provides separate interfaces between the HPMS and the FPGA fabric: the HPMS master (MM) and Fabric Master (FM). Each of these interfaces can be configured to operate as AHB-Lite or APB3. Depending on device density, there are up to two FIC blocks present in the HPMS (FIC_0 and FIC_1).

2.5.4. eSRAM (Ask a Question)

The HPMS contains two blocks of 32 KB eSRAM, giving a total of 64 KB. Having the eSRAM arranged as two separate blocks allows the user to take advantage of the parallelism that exists in the HPMS.

The eSRAM is designed for Single Error Correct Double Error Detect (SECDED) protection. When SECDED is disabled, the SRAM usually used to store SECDED data may be reused as an extra 16 KB of eSRAM.

2.5.5. eNVM (Ask a Question)

The HPMS contains up to 512 KB of eNVM (64 bits wide).

2.5.6. DMA Engines (Ask a Question)

Two DMA engines are present in the HPMS: High-Performance DMA (HPDMA) and Peripheral DMA (PDMA).

2.5.6.1. HPDMA (Ask a Question)

The High-Performance DMA (HPDMA) engine provides efficient memory to memory data transfers between an external DDR memory and internal eSRAM. This engine has two separate AHB-Lite interfaces—one to the MDDR bridge and the other to the AHB bus matrix. All transfers by the HPDMA are full word transfers.

2.5.6.2. PDMA (Ask a Question)

The Peripheral DMA engine (PDMA) is tuned for offloading byte-intensive operations, involving HPMS peripherals, to and from the internal eSRAMs. Data transfers can also be targeted to user logic/RAM in the FPGA fabric.

2.5.7. APB Configuration Bus (Ask a Question)

On every IGLOO® 2 device memory, an APB configuration bus is present to allow the user to initialize the SerDes ASIC blocks, the fabric DDR memory controller and user instantiated peripherals in the FPGA fabric.

2.5.8. Peripherals (Ask a Question)

A large number of communications and general purpose peripherals are implemented in the HPMS.

2.5.8.1. Communication Block (COMM_BLK) (Ask a Question)

The COMM block provides a UART-like communications channel between the HPMS and the system controller. System services are initiated through the COMM block. System services such as Enter Flash*Freeze mode are initiated though this block.

2.5.8.2. Serial Peripheral Interface (SPI) (Ask a Question)

The SPI controller is compliant with the Motorola SPI, Texas Instruments synchronous serial and National Semiconductor MICROWIRE™ formats. In addition, the SPI supports interfacing to large SPI flash and EEPROM devices by way of the client protocol engine. The SPI controller supports both Host and Client modes of operation.

The SPI controller embeds two 4 × 32 (depth × width) FIFOs for receive and transmit. These FIFOs are accessible through RX data and TX data registers. Writing to the TX data register causes the data to be written to the transmit FIFO. This is emptied by transmit logic. Similarly, reading from the RX data register causes data to be read from the receive FIFO.

2.6. Clock Sources: On-Chip Oscillators, PLLs and CCCs (Ask a Question)

IGLOO® 2 devices have two on-chip RC oscillators—a 1MHz RC oscillator and a 50 MHz RC oscillator —and the main crystal oscillator (32 kHz–20 MHz). These are available to the user for generating clocks to the on-chip resources and the logic built on the FPGA fabric array. These oscillators can be used in conjunction with the integrated user Phase- Locked Loops (PLLs) and FAB_CCCs to generate clocks of varying frequency and phase. In addition to being available to the user, these oscillators are also used by the system controller, power-on reset circuitry and HPMS during the Flash*Freeze mode.

IGLOO® 2 devices have up to six fabric CCC (FAB_CCC) blocks and a dedicated PLL associated with each CCC to provide flexible clocking to the FPGA fabric portion of the device. The user has the freedom to use any of the six PLLs and CCCs to generate the fabric clocks and the internal HPMS clock from the base fabric clock (CLK_BASE). There is also a dedicated CCC block for the HPMS (HPMS_CCC) and an associated PLL (MPLL) for HPMS clocking and de- skewing the CLK_BASE clock. The Fabric Alignment Clock Controller (FACC), part of the HPMS CCC, is responsible for generating various aligned clocks required by the HPMS for correct operation of the HPMS blocks and synchronous communication with the user logic in the FPGA fabric.

2.7. High Speed Serial Interfaces (Ask a Question)

This section discusses the various high-speed serial interfaces.

2.7.1. SerDes Interface (Ask a Question)

IGLOO® 2 FPGA has up to four 3.125 Gbps SerDes transceivers, each supporting the following components:

- Four SerDes/PCS lanes
- The native SerDes interface facilitates implementation of Serial RapidIO (SRIO) in fabric or a SGMII interface for a soft Ethernet MAC.

2.7.2. PCIe® (Ask a Question)

PCIe® is a high-speed, packet-based, point-to-point, low-pin-count, serial interconnect bus. The IGLOO® 2 family has two hard, high-speed serial interface blocks. Each SerDes block contains a PCIe® system block. The PCIe® system is connected to the SerDes block. The following features are supported::

- x1, x2 and x4 lane configuration
- Endpoint configuration only
- PCI Express® base specification revision 2.0
- 2.5 Gbps-compliant
- Embedded receive (2 KB), transmit (1 KB) and retry (1 KB) buffer dual-port RAM implementation
- Up to 2 KB maximum payload size
- 64-bit AXI or 32-bit/64-bit AHBL Host and Client interface to the application layer
- 32-bit APB interface to access configuration and status registers of the PCIe® system
- Upto 3 × 64 bit base address registers
- One Virtual Channel (VC)

2.8. High Speed Memory Interfaces: DDRx Memory Controllers (Ask a Question)

There are upto two DDR subsystems, including MDDR (HPMS DDR), present in IGLOO® 2 devices. Each subsystem consists of a DDR controller, PHY and a wrapper. The MDDR has an interface to/from the HPMS and fabric.

MDDR supports the following features:

- LPDDR, DDR2 and DDR3 memories
- Simplified DDR command interface to standard AMBA AXI/AHB interface
- Upto 667 Mbps (333 MHz double data rate) performance
- 1, 2 or 4 ranks of memory
- Different DRAM bus width modes: x8, x9, x16 and x18
- DRAM burst length of 2, 4 or 8 in Full Bus-Width mode; supports DRAM burst length of 2, 4, 8 or 16 in Half Bus-Width mode
- Memory densities up to 4 GB
- A maximum of eight memory banks
- SECDED enable/disable feature
- Embedded physical interface (PHY)
- Read and Write buffers in fully associative CAMs, configurable in powers of 2, up to 64 Reads plus 64 Writes
- Dynamically changing clock frequency while in self-refresh

- Command reordering to optimize memory efficiency
- Data reordering, returning critical word first for each command

2.8.1. MDDR Subsystem (Ask a Question)

The MDDR subsystem has two interfaces to the DDR. One is an AXI 64-bit bus from the DDR bridge within the HPMS. The other is a multiplexed interface from the FPGA fabric, which can be configured as either a single AXI 64-bit bus or two 32-bit AHB-Lite buses. There is also a 16-bit APB configuration bus, which is used to initialize the majority of the internal registers within the MDDR subsystem after reset. This APB configuration bus is mastered by a host in the FPGA fabric. Support for 3.3V Single Data Rate DRAMs (SDRAM) can be obtained by instantiating a soft AHB or AXI SDRAM memory controller in the FPGA fabric and connecting I/O ports to 3.3V MSIO.

2.9. IGLOO® 2 Development Tools (Ask a Question)

This section describes the IGLOO® 2 FPGA development tools.

2.9.1. Design Software (Ask a Question)

Microchip's Libero® SoC is a comprehensive software toolset to design applications using the IGLOO® 2 device. Libero® SoC manages the entire design flow from design entry, synthesis and simulation, place and route and timing and power analysis, with enhanced integration of the embedded design flow.

System designers can leverage the easy-to-use Libero® SoC that includes the following features:

- System Builder for creation of system-level architecture
- Synthesis, DSP and debug support from Synopsys®
- Simulation from Mentor Graphics
- Push-button design flow with power analysis and timing analysis
- SmartDebug for access to non-invasive probes within the IGLOO® 2 devices

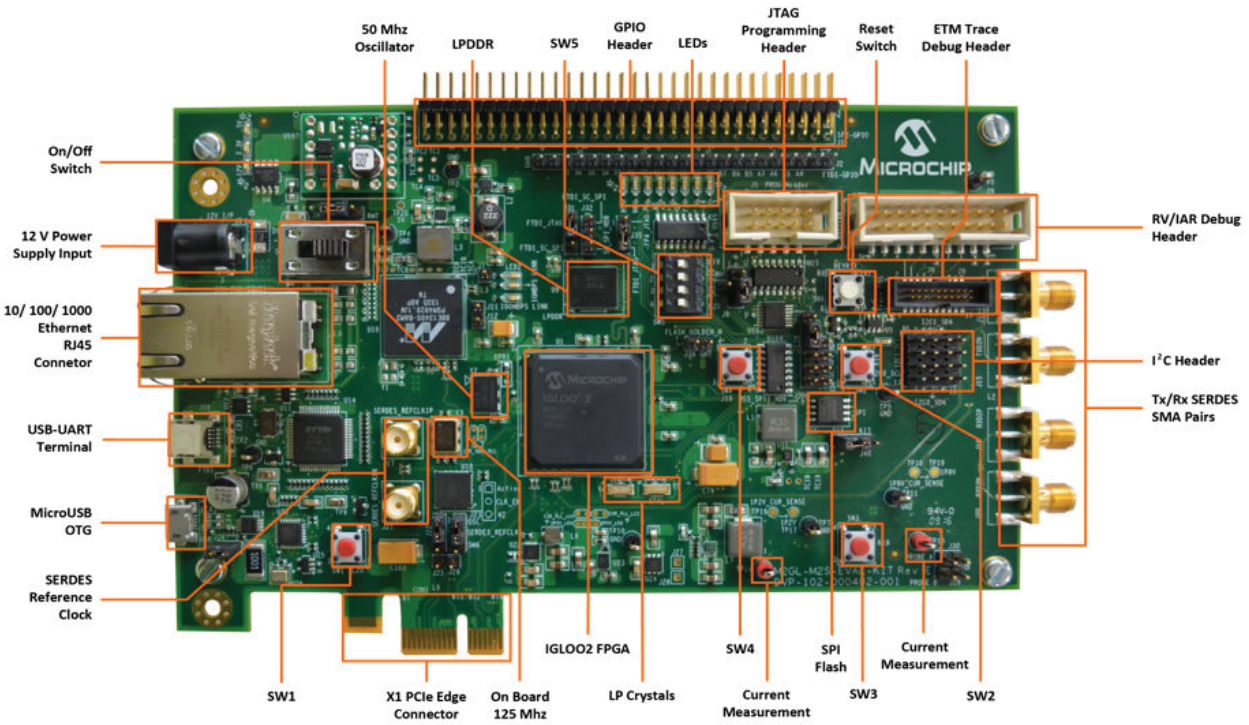
For more information, see Libero SoC.

2.9.2. Design Hardware (Ask a Question)

Microchip's IGLOO® 2 Evaluation Kit (M2GL-EVAL-KIT) is a low-cost platform to evaluate various features offered by the IGLOO® 2 devices; see the following figure.

Th ekit includes a M2GL010T-1FGG484 device. The board includes an RJ45 interface to 10/100/1000 Ethernet, 512-Mb LPDDR, 64-Mb SPI Flash, USB-UART connections as well as I2C, SPI and GPIO headers. The kit includes a 12V power supply but can also be powered through the PCIe® edge connector. The kit also includes a FlashPro4 JTAG programmer for programming and debugging.

Figure 2-1. IGLOO® 2 Evaluation Kit



2.9.3. IP Cores (Ask a Question)

Microchip offers many soft peripherals that can be placed in the FPGA fabric of the device. These include Core429, Core1553, CoreJESD204BRX/TX, CoreFRI, CoreFFT and many other DirectCores. For more information, see IP Cores.

3. Revision History (Ask a Question)

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

Table 3-1. Revision History

Revision	Date	Description
A	08/2025	The following is the list of changes made in Revision A of this document: • Document is updated as per Microchip publishing format. • The document number has changed from 51700135 to DS50003921. • Instances of Microsemi have been replaced with Microchip throughout the document. • As per Microchip terminology updates, replaced slave with client and master with host throughout the document
4	10/2015	The following is the list of changes made in Revision 4 of this document: • Updated Figure 1-1 (SAR 71996) and Table 1-1 (SAR 71996) in the Block Diagram section. • Updated Figure 1-2 (SAR 71996) in the Ordering Information section. • Updated the Marking Specification Details section (SAR 71996). • Updated the Low Power section (SAR 71996). • Changed memory values for LPDDR and SPI Flash in the Design Hardware section (SAR 71996).
3	06/2015	The following is the list of changes made in Revision 3 of this document: • Removed 5G SerDes and instances of XAUI support (SAR 68716). • Updated the SerDes Interface section (SAR68716).
2	06/2015	The following is the list of changes made in Revision 2 of this document: • Changed the document title from “Automotive Grade IGLOO 2 FPGAs Product Brief” to “Automotive Grade 2 IGLOO 2 FPGAs Product Brief” (SAR 68571). • Changed Grade 2 temperature from −40°C–135°C T_J to −40°C–125°C T_J (SAR 68571).
1	06/2015	Initial release

Microchip FPGA Support

Microchip FPGA products group backs its products with various support services, including Customer Service, Customer Technical Support Center, a website, and worldwide sales offices. Customers are suggested to visit Microchip online resources prior to contacting support as it is very likely that their queries have been already answered.

Contact Technical Support Center through the website at www.microchip.com/support. Mention the FPGA Device Part number, select appropriate case category, and upload design files while creating a technical support case.

Contact Customer Service for non-technical product support, such as product pricing, product upgrades, update information, order status, and authorization.

- From North America, call **800.262.1060**
- From the rest of the world, call **650.318.4460**
- Fax, from anywhere in the world, **650.318.8044**

Microchip Information

Trademarks

The "Microchip" name and logo, the "M" logo, and other names, logos, and brands are registered and unregistered trademarks of Microchip Technology Incorporated or its affiliates and/or subsidiaries in the United States and/or other countries ("Microchip Trademarks"). Information regarding Microchip Trademarks can be found at https://www.microchip.com/en-us/about/legal-information/microchip-trademarks.

ISBN: 979-8-3371-1801-7

Legal Notice

This publication and the information herein may be used only with Microchip products, including to design, test, and integrate Microchip products with your application. Use of this information in any other manner violates these terms. Information regarding device applications is provided only for your convenience and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. Contact your local Microchip sales office for additional support or, obtain additional support at www.microchip.com/en-us/support/design-help/client-support-services.

THIS INFORMATION IS PROVIDED BY MICROCHIP "AS IS". MICROCHIP MAKES NO REPRESENTATIONS OR WARRANTIES OF ANY KIND WHETHER EXPRESS OR IMPLIED, WRITTEN OR ORAL, STATUTORY OR OTHERWISE, RELATED TO THE INFORMATION INCLUDING BUT NOT LIMITED TO ANY IMPLIED WARRANTIES OF NON-INFRINGEMENT, MERCHANTABILITY, AND FITNESS FOR A PARTICULAR PURPOSE, OR WARRANTIES RELATED TO ITS CONDITION, QUALITY, OR PERFORMANCE.

IN NO EVENT WILL MICROCHIP BE LIABLE FOR ANY INDIRECT, SPECIAL, PUNITIVE, INCIDENTAL, OR CONSEQUENTIAL LOSS, DAMAGE, COST, OR EXPENSE OF ANY KIND WHATSOEVER RELATED TO THE INFORMATION OR ITS USE, HOWEVER CAUSED, EVEN IF MICROCHIP HAS BEEN ADVISED OF THE POSSIBILITY OR THE DAMAGES ARE FORESEEABLE. TO THE FULLEST EXTENT ALLOWED BY LAW, MICROCHIP'S TOTAL LIABILITY ON ALL CLAIMS IN ANY WAY RELATED TO THE INFORMATION OR ITS USE WILL NOT EXCEED THE AMOUNT OF FEES, IF ANY, THAT YOU HAVE PAID DIRECTLY TO MICROCHIP FOR THE INFORMATION.

Use of Microchip devices in life support and/or safety applications is entirely at the buyer's risk, and the buyer agrees to defend, indemnify and hold harmless Microchip from any and all damages, claims, suits, or expenses resulting from such use. No licenses are conveyed, implicitly or otherwise, under any Microchip intellectual property rights unless otherwise stated.

Microchip Devices Code Protection Feature

Note the following details of the code protection feature on Microchip products:

- Microchip products meet the specifications contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is secure when used in the intended manner, within operating specifications, and under normal conditions.
- Microchip values and aggressively protects its intellectual property rights. Attempts to breach the code protection features of Microchip products are strictly prohibited and may violate the Digital Millennium Copyright Act.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of its code. Code protection does not mean that we are guaranteeing the product is “unbreakable”. Code protection is constantly evolving. Microchip is committed to continuously improving the code protection features of our products.