PolarFire® FPGA Product Overview

Overview (Ask a Question)

PolarFire® FPGAs are the fifth-generation family of non-volatile FPGA devices from Microchip, built on state-of-the-art 28 nm non-volatile process technology. Cost-optimized PolarFire FPGAs deliver the lowest power at mid-range densities. PolarFire FPGAs lower the cost of mid-range FPGAs by integrating the industry's lowest power FPGA fabric, lowest power 12.7 Gbps transceiver lane, built-in low power dual PCI Express Gen2 (EP/RP), and, on select data security (S) devices, an integrated low-power crypto co-processor. PolarFire FPGAs can operate at 1.0 V and 1.05 V, offering the end user the ability to trade off power and performance to match the application requirements.

The PolarFire family now includes cost-optimized core devices for applications that don't require high-speed serial transceivers. These FPGAs offer up to 480K logic elements with a wide range of packaging options, fast I/O, and configuration flexibility to meet diverse performance, power, and cost requirements.

This document describes the features of the production PolarFire FPGA extended commercial (0 °C to 100 °C) and industrial (–40 °C to 100 °C) device offerings. Also included is the device offering for military temperate (–55 °C to 125 °C) grade and automotive (–40 °C to 125 °C) grade devices. See section PolarFire FPGA Device Offerings for military and automotive device offering. See the datasheet for current silicon status and electrical characteristics.

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1. Summary of Features (Ask a Question)

- Up to 481K logic elements consisting of a 4-input look-up table (LUT) with a fractureable D-type flipflop
- 20 Kb dual- or two-port large static random access memory (LSRAM) block with built-in single error correct double error detect (SECDED)
- 64 × 12 two-port µRAM block implemented as an array of latches
- 18 × 18 math block with a pre-adder, a 48-bit accumulator, and an optional 16 deep x 18 coefficient ROM
- Built-in µPROM, modifiable at program time, readable at run time for user data storage
- High-speed serial connectivity with built-in multi-gigabit multi-protocol transceivers from 250 Mbps to 12.7 Gbps
- Integrated dual PCIe for up to ×4 Gen2 endpoint (EP) and root port (RP) designs
- High-speed I/O (HSIO) supporting up to 1600 Mbps DDR4, 1333 Mbps DDR3L, and 1333 Mbps LPDDR3/DDR3 memories with integrated I/O digital
- General purpose I/O (GPIO) supporting 3.3 V, built-in CDR for serial gigabit Ethernet, 1067 Mbps DDR3, and 1600 Mbps LVDS I/O speed with integrated I/O digital logic
- Low-power phase-locked loops (PLLs) and delay-locked loops (DLLs) for high precision and low-jitter
- 1.0 V and 1.05 V operating modes

1.1. Low-Power Features (Ask a Question)

- Low device static power
- Low inrush current
- Low power transceivers

1.2. Reliability Features (Ask a Question)

- FPGA configuration cells single event upset (SEU) immune
- Built-in SECDED and memory interleaving on LSRAMs
- System controller suspend mode for safety-critical designs

1.3. Security Features (Ask a Question)

- Cryptography Research Incorporated (CRI)-patented differential power analysis (DPA) bitstream protection
- Integrated physically unclonable function (PUF)
- 56 Kbytes of secure non-volatile memory (sNVM)
- Built-in tamper detectors and countermeasures
- Digest integrity check for FPGA, µPROM, and sNVM
- Data security features in S devices—true random number generator, integrated Athena's TeraFire® EXP5200B Crypto Coprocessor, suite B capable, and CRI DPA countermeasure pass-through license

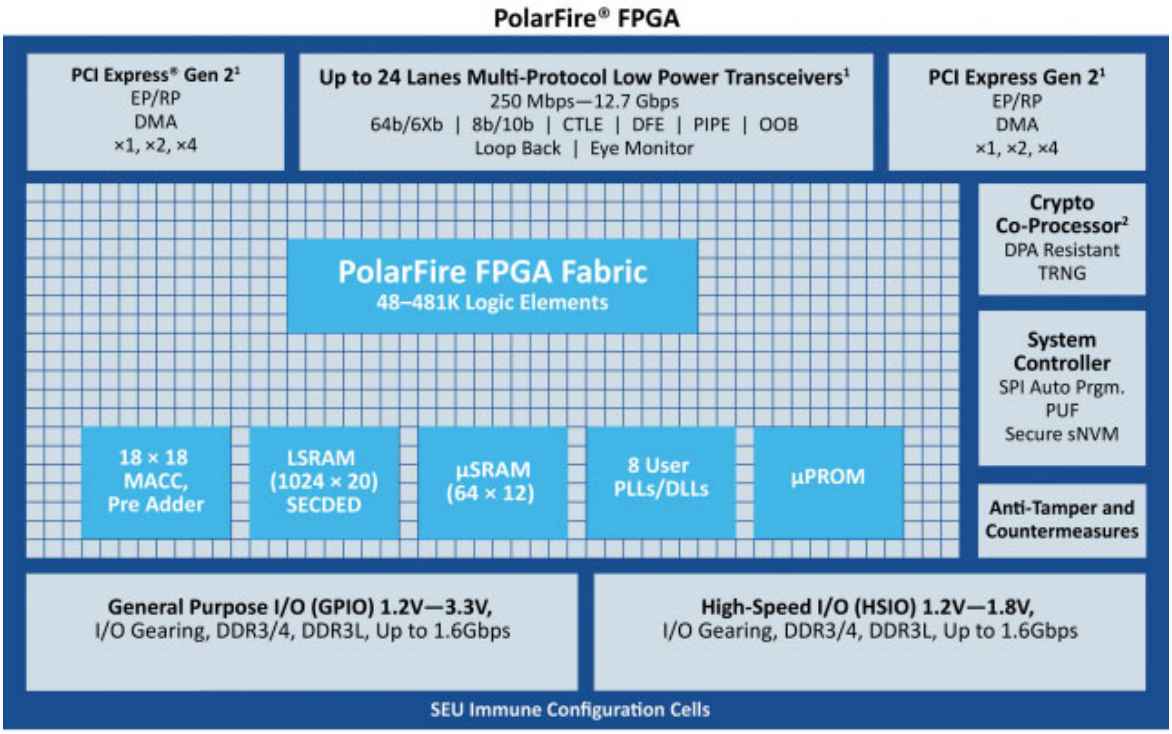
1.4. Libero® SoC PolarFire FPGA Toolset (Ask a Question)

- Complete FPGA and embedded software development environment
- Includes Synplify Pro synthesis and Mentor ModelSim ME simulation

2. Block Diagram (Ask a Question)

The following illustration shows the functional blocks of PolarFire FPGAs.

Figure 2-1. PolarFire FPGA Block Diagram



Notes:
1. PCIe® and Transceivers **not available** in PolarFire Core devices
2. DPA-Safe Crypto Co-Processor supported in S devices
3. PolarFire Core devices are available in STD speed only. Refer to STD speed I/O specs for core devices.

3. Product Family Table (Ask a Question)

The following table lists the product overview and packaging overview of the PolarFire FPGA product family.

Table 3-1. PolarFire FPGA Product Family

Features	MPF050T	MPF100T	MPF200T	MPF300T	MPF500T
K Logic elements (4 LUT + DFF)	48	109	192	300	481
Math blocks (18 x 18 MACC)	150	336	588	924	1480
LSRAM blocks (20 kbit)	160	352	616	952	1520
µSRAM blocks (64 x 12)	450	1008	1764	2772	4440
Total RAM (Mbits)	3.6	7.6	13.3	20.6	33
µPROM (Kbits)	216	297	297	459	513
User DLLs/PLLs	8	8	8	8	8
250 Mbps to 12.7 Gbps SERDES lanes*	4	8	16	16	24
PCIe Gen2 endpoints/root ports*	2	2	2	2	2
Total user I/Os	188	284	368	512	584
Type/Size/Pitch - Commercial/Industrial	**Total User I/Os (HSIO/GPIO), SGMII CDRs/Transceivers**				
FCSG325 0.5 mm 11 mm x 11 mm, 11 mm x 14.5 mm*	164(84/80), 6/4	170(84/86), 7/4	170(84/86), 7/4*	—	—
FCSG536 0.5 mm 16 mm x 16 mm	—	—	300(120/180), 15/4	300(120/180), 15/4	—
FCVG484 0.8 mm 19 mm x 19 mm	188(96/92), 7/4	284(120/164), 13/4	284(120/164), 13/4	284(120/164), 13/4	—
FCG484 1.0 mm 23 mm x 23 mm	—	244(96/148), 12/8	244(96/148), 12/8	244(96/148), 12/8	—
FCG784 1.0 mm 29 mm x 29 mm	—	—	364(132/232), 18/16	388(156/232), 18/16	388(156/232), 18/16
FCG1152 1.0 mm 35 mm x 35 mm	—	—	—	512(276/236), 19/16	584(324/260), 19/24
Type/Size/Pitch - Military	**Total User I/Os (HSIO/GPIO), SGMII CDRs/XCVRs**				
FCS325 0.5 mm 11 mm x 14.5 mm	—	—	170(84/86), 7/4*	—	—
FCS536 0.5 mm 16 mm x 16 mm	—	—	—	300(120/180), 15/4	—
FCV484 0.8 mm 19 mm x 19 mm	—	—	—	284(120/164), 13/4	—
FC484 1.0 mm 23 mm x 23 mm	—	—	—	244(96/148), 12/8	—
FC784 1.0 mm 29 mm x 29 mm	—	—	—	388(156/232), 18/16	388(156/232), 18/16

Table 3-1. PolarFire FPGA Product Family (continued)

Features	MPF050T	MPF100T	MPF200T	MPF300T	MPF500T
FC1152 1.0 mm 35 mm x 35 mm	—	—	—	—	584(324/260), 19/24
Type/Size/Pitch - Automotive	**Total User I/Os (HSIO/GPIO), SGMII CDRs/XCVRs**				
FCSG325 0.5 mm 11 mm x 11 mm, 11 mm x 14.5 mm*	164(84/80), 6/4	170(84/86), 7/4	170(84/86), 7/4*	—	—
FCSG536 0.5 mm 16 mm x 16 mm	—	—	300(120/180), 15/4	300(120/180), 15/4	—
FCVG484 0.8 mm 19 mm x 19 mm	188(96/92), 7/4	284(120/164), 13/4	284(120/164), 13/4	284(120/164), 13/4	—
FCG484 1.0 mm 23 mm x 23 mm	—	244(96/148), 12/8	244(96/148), 12/8	—	—
FCG784 1.0 mm 29 mm x 29 mm	—	—	—	—	388(156/232), 18/16
FCG1152 1.0 mm 35 mm x 35 mm	—	—	—	—	—

Notes:

- Devices in the same package and family type are pin compatible.
- TS devices contain an Athena's TeraFire® F5200B Crypto-Coprocessor.
- Extended commercial and industrial temperature grade devices are available in Green RoHS packages. Military temperature grade devices are available in leaded packages.
- See section PolarFire FPGA Device Offerings for legal device family ordering combinations for Low Power "L" devices and Data Security "S" devices.
- FCSG325 package has dimensions of 11 mm × 11 mm for MPF050 and MPF100 devices, and 11 mm × 14.5 mm for MPF200 devices.
- SERDES lanes and PCIe Gen2 endpoints/root ports are not available for the PolarFire core series.

4. Non-Volatile FPGA Fabric (Ask a Question)

The non-volatile FPGA fabric is built on state-of-the-art 28 nm low power non-volatile process technology. The PolarFire FPGA fabric is composed of the following building blocks:

- Logic element
- On-chip memory (LSRAM, µSRAM, sNVM, and µPROM)
- Math block

The FPGA fabric configuration cells are SEU immune and are used to configure I/Os and other aspects of the device. Non-volatile FPGAs do not require the configuration process inherent in SRAM FPGAs. Non-volatile FPGAs power-up quickly like an ASIC with minimal inrush current, and are ideal for root-of-trust first-up functionality in any system.

4.1. Logic Element (Ask a Question)

The 4-input LUT can be configured either to implement any 4-input combinatorial function or to implement an arithmetic function where the LUT output is XORed with a carry input to generate the sum output.

The logic element has the following features.

- A fully permutable 4-input LUT optimized for lowest power
- A dedicated carry chain based on a carry look-ahead technique
- A separate flip-flop that can be used independently from the LUT

4.2. On-Chip Memory (Ask a Question)

PolarFire FPGAs integrate four different types of memories that allow the designer to optimize for power, functionality, and area. Two memory types are volatile and two memory types are non-volatile.

Volatile memories include:

- LSRAM
- µSRAM

The LSRAMs are 20 Kbit SRAMs with a built-in SECDED and interleaving to prevent multi-bit-upsets (MBUs). The µSRAMs are small distributed 64 x 12 RAMs, well suited for efficient implementation of small buffers, thereby reserving LSRAM usage for the wider and deeper memories.

Non-volatile memories (NVMs) include:

- µPROM
- sNVM

The µPROM, constructed of SEU-immune FPGA configuration non-volatile cells, is readable at runtime and writable during device programming. It provides users with SEU-immune parameters, constants, IDs, and parametric or initialization data. The sNVM is accessible through system service calls. Data written to the sNVM can be protected by the PUF. The sNVM is readable and writable by the designer's application during runtime and is an ideal storage location for the boot code for soft processors and user keys.

4.3. LSRAM (Ask a Question)

Each LSRAM block consists of 20,480 bits of RAM and includes functionality to support dual-port and two-port modes. There are numerous configurations and features for each block. The Libero SoC PolarFire toolset has an LSRAM configurator that provides automated combining and cascading of several LSRAM blocks into larger memories.

LSRAM features include:

- 428 MHz operation
- True dual-port memory
- Two-port memory (one dedicated write port and one dedicated read port)
- Data widths of ×1, ×2, ×5, ×10, ×20, ×40, and ×33 with SECDED enabled
- Multi-bit-upset mitigation
- Synchronous operation
- Independent port clocks
- Byte enables
- Registered inputs
- Output registers with separate enables and synchronous resets
- Read enables to conserve power while retaining output data
- Power switch to minimize static power when the LSRAM is not used
- Fast zeroization mode

4.3.1. Dual-Port Mode (Ask a Question)

In dual-port mode, the width of both ports is less than 33 and the ports are independent of each other. The write and read operations can occur independently of each other, at any location. On write collisions, while the write operations occur correctly, the read operations can return ambiguous results while the write completes. After completing the write operation, the read data reads the newly written write data correctly.

4.3.2. Two-Port Mode (Ask a Question)

In two-port mode, at least one port has a width of 32 or 40 (or 33 with SECDED). Port A is dedicated for reads and port B for writes.

The following illustration shows port widths in various modes.

Figure 4-1. LSRAM Dual- and Two-Port Configurations

Port B Width \ Port A Width	x1/x1	x1/x2	x1/x4	x1/x8	x1/x16	W1/R32	N/A
	x2/x1	x2/x2	x2/x4	x2/x8	x2/x16	W2/R32	N/A
	x4/x1	x4/x2	x5/x5	x5/x10	x5/x20	W5/R40	N/A
	x8/x1	x8/x2	x10/x5	x10/x5	x10/x20	W10/R40	N/A
	x16/x1	x16/x2	x20/x5	x20/x10	x20/x20	W20/R40	N/A
	W32/R1	W32/R2	W40/R5	W40/R10	W40/R20	W40/R40	N/A
	N/A	N/A	N/A	N/A	N/A	N/A	Wx33/R33

Dual Port
Two Port
Two Port SECDED

4.4. µSRAM (Ask a Question)

The µSRAM is a two-port memory embedded in the FPGA fabric, which is provided for an efficient low-power implementation for small buffers. On write collisions, the write operations occur correctly, while the read operations can return ambiguous results while the write completes. After completing the write operation, the read data reads the newly written write data.

The following are key features of the µSRAM block:

- 480 MHz operation
- Two-port memory with 64 words of 12 bits
- The write port operates synchronously
- The write port has a fixed width
- The read port operates asynchronously and supports synchronous and pipeline operations with the FPGA fabric flip-flops
- The Libero SoC PolarFire toolset provides automated combining and cascading for larger memories
- Multiple memory blocks can be combined to extend the depth or width
- Provides a state-keeping, low-power suspend mode
- Implemented as an array of latches

4.5. µPROM (Ask a Question)

The µPROM is a single monolithic non-volatile memory that provides a PROM-like storage for a variety of purposes, including but not limited to: initialization data for other memories, user calibration data, and so on. The memory cells are constructed from the FPGA configuration cells and are updated when the device is programmed.

The following are key features of the µPROM:

- 10 ns read access time
- Programmed with the FPGA bitstream
- Asynchronous or synchronous read access mode from the FPGA fabric

4.6. sNVM (Ask a Question)

Each PolarFire FPGA has 56 Kbytes of sNVM. The sNVM is organized into 221 pages of 236 or 252 bytes, depending on whether the data is stored as plain text or encrypted/authenticated data. It is accessible to users through system services calls to the PolarFire FPGA system controller. Pages within the sNVM can be marked as ROM during bitstream programming. The sNVM content can be used to initialize LSRAM and µSRAMs with secure data. The sNVM is only accessible through system service calls. Data written to the sNVM can be protected by the PUF.

4.7. Math Block (Ask a Question)

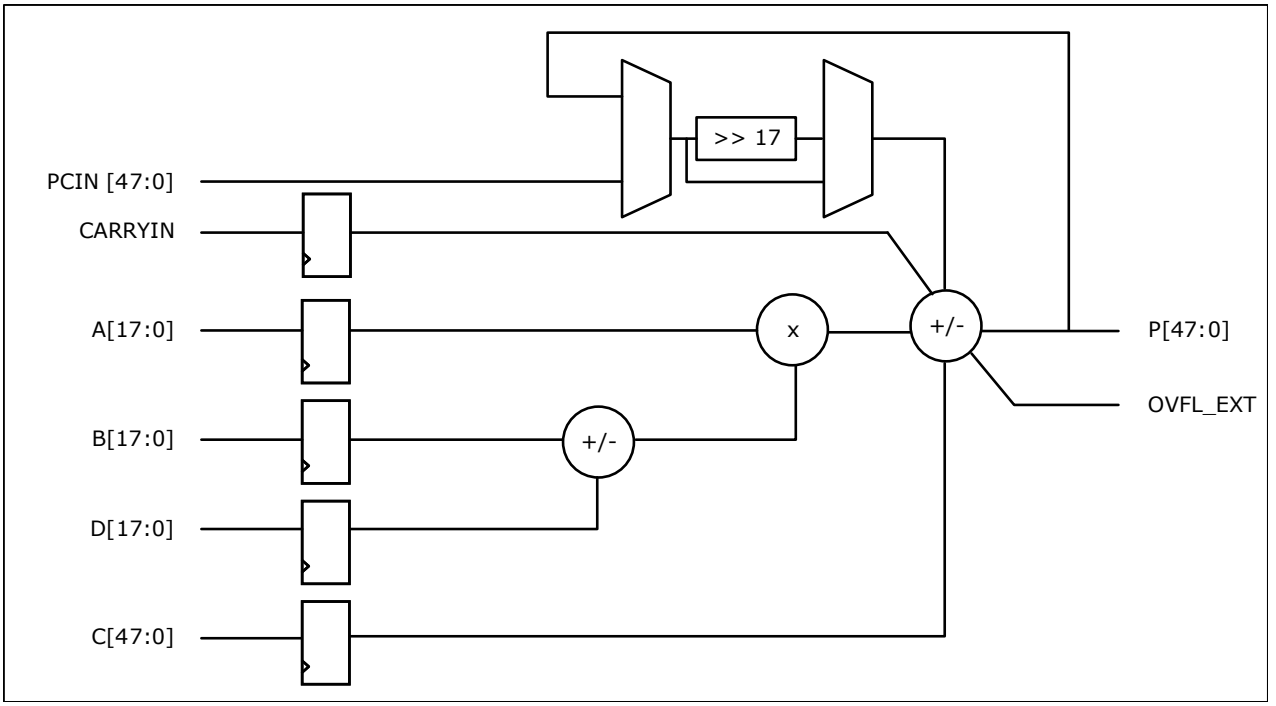
The fundamental building block in any digital signal processing algorithm is the multiply-accumulate (MACC) operation. PolarFire FPGAs implement a custom 18 x 18 MACC block for an efficient low-power implementation of complex DSP algorithms such as finite impulse response (FIR) filters, infinite impulse response (IIR) filters, and fast fourier transform (FFT) for filtering and image processing applications. An optional 16-word coefficient ROM can be constructed from logic elements located near the math block.

The following are key features of the math block functionality:

- 500 MHz operation
- 18 × 18 two's complement multiplier accumulator with an output width of 48 bits
- Power-saving pre-adder to optimize linear phase FIR filter applications and reduce the math block usage
- Optional pipelining and dedicated buses for cascading
- Dot-product mode for complex multiplies

Figure 4-2 shows the functional blocks of the math block.

Figure 4-2. Math Block



5. Clock Management (Ask a Question)

In each PolarFire FPGA, there are eight DLLs and eight PLLs to provide flexible clock generation and management capabilities. In addition to these DLLs and PLLs, up to 15 transceiver lane transmit PLLs are also available.

The following are key highlights of the clock management architecture:

- High-speed buffers and routing for low-skew clock distribution
- Frequency synthesis and phase shifting
- Low-jitter clock generation and jitter filtering

5.1. DLL (Ask a Question)

The DLL provides a calculated PVT compensated delay to the I/O's digital delay lines as well as delay or phase-shifted clocks to the FPGA fabric.

The following are the major modes to which the DLL can be configured.

- Time reference mode—the DLL takes a single clock as an input and determines how many delay line buffer taps are required for a signal to pass through them to rotate a signal. The main use of time reference mode is to know how many delay taps are needed to delay the clock by 90 degrees. The value is then provided to the data strobe signal (DQS)/DQSn input signals for double data rate (DDR) memory controllers to delay all DQS/DQSn signals by the required 90-degree phase shift to capture the data from the memory devices. Multiple memory interfaces of the same clock rate can reuse the same DLL with lane level controls for PVT updates.
- Clock injection delay mode—the DLL can be used to compensate for the clock injection delay associated with the source synchronous receive interfaces. The DLL can match delays for the global, regional, and high-speed bank clocks. There are two outputs from the DLL in this mode: a x1 output fixed in time and another output that can be divided by x1, x2, or x4 and can be phase shifted.

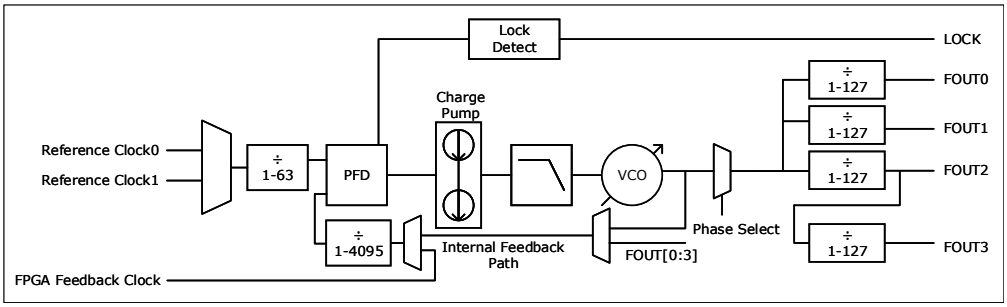
5.2. PLL (Ask a Question)

The programmable delta-sigma low-jitter fractional PLLs are multi-function and general purpose frequency synthesizers, as shown in Figure 5-1. Wide input and output ranges along with the best-in-class jitter performance allow these PLLs to be used for almost any clocking application. With excellent supply noise immunity, the PLL is ideal for use in noisy FPGA environments.

- The PLL output clock is available in eight phases with 45-degree phase differences. All eight phases are selectable to drive four separate outputs from the PLL, where each output can select any of the eight phases independent of other output selections and that each output can also be driven to a zero output when not used.
- Each of the four outputs from the PLL can then be divided independently for any value from 1 to 127. Each of the PLL outputs can have the output divider released by up to seven VCO/4 cycles. The delayed outputs can be set independently for each output clock.
- Fractional-N (24-bit accuracy) capability is added to the feedback divider to have the VCO frequency be a non-integer divide of the reference clock input frequency. The base frequency is applied to all PLL outputs.
- The PLL supports glitch-free start and stop on any one of the four outputs independently by either a register map or a fabric control. This capability also allows the output divider values and the VCO/4 phase selection to be modified glitch-free during the time that the clock is stopped.
- For fine granularity phase control of the PLLs, they can be cascaded with DLLs located near the PLLs, whereby the DLL delay lines can be used in a process, voltage, and temperature (PVT) compensated or non-PVT compensated mode to provide the phase control needed.

The following illustration shows the flow of the PLL functionality.

Figure 5-1. PLL Block Diagram



5.3. Clock Network (Ask a Question)

The clock network is designed to route clocks and asynchronous reset signals to large sections of the fabric with limited skew. On occasion, the network can also be used for other high fanout signals that can tolerate long delays, such as non-timing-critical synchronous enables or resets. There are two main clock networks for the FPGA fabric, global and regional clocks.

5.3.1. Global Clocks (Ask a Question)

There are 24 clocks on the device with global low skew scope to all synchronous elements. The global can be divided into left and right sides of the device. Thus, the number of globals can increase to 48 total clocks with 24 in the left and 24 in the right.

5.3.2. Regional Clocks (Ask a Question)

There are up to 38 regional clock domains that interface to the edges of the device. The regional clocks provide a fixed number of logic elements based on the size of the device. Up to 14 clocks are available for the FPGA I/Os and up to 24 clocks for the transceiver lanes, one for each lane direction. These are the fast insertion clock networks used to move data in and out of the fabric.

6. I/Os (Ask a Question)

PolarFire device user I/Os support multiple I/O standards while providing the high bandwidth needed to maximize the internal logic capabilities of the device and achieve the required system-level performance.

6.1. Low-Power, High-Speed Transceiver Lane (Not Applicable to PolarFire Core FPGA Devices) (Ask a Question)

All PolarFire FPGAs contain state-of-the-art low-power transceiver lane capabilities from speeds as low as 250 Mbps up to 12.7 Gbps. The PMA is designed to support multiple protocols (as listed in the following table) with state-of-the-art control and debug features. PCI Express Gen1 or Gen2 support is provided by a hard macro. All other protocols are implemented with a soft IP. Serial Gigabit Ethernet is also supported with GPIO 3.3 V LVDS differential pairs. A single transmit PLL can provide a high-speed clock up to four transceiver lanes.

Table 6-1. Transceiver Lane Protocol Support

Protocol	Data Rate (Gbps)	Channels Bonded
PCIe	2.5, 5	1, 2, 4
Interlaken	6.375, 12.7	1–16
10GBASE-R/KR	10.3125–12.7	1
SGMII/QSGMII	1.25–5	1
XAUI	3.125	4
RXAUI	6.25	2, 3, 4, 6
HiGig/HiGig+/HiGiGII	3.75–4.065	4
CPRI	0.6144–12.165	1
Fiber channel	0.6144–12.165	1
SRIO	1.25–6.3	1, 2, 4, 8
SATA	1.5–6	1
JESD204B	0.5–12.5	1–4
Display port	2, 5, 8	4
SDI	0.277–11.88	1

6.1.1. Low-Power Transceiver Lane Features (Ask a Question)

The following are low-power transceiver lane features:

- Advanced low-power modes
- Programmable transmit amplitude and emphasis control
- Low-speed CDR operation with support for 270 Mbps SMPTE serial line rates
- Continuous time linear equalization (CTLE) and decision feedback equalization (DFE) for long-reach or backplane applications
- Auto-adaption at receiver equalization and integrated eye monitor feature for easy serial link tuning
- Eye monitor and/or equalization can be powered down to reduce power if not needed
- Out-of-band, electrical idle signaling capability for SAS, SATA, and PCIe
- Multiple loopback modes for test and debug
- Transmit jitter attenuation for loop timing applications (SyncE compatible)

- Hot-socketing capable
- IEEE 1149.6 AC JTAG
- Adjacent channel loopback modes allow transceiver lane data streams to remain active during FPGA fabric programming

6.1.2. Transmitter (Ask a Question)

The transmitter is fundamentally a parallel-to-serial converter with a conversion ratio of 8, 10, 16, 20, 32, 40, 64, or 80 bits. It allows the designer to trade-off data path width for timing margin in high-performance designs. These transmitter outputs drive the PC board with a differential output signal. TX_CLK is the appropriately divided serial data clock available to the fabric, and can be used directly to register the parallel data coming from the internal logic. The transmit parallel data has additional hardware support for the 8b/10b, 64b/66b, or 64b/67b encoding schemes to provide a sufficient number of transitions. The bit-serial output signal drives two package pins with differential signals. The output signal pair supports a wide variety of serial protocols and has programmable signal swing as well as programmable pre- and post-emphasis to compensate for PC board losses and other interconnect characteristics. For shorter channels, the swing can be reduced to lower power consumption. Each transmit lane can be sourced by one of two transmit PLLs. Each transmit PLL can drive up to four transceiver lanes. Transmitter PLLs are state-of-the-art fractional frequency synthesizers with integrated jitter attenuation.

6.1.3. Receiver (Ask a Question)

The receiver is fundamentally a serial-to-parallel converter with clock recovery changing the incoming bit-serial differential signal into a parallel stream of words of 8, 10, 16, 20, 32, 40, 64, or 80 bits. This allows the FPGA designer to trade off the internal data path width versus logic timing margin. The receiver takes the incoming differential data stream, feeds it through programmable linear and decision feedback equalizers (to compensate for PC board and other interconnect characteristics), and uses the reference clock input to initiate clock recognition. The data pattern uses non-return-to-zero (NRZ) encoding and optionally guarantees sufficient data transitions by using the selected encoding scheme. The outgoing parallel data has additional hardware support for the 8b/10b, 64b/66b, or 64b/67b encoding schemes to provide a sufficient number of transitions. Parallel data is transferred into the FPGA logic using the recovered clock (RX_CLK).

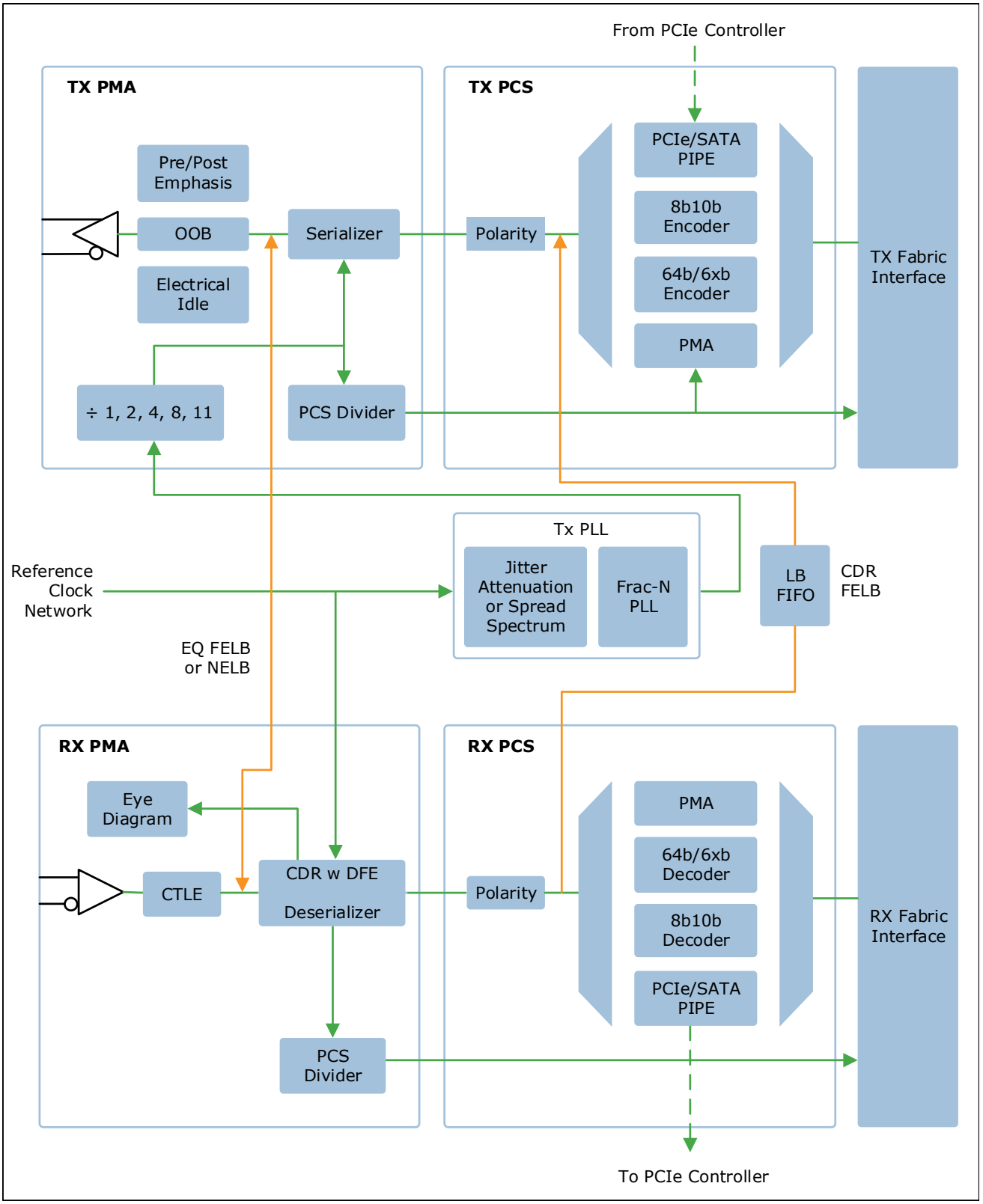
6.1.4. Transceiver Lane Modes (Ask a Question)

The transceiver lane supports five different modes of operations:

- PMA—direct access to the PMA without any encoding
- 8b/10b—8b/10b encoding/decoding is provided
- 64b/6xb—64b/66b or 64/67b encoding/decoding with gearbox logic is provided
- PIPE—a PIPE interface supporting both PCIe Gen2 and SATA 3.0
- PCIe—direct connection to the embedded PCIe Gen2 controller

Figure 6-1 shows the collaboration of five modes that transceiver lanes support.

Figure 6-1. Transceiver Lane Modes

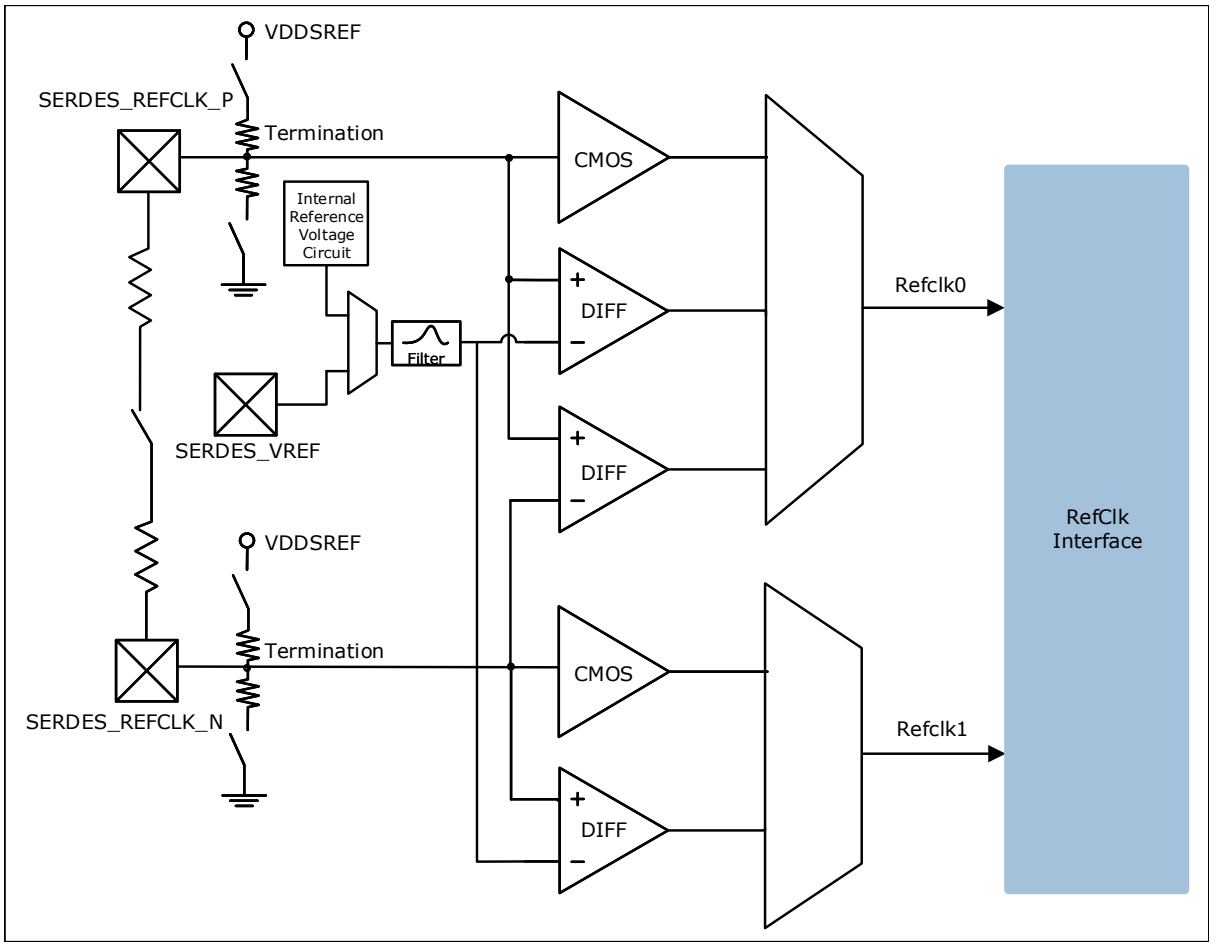


6.1.5. Reference Clock (Ask a Question)

The reference clock pins allow connections directly with the transceiver lane quads. The reference clock inputs provide flexibility to interface with both single-ended and differential clocks, and can drive up to two independent clocks per transceiver lane quad. These reference clocks can also be sources for the global and regional clock networks in the FPGA fabric of the device.

The following illustration shows the connectivity between the reference clock and transceiver lane quads.

Figure 6-2. Reference Clock



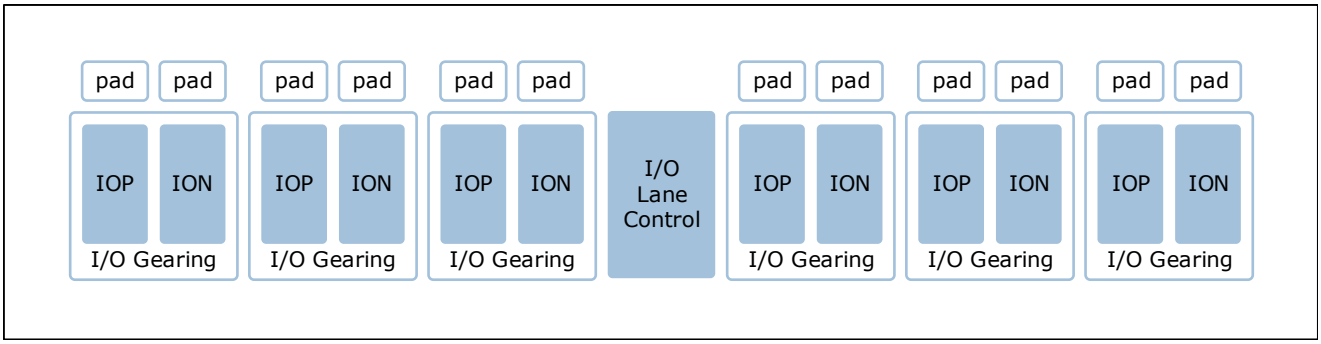
6.1.6. Quad Lane Overlay Assignments (Ask a Question)

The transceiver lane either connects the parallel side of the interface to the PCIe Gen2 controller or to the fabric. The PCIe connections are fixed in the hardware and have a dedicated number of combinations between the two controllers. The fabric interface is used to support the PMA, 8b/10b, 64b/6xb, and PIPE modes and has complete flexibility into the fabric connections. For detailed lane assignments, see UG0685: PolarFire FPGA PCI Express User Guide.

6.2. Inputs/Outputs (Ask a Question)

PolarFire FPGA I/Os are grouped into pairs to meet the differential I/O standards. Additionally, they are grouped in lanes of 12 buffers with a lane controller for memory interfaces, as shown in the following illustration.

Figure 6-3. I/O Topology



The number of I/O pins varies depending on the device and package size. The persistent I/O feature preserves a state on an I/O without user intervention during programming mode. The PolarFire FPGA I/O buffers are constructed from the following main sub modules.

- Transmit buffer (PVT compensated)
- Receive buffer
- Termination (Thevenin, Differential, Up, and Down)
- Weak pull mode logic (Up, Down, and Bus-Hold)

Each I/O is configurable and can comply with a large number of I/O standards. See the PolarFire FPGA Datasheet for specific I/O standard support and data rates. There two types of user I/Os in PolarFire FPGAs:

- High-speed I/O (HSIO) optimized for DDR4 memories at speeds up to 1.6 Gbps and a maximum voltage of 1.8 V nominal
- GPIO capable of supporting multiple standards including 3.3 V with an integrated CDR to support SGMII Ethernet applications

The following table lists the GPIO LVTTL or LVCMOS receivers that are also designed to support a limited mixed mode of operation to provide greater board I/O design flexibility. For example, if VDDIO is set to 3.3 V, the I/O receivers can operate at the lower voltage of JEDEC® standards.

Table 6-2. GPIO Mixed Receiver Mode Operation Capability

VDDIO (V)	LVCMOS33	LVCMOS25	LVCMOS18	LVCMOS15	LVCMOS12
3.3	Yes	Yes	Yes	Not available	Yes
2.5	Yes	Yes	Yes	Yes	Yes
1.8	Yes	Yes	Yes	Yes	Yes
1.5	Yes	Yes	Yes	Yes	Yes
1.2	Yes	Yes	Not available	Yes	Yes

The following table lists the HSIO mixed receiver mode capability.

Table 6-3. HSIO Mixed Receiver Mode Capability

VDDIO (V)	LVCMOS18	LVCMOS15	LVCMOS12
1.8	Yes	Yes	Yes
1.5	Yes	Yes	Yes
1.2	Not available	Yes	Yes

6.3. I/O Digital (Ask a Question)

The PolarFire FPGA I/O digital logic is used to interface between the FPGA fabric and the I/O buffers. It interfaces between the high-speed I/O buffers and lower-speed FPGA fabric. The I/O digital block consists of the following:

- A delay chain, for input or output delay
- Registers and control logic for input modes and output modes

The I/O digital registers can be configured for both input and output DDR and shift register modes and combined DDR-shift register modes. It allows gearing up the output data rate and gearing down the input data rate. The PolarFire FPGA I/O digital logic works in conjunction with fast and low-skew clock distributions that are optimized for DDR applications, special clock dividers, and other support circuits to guarantee clock domain crossings.

6.3.1. I/O Digital Features (Ask a Question)

The following are the I/O digital features:

- Programmable input and/or output delay chain
- Data eye monitor for detecting margin to clock edges
- Data eye position optimizer
- Up to 10:1 input deserialization
- Up to 10:1 output serialization
- Support for DDR and SDR interfaces
- Receive slip control to facilitate word alignment
- Fast and low-skew lane clocks per 12 I/Os
- Clock recovery for SGMII and similar interfaces (one per 12 I/Os)

7. PCI Express (Not Applicable to PolarFire Core FPGA Devices) (Ask a Question)

Each PolarFire FPGA integrates two low-power built-in PCIe Gen2 controllers, allowing seamless and easy connectivity to one or more host processors. The two PCIe controllers are shared across two quads, as shown in the following illustration. All PLLs are jitter attenuation-capable, while the SSC label indicates spread spectrum clock (SSC) capability.

7.1. PCI Express Features (Ask a Question)

The following are PCIe features:

- ×1, ×2, and ×4 lane support
- Suitable for root port, native endpoint
- PCI Express base specification revision 2.0 and 1.1 compliant
- AXI4 master and slave interfaces to the FPGA fabric
- Single function capability
- Advanced error reporting (AER) support
- Integrated clock domain crossing (CDC) to support user-selected AXI4 frequency
- Lane reversal support
- Legacy PCI power management support
- Native active state power management L0s and L1 state support
- Power management event (PME message)
- MSI and legacy INT message support
- Latency tolerance reporting (LTR)
- L1 PM sub-states with CLKREQ
- Address translation tables between the PCIe and AXI4 domains

7.2. PCI Express DMA Engines (Ask a Question)

Each PCIe controller supports the following built-in DMA modes, enabling low-power and efficient data transfer into the FPGA fabric.

- Two DMA channels
- Eight outstanding read and write requests
- Completion reordering support
- Flexible scatter-gather DMA modes, including dynamic DMA control per descriptor
- Optional DMA engine reporting to the descriptor to ease software management
- Fetching of up to three descriptors to optimize throughput

8. PolarFire FPGA System Controller (Ask a Question)

The PolarFire FPGA system controller is based on the industry-standard ARM Cortex-M3 and is only used for FPGA powerup, secure DPA safe FPGA programming, and executing and responding to system services. All internal memories are SECDED protected with background scrubbing capabilities to remove single bit errors.

8.1. System Services (Ask a Question)

System services provide the user with information about the state of the FPGA and allow the user to request the system controller to perform predefined functions using a standard Application Programming Interface (API).

Design services

- Initialize fabric RAM
- Bitstream authentication
- IAP image authentication

Data services

- sNVM read/write
- PUF emulation service
- Nonce service

Device services

- Serial number
- JTAG user code
- Design version number
- Device certificate

FPGA fabric services

- In-application programming
- Digest check

9. Debug Probe System (Ask a Question)

Two specified user I/Os can be configured (at design capture stage) as either two single-ended live probes or one differential live probe. These live probes can provide read access to any register in the FPGA fabric, to the output pipeline registers in the LSRAMs, and to all the registers in the math block in real-time without having to re-instrument the code. A snapshot of all internal probe points can be created and read out asynchronously. The live-probe feature can be considered like a two-channel oscilloscope, whose two channels can be routed out to I/Os for external observation, and to internal ports to allow fabric design observation. Selecting different probe points within the PolarFire FPGA occurs dynamically through commands over the JTAG port using SmartDebug. Reprogramming of the FPGA is not required.

The debug probe system includes the following:

- Active probe allows dynamic asynchronous read and write to a flip-flop or a probe point. This enables quick internal observation of the logic output or experimentation on how the logic will be affected by writing to a probe point.
- Memory debug allows dynamic asynchronous read and write to a µSRAM or a large SRAM block to quickly verify if the content of the memory is changing as expected.
- Probe insertion allows routing of nodes or debug points in the FPGA design externally through unused I/Os. An oscilloscope/logic analyzer can be attached to monitor them as live signals.

10. Programming (Ask a Question)

Microchip's PolarFire FPGAs have multiple programming modes designed to enable various use models. All bitstreams are always encrypted and DPA safe. Each PolarFire FPGA can be programmed using a dedicated SPI peripheral and JTAG port. All PolarFire FPGAs are typically reprogrammed in less than 60 seconds. For device specific programming timings, see the PolarFire FPGA Datasheet.

The following programming modes are supported:

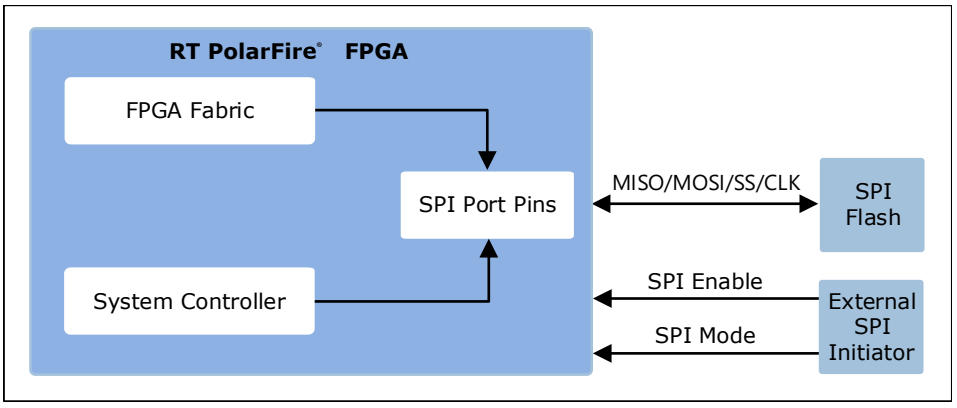
- Slave Programming
  - JTAG
  - Slave SPI—an external SPI master programs the FPGA
- SPI Master Programming—In-Application Programming (IAP)
  - Auto update feature—the system controller on power-up checks for a new bitstream in an external SPI flash and programs the FPGA.
  - Auto programming feature—on a blank device, the system controller on power-up checks for a bitstream in an external SPI flash and programs the FPGA.
  - Programming recovery feature—if remote programming fails due to a power interruption, the system controller reprograms the FPGA on the next power-up cycle from a golden bitstream (located in an external SPI flash).

10.1. Dedicated SPI Programming Port (Ask a Question)

To facilitate the use of various programming modes PolarFire FPGAs share dedicated SPI port pins between the system controller and user logic embedded in the FPGA. User logic must instantiate the User SPI macro to gain access to the pins from their design. The SPI port pins can be used as a master or slave programming port based on the signal level on the dedicated SPI mode pin. The dedicated SPI Enable pin also allows an external SPI master to program the on-board SPI flash without an external MUX by tri-stating the SPI MOSI/MISO/SS/CLK pins on the PolarFire FPGA.

The following illustration shows the SPI port facilitating the use of various programming modes.

Figure 10-1. SPI Programming Port



11. Low Power (Ask a Question)

PolarFire FPGAs offer a variety of techniques and capabilities to lower the total application power. Users can take advantage of these features to lower both capital and operational expenditures with smaller or no heat sinks, smaller or fewer fans, lower cooling costs, and so on. Additionally, the lower total power advantage can also allow the user to pack more compute operations into an existing thermal budget.

11.1. Non-Volatile Technology (Ask a Question)

Using a non-volatile complementary metal–oxide semiconductor (CMOS) technology for the FPGA configuration cells offers several power advantages over SRAM FPGA technology.

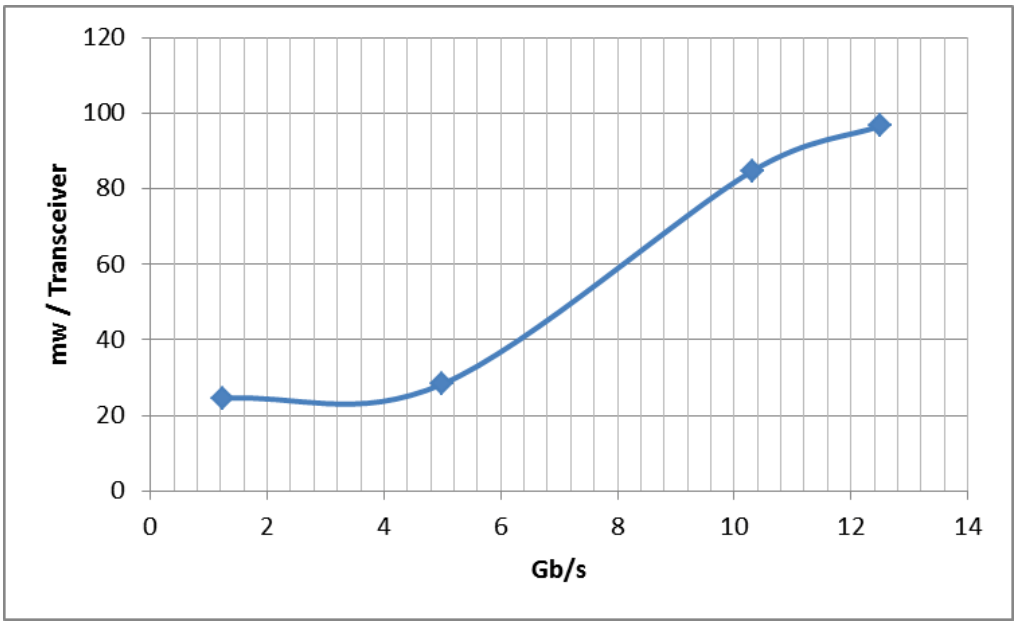
- A non-volatile switch has lower power than a SRAM switch, leading to lower static power consumption
- No SRAM configuration in-rush currents
- An external configuration component is not necessary

11.2. Low-Power Transceiver Lane (Not Applicable to PolarFire Core FPGA Devices) (Ask a Question)

PolarFire FPGAs' low-power capability is also extended to the industry's most power efficient transceiver lane, enabling 10GBASE-KR applications at less than 100 mW of power per lane. The transceiver lane has comprehensive power-down controls to optimize power consumption, including programmable amplitude and edge rate control.

The following illustration shows the connection between transceiver power and data rate.

Figure 11-1. Transceiver Power versus Data Rate



11.3. Lower Power "L" Devices (Ask a Question)

Low power (L) devices provide up to 35 percent lower static power with identical electrical specifications to the STD speed grade device. L devices can be ordered as described in the section Ordering Information.

12. Reliability (Ask a Question)

Microchip continues to offer the industry's most reliable FPGAs for your mission and safety critical applications.

12.1. FPGA Fabric (Ask a Question)

PolarFire FPGA configuration cells are inherently immune to SEUs caused by neutrons. Contrary to popular belief, shielding does not prevent a neutron from passing through an electronic system or electronic device. As semiconductor device geometry shrinks to smaller lithography, the problem of MBUs starts appearing. SRAM FPGA scrubbing techniques might be inadequate in these circumstances and while scrubbing may help, an important point is that scrubbing detects an error after the fact. The error has already occurred and propagated throughout the system. The configuration of the PolarFire FPGA fabric provides worry-free operation against random events caused by SEUs.

12.2. LSRAM (Ask a Question)

LSRAMs have built-in SECDED capability on a 32-bit word boundary. Seven additional bits are used for error correction. Two flags are provided to the user to indicate SECDED. Mitigation against multi-bit upsets is provided by keeping all cells in a word separated by a minimum distance. Applications that require scrubbing need to be accomplished with user logic. The error correction logic can be turned ON and OFF by the user to enable easy validation of the error correction operation.

12.3. µSRAM (Ask a Question)

The 64 × 12 µSRAMs are constructed from latches and are not as sensitive to SEUs as SRAMs are.

12.4. Digests (Ask a Question)

Digests verify the integrity of the programmed non-volatile data. Digests are a cryptographic hash of various data areas. Any digest that reports back an error raises the digest tamper flag.

The following are digestible non-volatile areas:

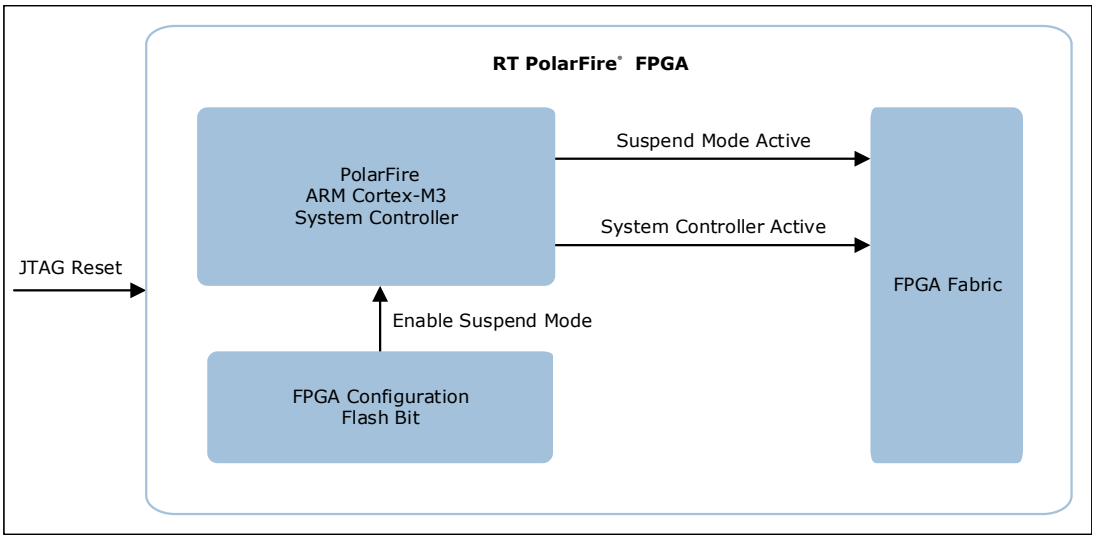
- The FPGA fabric and consequently the µPROM
- sNVM marked as ROM
- User key 1
- User key 2
- Factory parametric and key storage

12.5. System Controller Suspend Mode (Ask a Question)

For safety critical applications, PolarFire FPGAs allow the user to place the Cortex-M3-based system controller in a reset state after the FPGA has powered up. By programming an SEU configuration nonvolatile bit, the Cortex-M3 is placed in reset by a TMRed SEU immune reset latch after FPGA power-up. User logic can monitor if the suspend mode command is active and if the system controller cannot fetch instructions while in the reset state. The FPGA can be re-programmed after disabling the suspend mode by asserting the appropriate JTAG signals. The JTAG TRSTB signal must be asserted low for suspend mode to remain active.

The following illustration shows how to activate and deactivate suspend mode.

Figure 12-1. System Controller Suspend Mode



13. Security (Ask a Question)

Microchip's PolarFire FPGA and PolarFire SoC FPGAs implement layered security and represent the industry's most advanced and secure programmable FPGAs; Users may choose devices based on the level of security needed in their applications.

13.1. Hardware Security (Ask a Question)

Security considerations for an electronic system start from wafer manufacturing and continue all the way through to deployed end products. The following features provide state-of-the-art supply chain assurance in all PolarFire FPGA and PolarFire SoC FPGA devices:

- Secure supply chain management using Hardware Security Modules (HSMs) during wafer testing and packaging
- Supply chain assurance using a 768-byte digitally signed x.509 FPGA certificate embedded in every FPGA/SoC FPGA
- Microchip's Secure Production Programming Solution (SPPS) extends the secure supply chain to the customer's manufacturing flow

13.2. Design Security (Ask a Question)

The following features are available in all PolarFire FPGAs and SoC FPGAs.

- CRI patent-protected DPA countermeasures, AES-256 encrypted bitstream, and key management protocols
- Built-in tamper detection using voltage monitors, temperature monitors, clock glitch detectors, frequency monitors, JTAG active detectors, and protective meshes
- Programmable tamper responses like disabling specific I/Os, security lockdown, reset, and zeroization
- Zeroization capabilities for all on-chip memories and the FPGA fabric
- Random number generation with Physically Unclonable Function (PUF) as the source of entropy

The following features are available in select devices (referred to as "S" devices with "TS"/"TLS" in the part number)

- Root of trust implementation: digital signature service to sign user-supplied SHA-384 hash
- Read and write authenticated plain text and cipher text to secure non-volatile memory
- PUF emulation for device authentication or pseudo-random bit string generation
- Nonce service provides an alternate source of entropy using the SRAM-PUF

13.3. Data Security (Only "S" Devices) (Ask a Question)

Select PolarFire FPGAs and PolarFire SoC FPGAs ("S" devices with "TS"/"TLS" in the part number) include a TeraFire® EXP-F5200B cryptographic co-processor that enables high-speed DPA-safe cryptographic protocols at wire-line speeds. These data security features include:

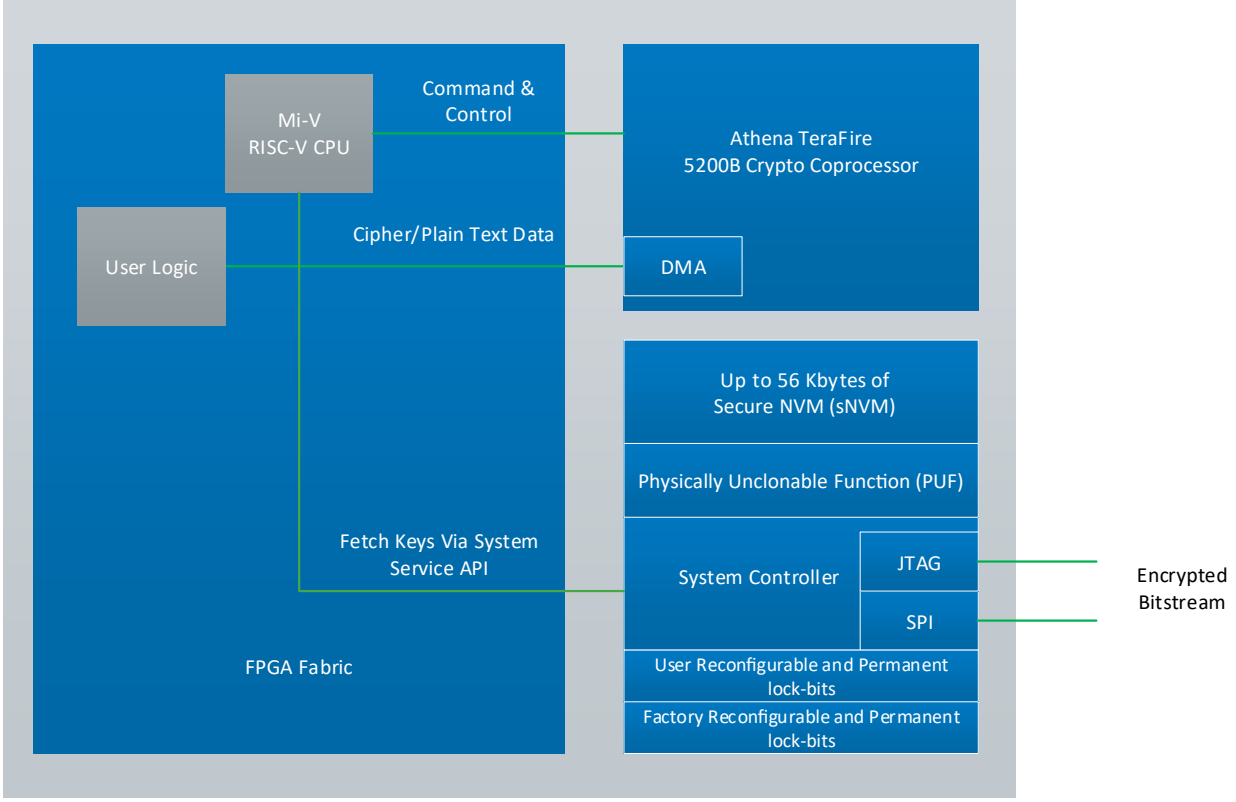
- Integrated true random number generator for modern cryptographic protocols at greater than 100 Mbps
- 189 MHz Athena TeraFire 5200B DPA-safe Crypto Coprocessor capable of implementing Suite-B+ algorithms
- CRI DPA pass-through licensing enables DPA-safe high-speed cryptographic designs in the FPGA fabric (a CRI license is included in the purchase price of the "S" device, ao there is no need to negotiate a separate license)
- NIST-certified protocols

The following are TeraFire EXP-F5200B supported protocols/features:

- TRNG (integrated): SP800-90A CTR_DRBG-256, and SP800-90B(draft) NRBG
- AES-128/192/256 E/D (ECB, CBC, CTR, OFB, CFB, CCM, GCM, KeyWrap)
- SHA-1/224/256/384/512
- HMAC-SHA-256/384/512; GMAC; CMAC
- SHA-256 Key Tree
- ECC-NIST P192/224/256/384/521 and Brainpool P256/384/512 curves with: KAS-ECC CDH; ECDSASigGen, SigVer, PKG, and PKV
- FFC: 1024/1536/2048/3072/4096-bits with: DSA SigGen and SigVer; and KAS-DH
- IFC: 1024/1536/2048/3072/4096/8192-bits with RSA E/D; SSA_PKCS1_V1_5 SigGen and SigVer; and ANSI X9.31 SigGen and SigVer

The following illustration shows a typical use model for using the Athena Crypto Coprocessor.

Figure 13-1. Using the Athena TeraFire® 5200B Crypto Coprocessor



Users instantiate a RISC-V CPU for command and control, including fetching keys from the system controller through a system service API, initializing the Athena Core, and setting up DMA to perform the desired function. The TeraFire core comes with a complete firmware driver library for all supported protocols. These driver libraries are delivered to the designer's desktop through our Firmware Catalog within Libero SoC PolarFire.

13.4. Security Features and System Services Summary (Ask a Question)

The following tables summarize the security features and system services.

Table 13-1. Security Features Summary

Feature		PolarFire FPGA	
		Non-S	S
Hardware Security	Supply chain assurance	Available	Available
	Anti-cloning protection	Available	Available
	Device integrity protection	Available	Available
	Hardware Access control with passcodes and security locks	Available	Available
Design Security	Key management	Available	Available
	Encrypted bitstream	Available	Available
	Bitstream versioning	Available	Available
	Digest for data integrity	Available	Available
	Tamper Monitoring on JTAG, Voltage, Temperature, clock glitch, clock frequency, Mesh	Available	Available
Data Security	User Cryptoprocessor and NRBG	NA	Available
	DPA protection CRI pass-through license	NA	Available
	Digital Signature Service	NA	Available
	Secure NVM Wite	Plaintext only	Plaintext, authenticated plaintext, authenticated ciphertext
	Secure NVM Read	Plaintext only	Plaintext, authenticated plaintext, authenticated ciphertext
	PUF Emulation	NA	Available
	Nonce Service	Entropy from PUF	Entropy from PUF + Device unique key

Table 13-2. System Services Summary

System Services		PolarFire FPGA	
		Non-S	S
Device and Design Information Services	Serial Number Service	Available	Available
	Usercode Service	Available	Available
	Design Information service	Available	Available
	Device Certificate Service	Available	Available
	Read Digest SERvice	Available	Available
	Query Security Service	Available	Available
	Read Debug Information Service	Available	Available
Design Programming Services	Bitstream Authentication Service	Available	Available
	IAP Image Authentication Service	Available	Available

Table 13-2. System Services Summary (continued)

System Services		PolarFire FPGA	
		Non-S	S
Fabric Services	Digest Check Service	Available	Available
	In-Application Programming Service	Available	Available
	Auto Update Service	Available	Available
SPI Flash Memory Read Service	SPI Copy Service	Available	Available

14. PolarFire FPGA Device Offerings (Ask a Question)

PolarFire FPGAs offer low-power transceiver devices and various device offerings with transceivers, such as design security, data security, and low-power data security. All PolarFire FPGAs are integrated with multi-protocol industry-leading low-power transceivers. Low power (L) devices provide up to 35 percent lower static power with identical electrical specifications to the STD speed grade device. Also, data security (S) devices integrate a DPA-resistant crypto accelerator.

The following table lists the PolarFire FPGA device options available in extended commercial and industrial temperature grades using the MPF300T as an example. The MPF050T, MPF100T, MPF200T, and MPF500T device densities have identical offerings. Temperatures listed are junction temperatures. The complete list of device offerings in extended commercial, industrial, military, and automotive T2 offerings are available in Appendix: Device Offering.

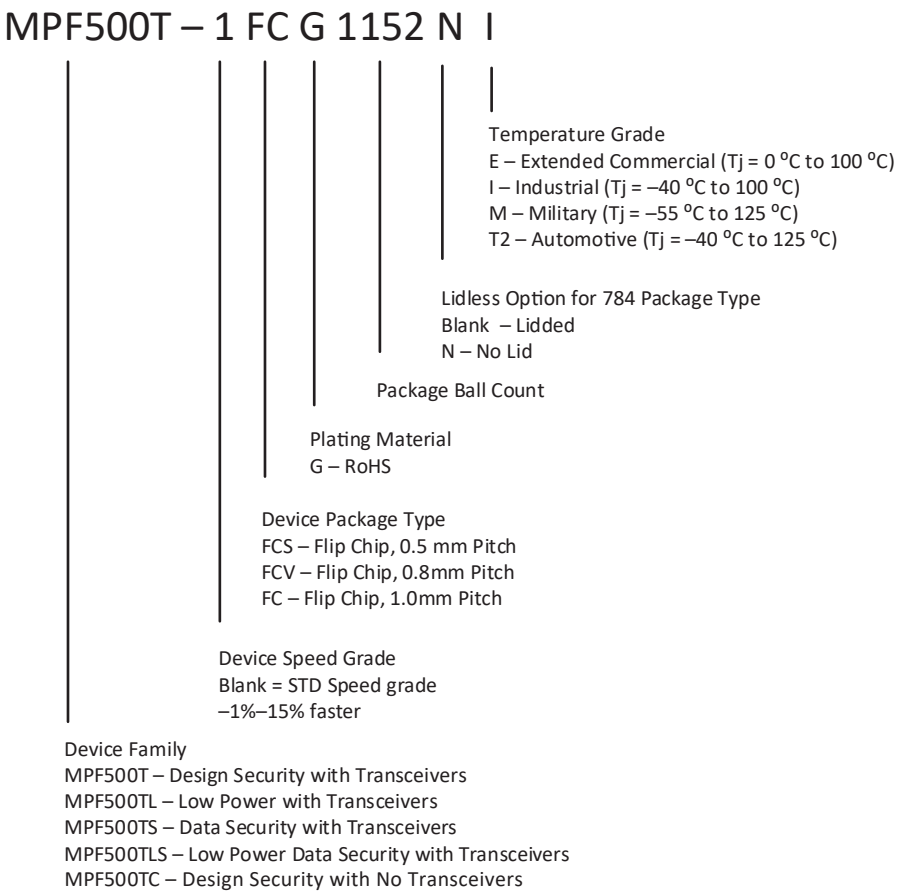
Table 14-1. PolarFire FPGA Offerings

Device Options	Extended Commercial Temperature (E) 0°C–100 °C	Industrial Temperature (I) –40 °C–100 °C	STD Speed Grade	–1 Speed Grade	Lower Static Power (L)	Data Security (S)
MPF300T	Yes	Yes	Yes	Yes	—	—
MPF300TL	Yes	Yes	Yes	—	Yes	—
MPF300TS	—	Yes	Yes	Yes	—	Yes
MPF300TLS	—	Yes	Yes	—	Yes	Yes
MPF300TC	Yes	Yes	Yes	—	—	—

15. Ordering Information (Ask a Question)

PolarFire FPGAs are offered with multiple speed grades, temperatures, and package combinations. All FPGAs are equipped with low-power transceivers. All temperatures are specified as junction temperatures.

Figure 15-1. Ordering Information



15.1. Packaging (Ask a Question)

All PolarFire devices come in high-performance flip-chip packaging. 1.0 mm pitch devices include on-substrate decoupling capacitors to improve device and transceiver performance in those packages. 0.8 mm packages and 0.5 mm packages do not include on-substrate decoupling capacitors. For more information, see the PolarFire Packaging User Guide and the Material Safety Datasheets.

Lidless Packaging Options

The 1.0 mm 484 package is a lidless package. In addition to the 1.0 mm 484, the MPF300T in the 1.0 mm 784 package is available in a lidded or lidless version. The following MPF300Ts can be ordered in a lidless 784 package:

- MPF300T-FCG784NI
- MPF300T-1FCG784NI
- MPF300TS-FCG784NI
- MPF300TS-1FCG784NI

16. Export Classification (Ask a Question)

The export control classification numbers (ECCN) of PolarFire FPGAs are available at www.microchip.com/exportcontroldata.

17. Appendix: Device Offering (Ask a Question)

The devices offered in PolarFire FPGAs are listed below.

Table 17-1. PolarFire FPGA Extended Commercial and Industrial Temperature Offerings

MPF050T-1FCSG325E	MPF200T-1FCVG484E	MPF300T-FCG784E
MPF050T-1FCSG325I	MPF200T-1FCVG484I	MPF300T-FCG784I
MPF050T-1FCVG484E	MPF200T-FCG484E	MPF300T-FCG784NE
MPF050T-1FCVG484I	MPF200T-FCG484I	MPF300T-FCG784NI
MPF050T-FCSG325E	MPF200T-FCG784E	MPF300T-FCSG536E
MPF050T-FCSG325I	MPF200T-FCG784I	MPF300T-FCSG536I
MPF050T-FCVG484E	MPF200T-FCSG325E	MPF300T-FCVG484E
MPF050T-FCVG484I	MPF200T-FCSG325I	MPF300T-FCVG484I
MPF050TL-FCSG325E	MPF200T-FCSG536E	MPF300TL-FCG1152E
MPF050TL-FCSG325I	MPF200T-FCSG536I	MPF300TL-FCG1152I
MPF050TL-FCVG484E	MPF200T-FCVG484E	MPF300TL-FCG484E
MPF050TL-FCVG484I	MPF200T-FCVG484I	MPF300TL-FCG484I
MPF050TLS-FCSG325I	MPF200TL-FCG484E	MPF300TL-FCG784E
MPF050TLS-FCVG484I	MPF200TL-FCG484I	MPF300TL-FCG784I
MPF050TS-1FCSG325I	MPF200TL-FCG784E	MPF300TL-FCSG536E
MPF050TS-1FCVG484I	MPF200TL-FCG784I	MPF300TL-FCSG536I
MPF050TS-FCSG325I	MPF200TL-FCSG325E	MPF300TL-FCVG484E
MPF050TS-FCVG484I	MPF200TL-FCSG325I	MPF300TL-FCVG484I
MPF100T-1FCG484E	MPF200TL-FCSG536E	MPF300TLS-FCG1152I
MPF100T-1FCG484I	MPF200TL-FCSG536I	MPF300TLS-FCG484I
MPF100T-1FCSG325E	MPF200TL-FCVG484E	MPF300TLS-FCG784I
MPF100T-1FCSG325I	MPF200TL-FCVG484I	MPF300TLS-FCSG536I
MPF100T-1FCVG484E	MPF200TLS-FCG484I	MPF300TLS-FCVG484I
MPF100T-1FCVG484I	MPF200TLS-FCG784I	MPF300TS-1FCG1152I
MPF100T-FCG484E	MPF200TLS-FCSG325I	MPF300TS-1FCG484I
MPF100T-FCG484I	MPF200TLS-FCSG536I	MPF300TS-1FCG784I
MPF100T-FCSG325E	MPF200TLS-FCVG484I	MPF300TS-1FCG784NI
MPF100T-FCSG325I	MPF200TS-1FCG484I	MPF300TS-1FCSG536I
MPF100T-FCVG484E	MPF200TS-1FCG784I	MPF300TS-1FCVG484I
MPF100T-FCVG484I	MPF200TS-1FCSG325I	MPF300TS-FCG1152I
MPF100TL-FCG484E	MPF200TS-1FCSG536I	MPF300TS-FCG484I
MPF100TL-FCG484I	MPF200TS-1FCVG484I	MPF300TS-FCG784I
MPF100TL-FCSG325E	MPF200TS-FCG484I	MPF300TS-FCG784NI
MPF100TL-FCSG325I	MPF200TS-FCG784I	MPF300TS-FCSG536I
MPF100TL-FCVG484E	MPF200TS-FCSG325I	MPF300TS-FCVG484I
MPF100TL-FCVG484I	MPF200TS-FCSG536I	MPF500T-1FCG1152E
MPF100TLS-FCG484I	MPF200TS-FCVG484I	MPF500T-1FCG1152I
MPF100TLS-FCSG325I	MPF300T-1FCG1152E	MPF500T-1FCG784E
MPF100TLS-FCVG484I	MPF300T-1FCG1152I	MPF500T-1FCG784I
MPF100TS-1FCG484I	MPF300T-1FCG484E	MPF500T-FCG1152E
MPF100TS-1FCSG325I	MPF300T-1FCG484I	MPF500T-FCG1152I
MPF100TS-1FCVG484I	MPF300T-1FCG784E	MPF500T-FCG784E

MPF100TS-FCG484I	MPF300T-1FCG784I	MPF500T-FCG784I
MPF100TS-FCSG325I	MPF300T-1FCG784NE	MPF500TL-FCG1152E
MPF100TS-FCVG484I	MPF300T-1FCG784NI	MPF500TL-FCG1152I
MPF200T-1FCG484E	MPF300T-1FCSG536E	MPF500TL-FCG784E
MPF200T-1FCG484I	MPF300T-1FCSG536I	MPF500TL-FCG784I
MPF200T-1FCG784E	MPF300T-1FCVG484E	MPF500TLS-FCG1152I
MPF200T-1FCG784I	MPF300T-1FCVG484I	MPF500TLS-FCG784I
MPF200T-1FCSG325E	MPF300T-FCG1152E	MPF500TS-1FCG1152I
MPF200T-1FCSG325I	MPF300T-FCG1152I	MPF500TS-1FCG784I
MPF200T-1FCSG536E	MPF300T-FCG484E	MPF500TS-FCG1152I
MPF200T-1FCSG536I	MPF300T-FCG484I	MPF500TS-FCG784I

Table 17-2. PolarFire Core FPGA Extended Commercial and Industrial Temperature Offerings

MPF050TC-FCSG325E	MPF200TC-FCG784E	MPF300TC-FCG784E
MPF050TC-FCSG325I	MPF200TC-FCG784I	MPF300TC-FCG784I
MPF050TC-FCVG484E	MPF200TC-FCSG325E	MPF300TC-FCSG536E
MPF050TC-FCVG484I	MPF200TC-FCSG325I	MPF300TC-FCSG536I
MPF100TC-FCG484E	MPF200TC-FCSG536E	MPF300TC-FCVG484E
MPF100TC-FCG484I	MPF200TC-FCSG536I	MPF300TC-FCVG484I
MPF100TC-FCSG325E	MPF200TC-FCVG484E	MPF500TC-FCG1152E
MPF100TC-FCSG325I	MPF200TC-FCVG484I	MPF500TC-FCG1152I
MPF100TC-FCVG484E	MPF300TC-FCG1152E	MPF500TC-FCG784E
MPF100TC-FCVG484I	MPF300TC-FCG1152I	MPF500TC-FCG784I
MPF200TC-FCG484E	MPF300TC-FCG484E	—
MPF200TC-FCG484I	MPF300TC-FCG484I	—

Table 17-3. PolarFire FPGA Military Temperature Offerings

The PolarFire FPGA military temperature devices are offered with data security "S", STD speed grade and in leaded package.

MPF200TS-FCS325M	MPF300TS-FCS536M	MPF500TS-FC1152M
MPF300TS-FC484M	MPF300TS-FCV484M	—
MPF300TS-FC784M	MPF500TS-FC784M	—

Table 17-4. PolarFire FPGA Automotive AECQ-100 (T2) Offerings

MPF050T-1FCSG325T2	MPF100T-FCVG484T2	MPF300T-1FCSG536T2
MPF050T-1FCVG484T2	MPF200T-1FCG484T2	MPF300T-1FCVG484T2
MPF050T-FCSG325T2	MPF200T-1FCSG325T2	MPF300T-FCSG536T2
MPF050T-FCVG484T2	MPF200T-1FCSG536T2	MPF300T-FCVG484T2
MPF100T-1FCG484T2	MPF200T-1FCVG484T2	MPF300TS-1FCVG484T2
MPF100T-1FCSG325T2	MPF200T-FCG484T2	MPF300TS-FCVG484T2
MPF100T-1FCVG484T2	MPF200T-FCSG325T2	MPF500TS-1FCG784T2
MPF100T-FCG484T2	MPF200TS-1FCVG484T2	MPF500TS-1FCG1152T2
MPF100TS-1FCVG484T2	MPF200TS-FCVG484T2	MPF500TS-FCG1152T2
MPF100TS-FCVG484T2	MPF200T-FCSG536T2	MPF500TS-FCG784T2
MPF100T-FCSG325T2	MPF200T-FCVG484T2	—

Table 17-5. PolarFire Core FPGA Automotive AECQ-100 (T2) Offerings

MPF050TC-FCSG325T2	MPF100TC-FCVG484T2	MPF200TC-FCVG484T2
MPF050TC-FCVG484T2	MPF200TC-FCG484T2	MPF300TC-FCSG536T2
MPF100TC-FCG484T2	MPF200TC-FCSG325T2	MPF300TC-FCVG484T2
MPF100TC-FCSG325T2	MPF200TC-FCSG536T2	MPF500TC-FCG784T2

18. Revision History (Ask a Question)

Revision	Date	Description
R	05/2025	• Updated Block Diagram. • Updated tables in Appendix: Device Offering.
Q	05/2025	• Added PolarFire SoC core information to Overview. • Updated Block Diagram. • Added note to Product Family Table. • Added MPF300TC to PolarFire FPGA Device Offerings. • Added MPF500TC to Ordering Information. • Added new devices to respective temperature grade tables under Appendix: Device Offering.
P	07/2024	• Corrected list of devices in Appendix: Device Offering.
N	06/2024	• Made the following updates to table PolarFire FPGA Product Family: – Corrected SERDES speed specification. – Corrected User I/O count of MPF050T in FCVG484 package and automotive packages. – Added note under table. • Removed device lists from PolarFire FPGA Device Offerings and added reference to Appendix: Device Offering. • A complete list of devices offered is in Appendix: Device Offering.
M	12/2023	• Replaced references to ECCN with a weblink that has the latest information.
L	08/2023	• Added more feature details in section Security. • Included new automotive T2 device in the FCG784 package in PolarFire FPGA Device Offerings and Product Family Table.
K	08/2022	• Updated ECCN# for military-grade devices in Table 14-3. Orderable Military Device Part Numbers.
J	08/2022	• Updated export classifications for military-grade devices in section Export Classification.
H	07/2021	• Updated Export Classifications. • Corrected typos in Figure 2-1. PolarFire FPGA Block Diagram.
G	05/2021	• Updated Table 3-1. PolarFire FPGA Product Family with Type/Size/Pitch information for Commercial/Industrial and Automotive.
F	05/2021	• Updated Figure 2-1. PolarFire FPGA Block Diagram.
E	02/2021	• Updated Table 3-1. PolarFire FPGA Product Family. • Updated Figure 13-1. Using the Athena TeraFire 5200B Crypto Coprocessor.
D	02/2021	• Removed "Figure 7-1. PCI Express Hard Macro Lane Sharing".
C	12/2020	• Removed "Table 6-2. Quad0 Lane Assignments" and referred users to *UG0685: PolarFire FPGA PCI Express User Guide* for detailed lane assignments.

Revision History (continued)

Revision	Date	Description
B	12/2020	• Added automotive-grade device information to Overview. • Updated number of SGMII CDRs for the 1152 package in the PolarFire FPGA Product Family table. • Added note to the the PolarFire FPGA Product Family table. • Corrected PCIe lane assignments in the Quad0 Lane Assignments table. • Added new military temperature device in the PolarFire FPGA Military Temperature Offering table and Orderable Military Device Part Numbers table. • Added Orderable Automotive Device Part Numbers table. • Added automotive ordering code to Ordering Information.
A	09/2020	The following is the summary of changes in revision A: • The document was updated to Microchip template. • Packaging section was updated to correct the ordering information for the lidless device • Polarfire FPGA Export Classification was updated to reflect an updated device export classification
1.7	04/2020	The following is the summary of changes in revision 1.7: • PolarFire FPGA Block Diagram was updated. • References to DDR2 support in GPIO were removed. • The Military device offering section was updated. • I/O Digital Modes section was deleted. For details, see *AC/DC electrical characteristics datasheet.* • Packaging section was added to indicate a new lidless 784 package option.
1.6	10/2019	The following is the summary of changes in revision 1.6: • Voltage glitch detectors were removed. • I/O types and speeds were removed. See the *PolarFire Datasheet* for I/O standard support by I/O type and corresponding rates.
1.5	03/2019	The following is the summary of changes in revision 1.5: • Flash*Freeze mode was removed from I/Os, Low Power, and System Services sections.
1.4	09/2018	The following is the summary of changes in revision 1.4: • Flash*Freeze mode was removed. • Export Classification section was added.
1.3	06/2018	The following is the summary of changes in revision 1.3: • Block Diagram was updated. • I/Os and Data Security sections were updated to reflect changes in the preliminary datasheet.
1.2	08/2017	The following is the summary of changes in revision 1.2: • LVDS rates were changed to a max of 1.25G. For more information, see Differential I/O Standards.
1.1	05/2017	The following is the summary of changes in revision 1.1: • The Product Family Table was updated. • Information about the Dedicated SPI Programming Port section was updated. • The PolarFire FPGA Device Offerings section was updated.
1.0	02/2017	This is the initial release of this document.

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