

## Introduction

The PolarFire® SoC FPGA family devices are subjected to the limitations described in this errata document. This document contains updated information about known devices specific issues and provides the available limitations and workarounds. For more information, contact [Microchip Technical Support](#).

## PCB Designs

For information about how to determine proper signal pinout, see the [PolarFire® SoC FPGA Board Design Guidelines User Guide](#). The proper signal pinout is needed for all clocking, transceiver and FPGA pin recommendations.

## Device Identification

The following figures show the PolarFire SoC FPGA production samples.

**Figure 1.** Device Identification Markings: Pre-Production Devices

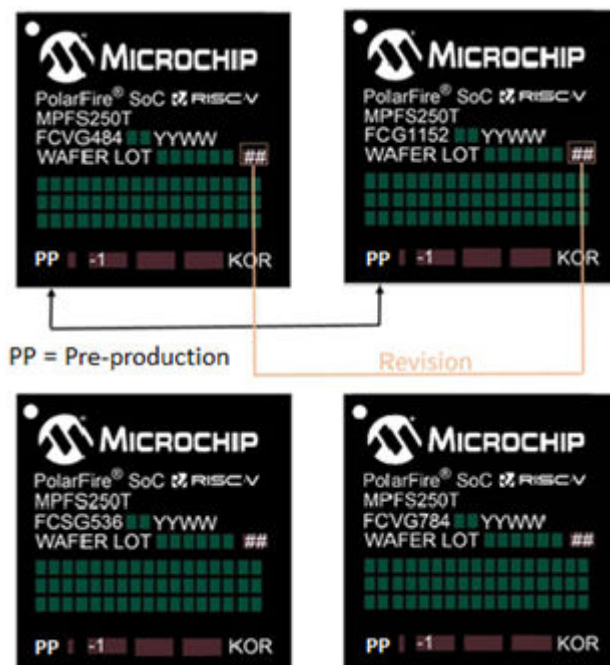
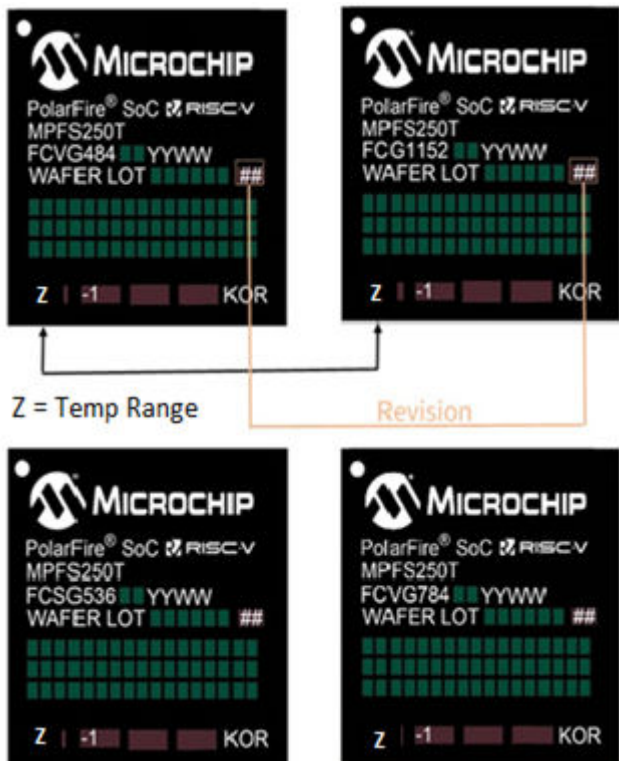


Figure 2. Device Identification Markings: Production Devices



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## 1. Errata Descriptions and Workarounds

The following section describes the device errata and the workarounds. The following table lists the errata for Engineering Samples (ES), Pre-Production (PP) silicon and production silicon. For device part marking specifications, see [Device Identification](#).

**Table 1-1.** Summary of PolarFire® SoC FPGA Errata

PolarFire® SoC MPFS250T Errata History	Silicon Revisions			
	ES <sup>1</sup>	Pre-Production		Production
	Revision 0	Revision 0	Revision 1	Revision 0
Microprocessor Subsystem (MSS) cannot access system controller SPI Flash.	* <sup>2</sup>	X <sup>3</sup>	X	X
AXI Switch Memory Protection Unit (MPU) is not operational.	*	X	X	X
MSS I <sup>2</sup> C peripheral works only with MSS core version 2.0.108 and above.	*	X	X	X
When MSS CPU's frequency is limited to 600 MHz.	*	X	X	X
When MSS works as a master, DRI interrupt line must not be used.	*	X	X	X
DRI error and DRI fault interrupts are not connected to the maintenance interrupt.	*	X	X	X
MSS GPIO configuration registers must only be reset by the CPUs.	*	X	X	X
Fabric APB DRI's slow writes corrupt the SmartDebug JTAG/SPI read data.	*	X	X	X
System controller suspend mode is not supported.	*	X	X	X
PolarFire SoC MSS GEM (Gigabit Ethernet MAC) has an issue with Undersize Frame Counter in Ethernet statistics.	*	X	X	X
Auto-program or Auto-update of eNVM must not be used.	*	X	X	X
Auto-update system service allows SPI master mode to be used incorrectly configured for SPI slave mode.	*	X	X	X
JTAG zeroization at the end of programming causing auto programming to kick in post zeroizing.	*	*	X	X
PCIe SECEDED ECC reporting counters and interrupts	*	*	*	*
Maximum DDR die density supported by the PolarFire SoC MSS DDR controller	*	*	*	*
External VERIFY_DIGEST with POR Digest Check for Fabric Components	*	*	*	*

### Notes:

1. See the [Errata for PolarFire® SoC ES Devices](#).
2. \* indicates that the errata exists for the specified silicon revision.
3. X indicates that the issue is fixed in the specified silicon revision.

## 1.1. MSS I<sup>2</sup>C in Fabric Mode Works Only With MSS Configurator v2022.2 and Above

MSS I<sup>2</sup>C configured in the Fabric mode does not function as expected in PolarFire SoC pre-production or production devices. For a workaround, use MSS Configurator v2022.2 or later. See the following Microchip Knowledge Base article for more information:

[MSS-I2C configured in FABRIC mode with Libero SoC v2022.1 \(or earlier\) may not work as intended for PolarFire SoC devices.](#)

**Note:** This issue does not affect the ES devices.

## 1.2. Production Validation Status

This section details the PolarFire SoC MPFS025T and PolarFire SoC MPFS250T product validation status for Revision 0.

### 1.2.1. eMMC HS400 and HS400 Enhanced Strobe Modes

eMMC validation over process, voltage and temperature is completed for all supported modes.

See *PolarFire SOC MSS Technical Reference Manual* for more information about eMMC supported modes or contact [Microchip Technical Support](#).

### 1.2.2. LPDDR4 Bring Up, Debug and Validation

LPDDR4 validation over process, voltage and temperature is completed. For reference board design files and board design practices to achieve expected performance from PCBs and PolarFire SoC devices, see [PolarFire® SoC FPGA Board Design Guidelines User Guide](#).



**Important:** For additional information for design, bring up, debug and validation of LPDDR4-based system, see the [PolarFire Family Memory Controller User Guide](#).

### 1.2.3. SD Compliance

The following lists the SD compliance status.

- SD validation over process, voltage, and temperature is completed for all the modes.
- Compliance is completed for SD-DS and SD-HS modes.
- Compliance for UHS-I SDR12, UHS-I SDR25, UHS-I SDR50, UHS-I SDR104 and UHS-I DDR50 is completed.

For more information about SD supported modes, see *PolarFire SOC MSS Technical Reference Manual* or contact [Microchip Technical Support](#).

## 1.3. PCIe® SECEDED Reporting Defeated

When ECC is enabled (default) within the PCIe hard IP block, the single error correction and double error detection error reporting counters and interrupt registers show erroneous values. The following features of the PCIe SECEDED are being defeated:

- Single error correction reporting features
- Double error detection feature

More information about this is available in the [change impact analysis document](#).

## 1.4. Maximum Supported DDR Die Density for MSS DDR Controller

Memory manufacturers specify refresh interval requirements based on the memory's operating case temperature ( $T_C$ ). The PolarFire SoC MSS DDR controller has a limitation that restricts the refresh interval ( $t_{REFI}$ )<sup>1</sup> to be at least 4 times the refresh cycle time ( $t_{RFC}$ )<sup>2</sup>. As a result, the max supported DDR die density is restricted at higher temperatures.

The maximum supported DDR densities at different memory case temperatures ( $T_C$ ) are listed in table below.

**Table 1-2.** PolarFire SoC MSS DDRC Max Supported DDR Density

Memory Case Temperature	Max Memory Density (Max Die Density)			
	$-40\text{ }^{\circ}\text{C} < T_C^3 < 85\text{ }^{\circ}\text{C}$	$-40\text{ }^{\circ}\text{C} < T_C < 95\text{ }^{\circ}\text{C}$	$-40\text{ }^{\circ}\text{C} < T_C < 105\text{ }^{\circ}\text{C}$	$-40\text{ }^{\circ}\text{C} < T_C < 125\text{ }^{\circ}\text{C}$
DDR4	128 Gb (16 Gb)	128 Gb (16 Gb)	32 Gb (8 Gb)	8 Gb (2 Gb)
LPDDR4	32 Gb (16 Gb)	8 Gb (4 Gb)	8 Gb (4 Gb)	8 Gb (4 Gb)

**Note:**

The above table details the maximum supported DDR density for a given operating temperature provided the DDR die density is within the maximum mentioned (in parentheses). For example, at a DDR case temperature range of  $-40\text{ }^{\circ}\text{C}$  to  $85\text{ }^{\circ}\text{C}$ , the PolarFire SoC FPGA MSS DDR controller can support up to 128 Gigabit DDR4 memory provided the internal DDR die density doesn't exceed 16 Gigabits. The 128 Gb DDR may be implemented as 4 DDR chips with a 16 Gb dual-rank x8 configuration each.

DDR3 and LPDDR3 memories are also supported by the PolarFire SoC FPGA MSS DDR controller but are not affected by this errata.

For further details, refer to the [PolarFire Family Memory Controller User Guide](#).

## 1.5. Depreciated Feature: Use of External VERIFY\_DIGEST with POR Digest Check for Fabric Components

When the device is configured for Fabric Power-On-Reset (POR) digest check, VERIFY\_DIGEST of fabric components via JTAG/SPI may report false failures and is deprecated. This issue does not affect:

- VERIFY\_DIGEST of non-fabric components
- CHECK\_DIGEST via system service call
- VERIFY\_DIGEST functionality for fabric components when Fabric POR digest check is disabled

For more information, refer to the latest revision of the [PolarFire Family Security User Guide](#).

<sup>1</sup> Refresh Interval ( $t_{REFI}$ ): Time between two refresh commands

<sup>2</sup> Refresh Cycle Time ( $t_{RFC}$ ): Time taken to complete a refresh command

<sup>3</sup>  $T_C$ : Memory case temperature

## 2. Libero<sup>®</sup> SoC Software Errata

For Libero SoC related issues and limitations, see [Libero<sup>®</sup> SoC Release Notes](#).

### 3. Embedded Software Errata

See [SoftConsole Release Notes](#) for more information.

## 4. Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

Revision	Date	Description
F	08/2025	<ul style="list-style-type: none"> <li>SD compliance tests are completed.</li> <li>Added row to <a href="#">Table 1-1. Summary of PolarFire® SoC FPGA Errata</a> for “External VERIFY_DIGEST with POR Digest Check for Fabric Components.”</li> <li><a href="#">Deprecated Feature: Use of External VERIFY_DIGEST with POR Digest Check for Fabric Components.</a></li> </ul>
E	06/2024	<ul style="list-style-type: none"> <li>Refer to the <a href="#">Change Impact Analysis</a> document for this update.</li> <li>Added note on max supported DDR die density in <a href="#">Errata Descriptions and Workarounds</a>.</li> <li>Added section <a href="#">Maximum Supported DDR Die Density for MSS DDR Controller</a>.</li> </ul>
D	01/2024	<ul style="list-style-type: none"> <li>Defeatured PCIe SECCED reporting. More information about this is available in the <a href="#">change impact analysis document</a>.</li> </ul>
C	12/2022	<ul style="list-style-type: none"> <li>Edited <a href="#">Table 1-1 Notes</a>.</li> <li>Added <a href="#">MSS I2C in Fabric Mode Works Only With MSS Configurator v2022.2 and Above</a>.</li> <li>Edited <a href="#">eMMC HS400 and HS400 Enhanced Strobe Modes</a>.</li> <li>Updated <a href="#">LPDDR4 Bring Up, Debug and Validation</a>.</li> </ul>
B	06/2022	Made changes to the revision history and releasing this document for Production Device.
A	06/2022	Internal Release

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