

## Introduction

This functional safety package errata document is an early notification of issues along with a detailed description of the issues, the condition of occurrence, and the workaround. We will be working on updating the Functional Safety User Guide with these issues and further details on workarounds.

## Errata Description

Four issues have been identified and can affect functional safety designs when using the IEC-61508 certified Libero® SoC 11.5 SP2. We are providing this document as an early notification of these issues and will be working on updating the Functional Safety User Guide with these issues and further details on workarounds.

### Microchip Parts Affected

Customers using the SmartFusion®, IGLOO®, and ProASIC3® family of devices that uses the SAFETY-PKG-G3-F or SAFETY-PKG-G3-NL functional safety package.

### Impacts to Data Sheet

Not applicable.

### Change Impact

Customers utilizing any of the outlined configurations to design their high-reliability applications need to evaluate the use and impact to their functional safety designs.

### Change Implementation Status

In Progress. The changes to the functional safety package including the Functional Safety Manual will be completed and provided to customers.

### Method to Identify Change

The Functional Safety User Guide will be updated to reflect the information provided and any identified workarounds for these issues.

### Qualification Plan

Not applicable.

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## 1. Details of Identified Issues and Workaround

Four issues have been identified and can affect functional safety designs when using the IEC-61508 certified Libero SoC 11.5 SP2.

### 1.1 Libero SoC Design Suite Generates Incorrect RAM Configurations When Using SmartGen for IGLOO, ProASIC3, and SmartFusion Families

#### Description

Integrated into Libero® SoC Design Suite, SmartGen generates an incorrect RAM configuration for two-port and dual-port SRAMs in IGLOO, ProASIC3, and SmartFusion family of devices. The issue is that the de-asserted TPSRAM REN (read enable) or DPSRAM BLKA/B signals do not hold read-data when address jumps into another block.

#### Condition of Occurrence

The behavior anomaly occurs in both two-port and dual-port SRAM configurations:

- Two-port RAM configurations of multiple blocks depth-wise and dynamic REN signal
  - When the REN signal is de-asserted and the read address jumps from one block to another block, the read-data is not held (becomes zero).
- Dual-port RAM configurations of multiple blocks depth-wise and dynamic BLKA or BLKB signal
  - When the BLKA or BLKB signal is de-asserted and the corresponding port address jumps from one block to another block, the port's read-data is not held (becomes zero).

Parse the SmartGen log of the RAM component to determine if the configuration contains multiple blocks depth-wise.

#### Workaround

Avoid using any configuration that fits the description. Contact your local Embedded Solution Engineer for details. This issue was fixed in Libero SoC 11.8

### 1.2 Using Libero SoC Design Suite and the Integrated Function SmartTime Does Not Calculate the Clock Generation Correctly

#### Description

Miscalculation of the clock generation delay under specific conditions may yield unreported violations.

#### Condition of Occurrence

Using opposite edges between the source FF and the sink FF or using a clock domain crossing CDC scheme between the ref clock of the CCC and the generated clock.

#### Workaround

Avoid using any configuration that fits the description. Contact your local Embedded Solution Engineer for details. This issue was fixed in Libero SoC 11.7.

### 1.3 Missing Timing Paths for RAM4Kx9 Macro when Using Libero SoC Design Suite's SmartTime

#### Description

A clock-to-out RAM timing arc is missing under specific conditions, which yields in unreported violations.

#### Condition of Occurrence

The RAM must be configured with pass-through and pipeline mode enabled.

**Workaround**

Avoid using any configuration that fits the description . Contact your local Embedded Solution engineer for details. This defect will be logged as a known issue for the certified release.

**1.4 Simulation Issue Found with CoreGPIO v3.1 when VHDL HDL is Used****Description**

The APB slave address (PADDR) of CoreGPIO is not qualified with PSEL signal. Due to this issue, any APB slave address outside the permissible range of CoreGPIO results in a simulation error.

The issue in the IP does not have an impact in hardware validation.

**Condition of Occurrence**

- The issue is observed for the problem mentioned above in VHDL simulation only.
- The issue is observed if the APB slave address falls outside the permissible range of CoreGPIO. The permissible range is based on the CoreGPIO configuration.

**Workaround**

Avoid VHDL simulation that fits the description. Contact your local Embedded Solution engineer for details. This defect will be logged as a known issue for the certified release.

## 2. Revision History

| Revision | Date    | Description  |
|----------|---------|--|
| A        | 05/2023 | This is the initial release of errata with details of newly identified issues potentially affecting functional safety designs utilizing Libero SoC® Design Suite version 11.5 SP2, which is the basis for the Functional Safety package for IGLOO®, ProASIC3®, and SmartFusion® FPGA product families. |

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